CMOS-MEMS Based Optical Electrostatic Phase Shifter Array With Low Driving Voltage and High Fill Factor

Jin-Chern Chiou, Chen-Chun Hung, and Li-Jung Shieh

***Abstract*—This work develops a novel 4×4 optical phase shifting micromirror array that achieves a $\lambda/4$ vertical displacement and makes the mirror peak-to-valley deformation within $\lambda/10$ (514 nm light source). Each individual micromirror pixel is controllable and driven by an electrostatic parallel plate actuator. The mirror reflective surface is an aluminum layer with a high optical reflectivity exceeding 90%. This device achieves a high fill factor of more than 90% without an additional flip-chip bonding process due to the parallel plate actuator and the hidden suspension beam structures. The phase shifter array is fabricated using the Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μm 2p4m CMOS process and post-CMOS process. An in-house post-process is utilized to reserve a 40 μm thick bulk-silicon under the 200 μm$\times$ 200 μm mirror. This eliminates mirror deformation from residual stress after the device is released. The micromirror demonstrates a vertical displacement of $\lambda/4$ at only 3 V and the resonant frequency is 3.6 kHz. Industry can use this phase-shifting micromirror array as a spatial light modulator in holographic data storage systems in the future.**

***Index Terms*—CMOS MEMS, MEMS, micromirror, MOEMS, phase shifter.**

I. Introduction

OPTICAL MEMS have flourished over the last decade by leveraging IC micro-fabrication technology [1]. Their applications include projection displays [2], optical scanners [3] and imaging systems [4]. Among these devices, optical phase shifter plays an important role in the light-diffraction interference. If a phase shifter can be operated in in-phase mode (0° phase difference) and out-of-phase mode (180° phase difference) respectively, the capacity of a holographic data storage system can be increased in double. Furthermore, this capacity will be increased by 2^{N} times when N phase shifters are in the system [5], [6].

Among the existing actuation methods for MEMS mirrors that were previously proposed are included electrostatic, piezoelectric and thermal. Electrostatic actuation is the most widely used method in micromachined mirrors [7]–[10]. The main benefit of electrostatic actuation is its low power consumption and capability for sub-micrometer displacement in optical devices. Furthermore, unlike piezoelectric devices, electrostatic devices are compatible with the CMOS process [11], [12]. Interferometry using an electrostatic driven microactuator can precisely control displacements in the nanometer range, and the required actuation force is usually low [13]. Recently, many electrostatic actuation methods have been developed, such as the parallel plate, lateral comb drive and vertical comb drive structures. Vertical out-of-plane motion micromirrors with a parallel plate electrostatic actuator have a nonlinear phenomenon, called pull-in, which severely constrains the stable region at one-third the length of the gap [14], [15]. Electrostatic comb drive actuators were developed to avoid pull-in. However, a drawback of electrostatic actuators is its high driving voltage which is not suitable for portable devices.

In general, surface flatness is an important issue when designing MEMS mirrors. Micromirrors made of thin film materials usually have a curved surface due to residual stress once the structure is released [16], [17]. Stress-induced out-of-plane deformation must be small compared to the optical wavelength to avoid adversely affecting device performance. Thus, a number of methods have been proposed to eliminate curvature or reduce residual stress of the micromirrors. For example, a thick bulk-silicon micromirror fabricated via DRIE process can overcome the nonplanarity of thin film CMOS microstructures [18]. Moreover, bombarding the microstructure surface with ions is also a method of modifying the residue stress gradient [19], [20].

In addition to mirror flatness, fill factor also plays an important role in optical applications. Previously reported micromirror arrays with a low fill factor resulted in low optical efficiency [21], [22]. In order to achieve an effectively high fill factor, driving and suspension mechanisms usually must be placed under the mirror plate. The most famous example is the Texas Instruments Digital Light Processor (TI DLPTM) mirror system that has a complicated superstructure to obtain a high fill factor in projection display application [23]. Besides, additional assembly process such as flip-chip bonding technique is also utilized to place the mirror plate on top of the actuator stage [24]–[27].

In order to overcome the above-mentioned drawbacks in fabricating micromirror, this work develops an optical phase

Manuscript received November 09, 2009; revised January 04, 2010. Current version published September 29, 2010. This work was supported in part by Ministry of Economic Affairs, Taiwan, R.O.C., under contract 97-EC-17-A-07-S1-011, in part by the National Science Council, Taiwan, R.O.C., under contracts NSC-98-2220-E-009-014, NSC-98-2220-E-009-032, and NSC-98-2218-E-039-001, and in part by Taiwan Department of Health Clinical Trial and Research Center of Excellence under contract DOH99-TD-B-111-004.

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Digital Object Identifier 10.1109/JQE.2010.2043502

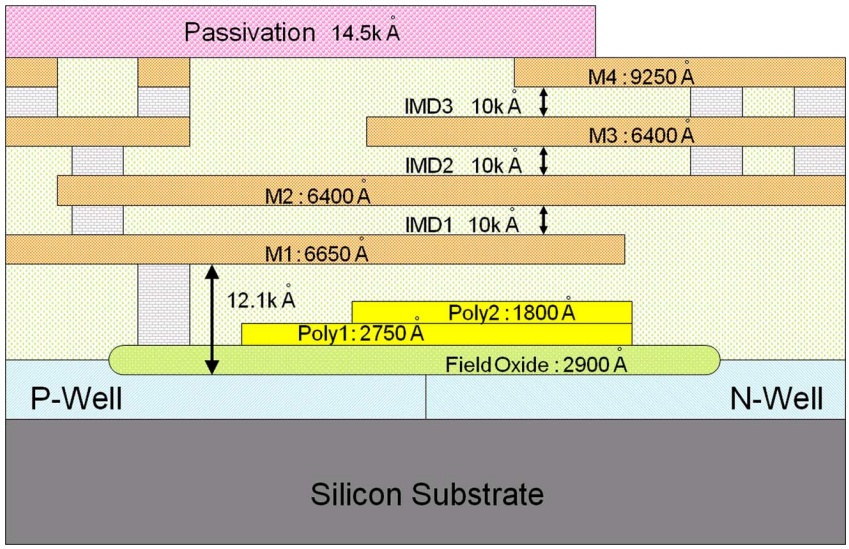

Fig. 1. The cross-section view of the TSMC CMOS MEMS process.

shifting micromirror array that can achieve a $\lambda/4$ vertical displacement and a mirror peak-to-valley deformation within $\lambda/10$. The fill factor is about 90% without additional flip-chip bonding process. Electrostatic actuators are employed to drive each individual mirror pixel. The standard CMOS process and in-house post-CMOS process are utilized to fabricate the device. The following sections describe device design, present theoretical analysis and simulation results, and provide fabrication details. Experimental results demonstrate that the micromirror had a vertical displacement of $\lambda/4$ at only 3 V and resonant frequency of 3.6 kHz.

II. Design Concept

The optical phase-shifting micromirror array is fabricated by the Taiwan Semiconductor Manufacturing Company (TSMC) standard 0.35 μm 2p4m (double polysilicon quadruple metal) CMOS process [28]. Fig. 1 depicts the cross-section view of the TSMC CMOS MEMS process. The micromirror is designed to achieve a $\lambda/4$ vertical displacement for a 514 nm wavelength light source. Fig. 2 illustrates the schematic drawings of an individual electrostatic driven mirror pixel. It consists of a 200 μm$\times$ 200 μm micromirror surface structure, suspension beams, net electrode, pillar-shape joiners, and proof mass. The micromirror is supported by two suspension beams and formed by metal 4 (M4), as shown in Fig. 2(a). The mirror reflective surface is an aluminum metal layer with high optical reflectivity exceeding 90%. The suspended beams are designed to be under the mirror plate. One end of the beam is fixed to an anchor and the other end is attached to the micromirror.

An electrostatic parallel plate actuator drives the mirror. The top electrode is the mirror plate and the bottom electrode is a net electrode. The net electrode is a clamped-clamped suspension structure, which acts as a stator. It is composed of M2, M3, and a tungsten layer between M2 and M3. The gap between mirror plate and net electrode is 1 μm, and one-third of the gap is larger than the desired micromirror motion displacement (128 nm). Therefore, the pull-in phenomenon can be avoided by applying a proper driving voltage. A 40 μm-thick bulk-silicon under the micromirror is reserved for reducing mirror deformation due to residual stress after the structure is released [29]. In order to connect the mirror plate and silicon proof mass, pillar-shape structures are designed for connectors, as shown in Fig. 2(b). The pillar-shape structure comprises all metal layers and tungsten via layers besides M4. The mirror and pillars act as a rotor. Fig. 2(c) shows stereo drawing of the whole micromirror structure. The pillars pass through the net electrode; thus, the rotor does not touch the stator. When voltage is applied between the stator and rotor, the electrostatic force pulls the micromirror downward. Thus, the multilayer structure provides vertical motion capability. The micromirror array achieves a high fill factor of more than 90% without an additional flip-chip bonding process because of the parallel plate actuator and the hidden suspension beams.

III. Theoretical Analysis and FEM Simulation

A. Static Behavior

Vertical motion of an electrostatic parallel plate actuator occurs when a driving voltage is applied between the top and bottom electrodes. The electrostatic force is given by

$$F = \frac{1}{2}\frac{dC}{dz}V^2 \tag{1}$$

where C is the capacitance between the electrodes, z is the vertical displacement along the actuation direction, and V is the applied DC bias voltage. For a parallel plate actuator, the capacitance varies with vertical displacement. Thus C can be expressed as

$$C = \frac{\varepsilon A}{(d-z)} \tag{2}$$

where ε is the dielectric constant in the air, A is the overlap area of top and bottom electrodes, and d is the gap between

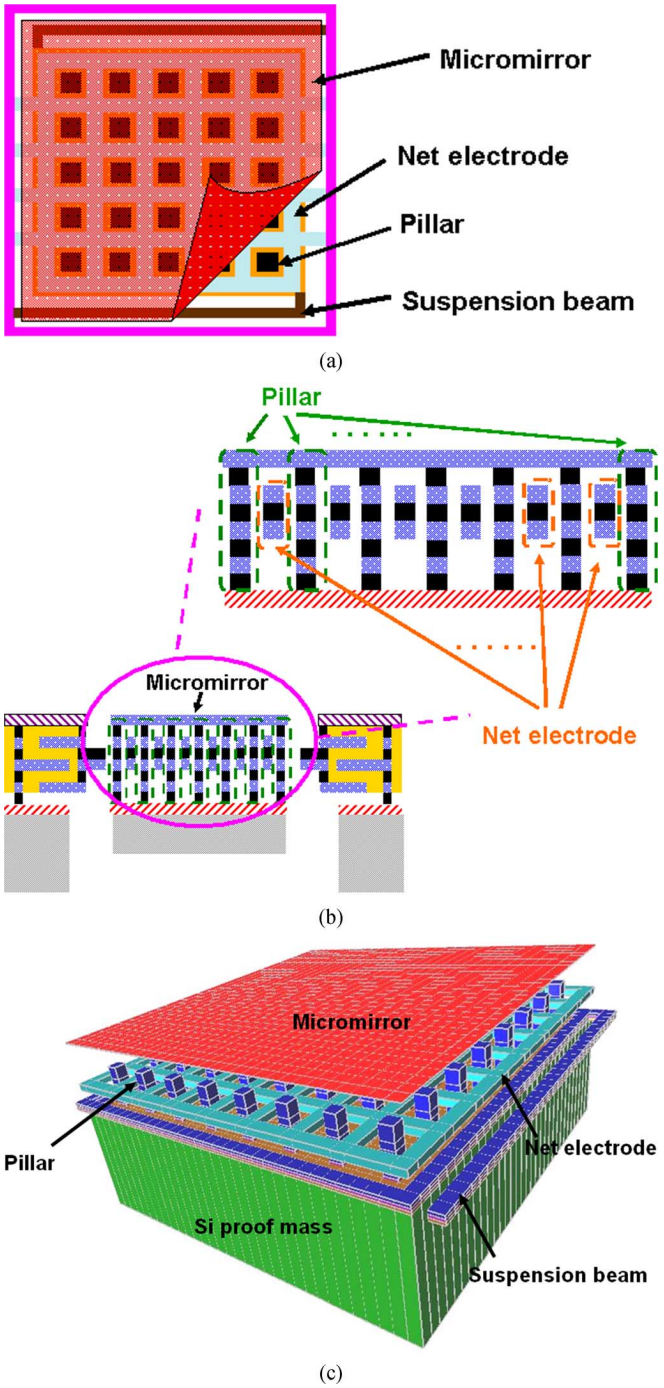

Fig. 2. The schematic of an individual mirror pixel: (a) top view; (b) cross-section view; (c) stereopicture of the micromirror.

electrodes. By summarizing (2) and (1), electrostatic force can be rewritten as a function of applied voltage and shown in (3)

$$F = \frac{1}{2}\frac{dC}{dz}V^2 = \frac{1}{2}\varepsilon A\left(\frac{V}{d-z}\right)^2. \tag{3}$$

According to spring design of the proposed device, the micromirror is considered to follow Hooke's law. While assuming the micromorror is driven by an electrostatic force F along the driving direction, the relationship between displacement and the reaction force F in the driving direction x can be expressed as

$$F = kx \tag{4}$$

where k represents the equivalent spring stiffness of the micromirror in the driving direction and x represents the displacement caused by the electrostatic force. In our case, the displacement x is equal to z, and the equivalent stiffness k is the summary of stiffness of two cantilever springs. Since (3) equals to (4) which yields (5) that specifies the relationship between moved displacement z and driving voltage V in the z direction

$$V = (d-z)\sqrt{\frac{2zk}{\varepsilon A}}. \tag{5}$$

In the present case, d is a constant value of 1 μm (distance between M3 and M4), A is square measure of net electrodes, k is spring constant of cantilever springs, and ε is the dielectric constant in the air. Based on (5), when the displacement is achieved 128 nm ($\lambda/4$), the relative driving voltage is about 2.6 V.

To understand the static behaviors of the device, a FEM simulator, IntelliSuite, is utilized to simulate micromirror deformation and displacement. Fig. 3 displays the simulation result of the actual dimension micromirror model with a driving voltage of 3 V. Micromirror displacement is clearly of the same with the free end of the suspension beams. That is, deformation of the suspension beams induced by the electrostatic force can fully pass to the micromirror and lead to a vertical levitation of the micromirror. Fig. 4 plots micromirror displacement versus driving voltage. The simulation result demonstrates that the micromirror can achieve a 128 nm ($\lambda/4$) vertical displacement when applied voltage is about 2.7 V. Moreover, the pull-in voltage is about 4.5 V according to the simulation result.

B. Resonant Frequency

A simplified theoretical model is utilized to calculate the resonant frequency of the proposed micromirror device. Deformation of the suspension beams which induced by an electrostatic force lead to a vertical levitation of the micromirror. Thus, the device model is similar to that of a clamped-clamped beam with a center mass, as illustrated in Fig. 5. The fundamental resonant frequency of the equivalent model is expressed as [30]

$$f = \frac{4}{\pi}\sqrt{\frac{3\times\sum_{i=1}^{N} E_i I_i}{L_B^3(M_B + 0.37m_B)}} \tag{6}$$

where N is the number of layers in the suspension beam; E_i and I_i are the Young's modulus and the moment of inertia of each layer, respectively; L_B and m_B are the length and the mass of the equivalent clamped-clamped beam, respectively; and M_B is micromirror mass. The theoretical resonant frequency derived by (6) is 3.94 kHz. Moreover, resonant frequency is also simulated using IntelliSuite. Notably the FEM simulations only require suspension beams and micromirror to calculate the resonant frequency. The simulation result indicates that the fundamental resonant frequency is about 4.14 kHz and the mode

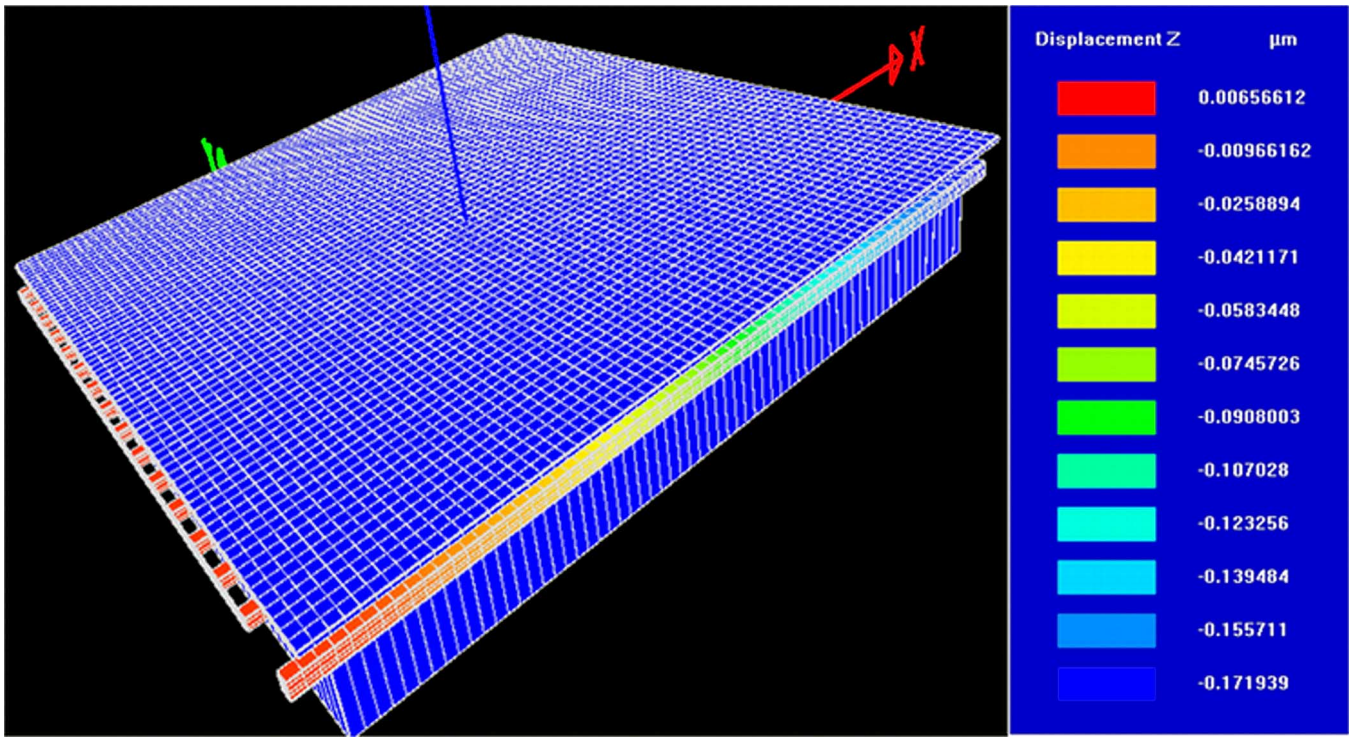

Fig. 3. The deformation of the actual micromirror model with 3 V DC bias voltage.

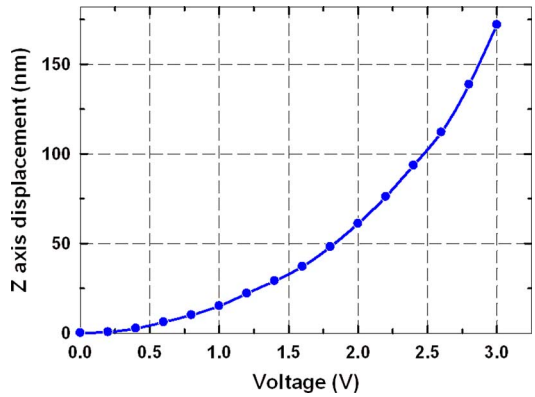

Fig. 4. The simulation result of Z-axis displacement versus driving voltage.

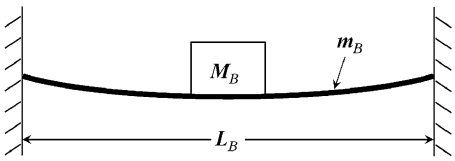

Fig. 5. The diagram of clamped-clamped beam with a center mass.

shape is vertical motion. These results can be used as the reference data in actual experimental measurements.

IV. Fabrication

The designed phase shifter device was manufactured using the TSMC 0.35 μm 2p4m CMOS process that was provided by the National Chip Implementation Center (CIC) [28] and a self-designed post-CMOS process. The CMOS process consists of two polysilicon layers, four metal layers, three via layers, and several dielectric layers. All metal layers are made of aluminum and the contact/via holes are filled with tungsten plugs. The dielectric layers are silicon dioxide and the passivation layer includes silicon dioxide and silicon nitride. The etched holes are filled with silicon dioxide. In order to fabricate a flat plane surface, chemical mechanical polishing (CMP) is employed after each deposition layer is completed.

A notable device releasing issue is that the passivation window of the MEMS structure must be opened in advance of the post-process. The self-designed post-CMOS process is applied to reserve a bulk silicon mass for reducing micromirror deformation and release the suspended structures. The post-process includes one grinding process, one backside alignment lithography process, a 2-step backside inductively coupled plasma (ICP) etching process, and an HF vapor releasing process. Fig. 6 illustrates the post-process flow. The post-process is implemented using the following steps:

a) The post-process starts with the device fabricated after the CMOS foundry process with the passivation window already open as shown in Fig. 6(a). The open-window step is implemented during the foundry process.
b) A backside grinding process is utilized to grind down the silicon substrate thickness, reserving only 100 μm for economic considerations to save expense and time for the ICP etching process, as shown in Fig. 6(b).
c) After that, a backside lithography process is applied to define the proof mass area, and then PI tape is used to protect the peripheral area of the chip from ICP etching, as illustrated in Fig. 6(c).
d) Then the first anisotropic ICP etching step is conducted to etch the silicon substrate for proof mass reservation, in which PR and PI tape are used as the hard mask, as illustrated in Fig. 6(d).

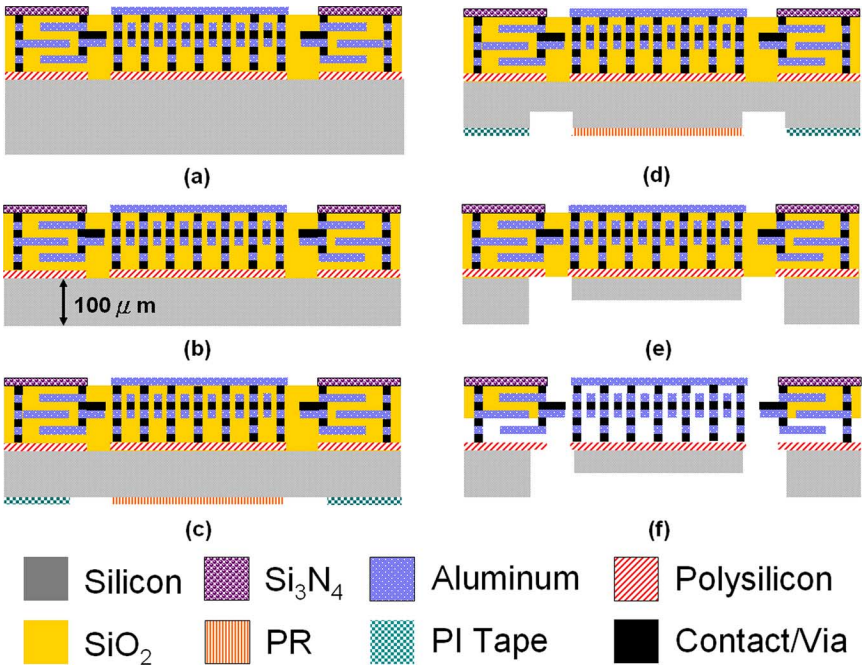

Fig. 6. Post-CMOS fabrication process flow: (a) completion of the CMOS process; (b) reserving only 100 μm of silicon by grinding process; (c) defining proof mass area by backside lithography process; (d) first backside ICP etching step; (e) second backside ICP etching step; (f) HF vapor etching process to release suspended microstructures.

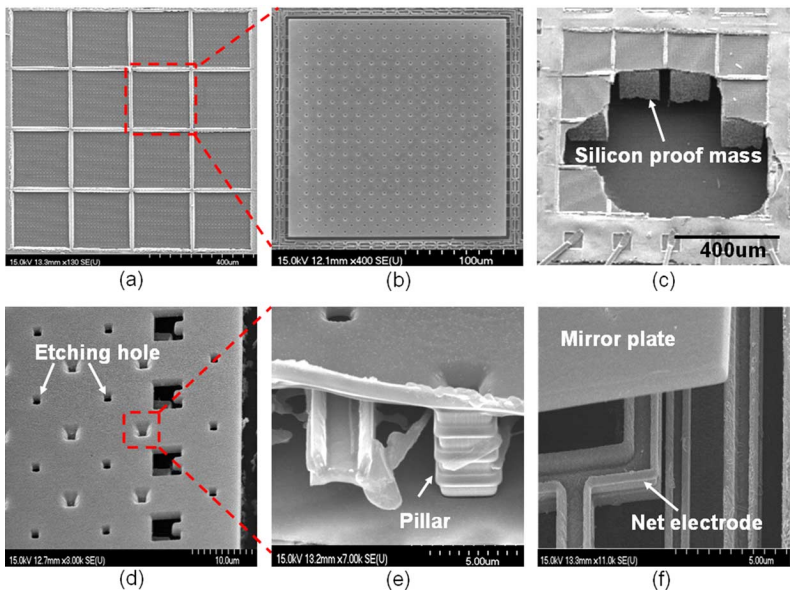

Fig. 7. SEM pictures of the proposed micromirror phase shifter: (a) 4 × 4 mirror array; (b) an individual mirror pixel; (c) the silicon proof mass under the mirror plate; (d) the etching holes and hollows on the mirror; (e) the pillar structure; (f) the net electrode under the mirror plate.

e) Fig. 6(e) depicts the second step of the ICP etching process. In this step, PR is removed by PR stripper but the PI tape is reserved for the second mask instead of PR. Although the ICP process etches the PI tape, the tape extends the etching time to form the proof mass. In this etching step, silicon dioxide is utilized as the etching stop layer since the etching selectivity of silicon dioxide is significantly higher than that of PI tape.

f) To prevent the micromirror from sticking problem during wet etching release process, as shown in Fig. 6(f), an HF vapor etching process is used to release the micromirror structure in the final step. The dry etching process is performed by heating 49% HF liquid to produce HF vapor which is utilized to etch SiO_2. Since the device was fabricated by CMOS process, the compositions of the four metal layers are not pure Al, but the alloy of Al, Cu, and Si. The etching selectivity between SiO_2 and Al is very large that we can use HF vapor process to release our device [31]. At first, the device chip is placed in a sealed limpid space. In the space there is a vessel with 49% HF liquid. A tungsten lamp is placed upon the sealed limpid space with 10 cm height. When the HF liquid is heated

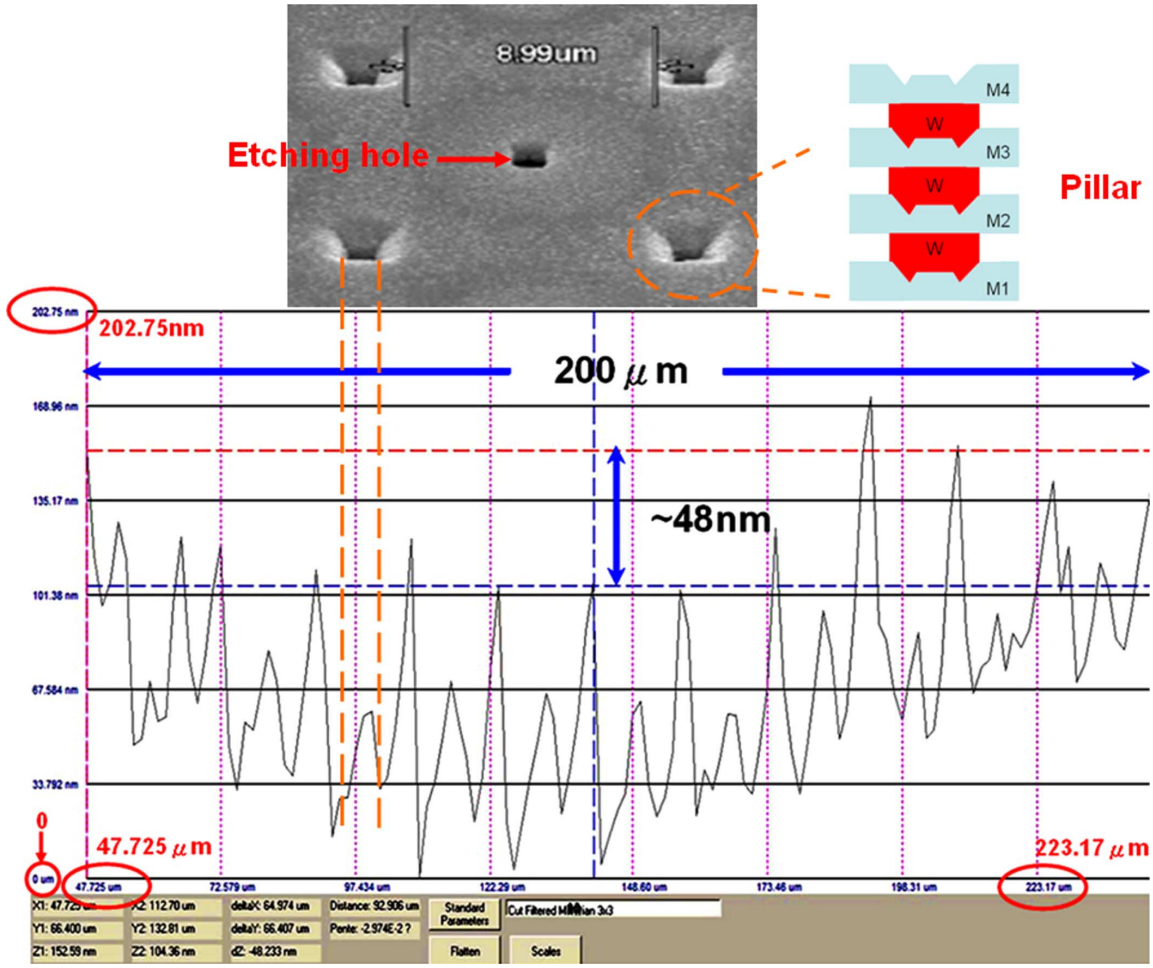

Fig. 8. X-direction surface flatness of the micromirror device.

to 45°C by tungsten lamp irradiation, the sealed space is full of HF vapor. Finally, the silicon dioxide is etched by HF vapor and device structures are released. The experimental release time in this case is about 12 minutes.

Fig. 7 displays SEM images of the device fabricated using the CMOS process and post-CMOS processes. Fig. 7(a) shows the 4×4 mirror array combined phase shifter device and an individual pixel is shown in Fig. 7(b). The proof mass design is clearly displayed in Fig. 7(c) and it can effectively reduce the residual stress from the CMOS surface process. The etching holes, pillars and net electrode of the micromirror are shown in Fig. 7(d) to (f), respectively. The hollows in Fig. 7(d) are due to violations of the CMOS design rule.

V. Experimental Results

A. Flatness of the Micromirror

Micromirror phase shifter flatness is a very important decisive factor for diffraction quality and its applications. In the surface MEMS fabrication process, the bending phenomenon of mirror is common seen due to the residual stress. In this experiment, the micromirror surface is scanned at a 200 μm range in the X- and Y-directions, respectively. Fig. 8 shows the X-direction roughness scanned at a 200 μm distance from one side, passing through the mirror center to the other side. The regular cavity profiles shown in Fig. 8 are due to the pillar structures which are formed by stacks of four metal layers and three via structures. The measurement shows that only slight deformation occurs in the edge of micromirror because there are no pillar connections in the edge of micromirror. Excepting the pillar cavities, the mirror deformation is only about 48 nm and within $\lambda/10$ (51 nm). Deformation induced by the residual stress from the CMOS process is effectively decreased due to reserving proper silicon proof mass. A similar scanning result is obtained for the Y-direction. Thus, mirror peak-to-valley deformation totally fits design specifications. Note that after completed the released process, each mirror pixel is positioned at different elevation due to the different stiffness of the suspension beams. Considering with whole flatness of the micromirror array, each micromirror is designed to be driven by individual driving voltage so that we can balance each mirror elevation to achieve flatness purpose by individual offset voltage.

B. Static Characteristic Measurement

Fig. 9 shows the experiment setup for static characteristic measurement. In this experiment, the WYKO interferometer is used again to measure the vertical distance moved by corresponding driving voltage. A DC bias voltage provided by the power amplifier is utilized to actuate the micromirror. Fig. 10 compares simulation and measurement results of a single mirror for vertical displacement versus driving voltage.

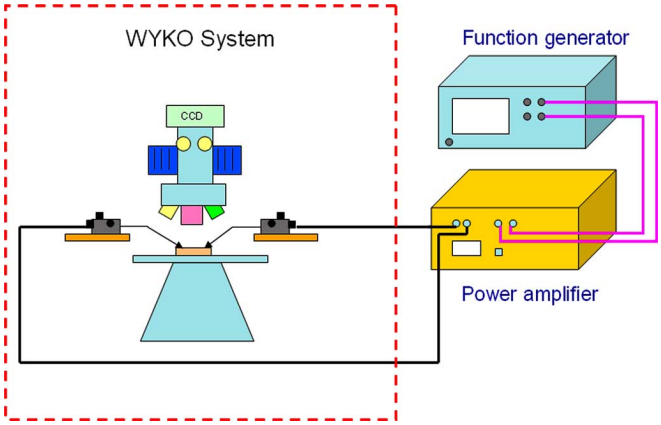

Fig. 9. The experimental diagram of static characteristic measurement.

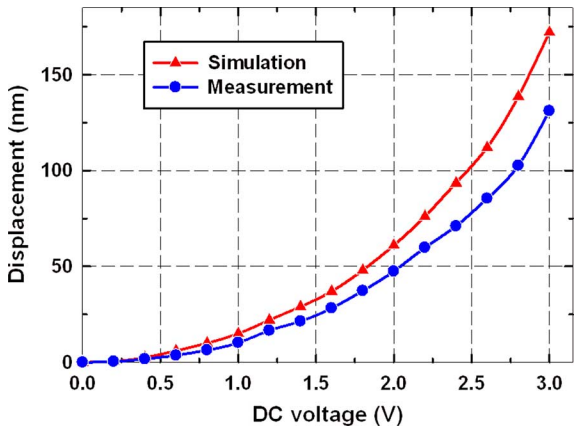

Fig. 10. The static characteristic of the micromirror.

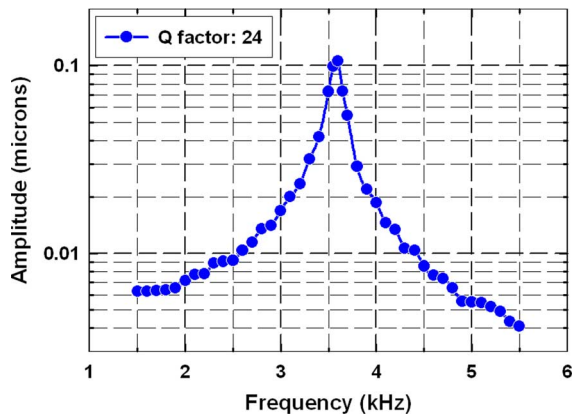

Fig. 11. The frequency response of the micromirror.

The experimental results demonstrate that vertical motion of the micromirror can achieve a 128 nm displacement ($\lambda/4$ of the 514 nm light source) when a 3 V driving voltage is applied to the actuator. The vertical displacement of the micromirror of 0~128 μm is obtained by increasing the driving voltage from 0 to 3 V. Thus, the requirement of $\lambda/4$ displacement can be easily reached with less than 5 V driving voltage. The low driving voltage characteristic gives the device potential to integrate with a CMOS circuit on one chip.

C. Frequency Response Measurement

Fig. 11 shows the frequency response of the micromirror device measured using a MEMS Motion Analyzer (MMA). The micromirror is biased by a sinusoidal wave with voltage amplitude of 0.5 V, and the frequency ranges between 1.5 and 5.5 kHz. The first resonant frequency mode is measured at 3.60 kHz, which closely matches the calculation (3.94 kHz) and simulation (4.14 kHz) results. The error is due to variations in the CMOS fabrication process and post-process. The quality factor of the mirrors is calculated at 24 in air.

VI. Conclusions

This study presents a 4×4 electrostatic phase shifter micromirror array fabricated by TSMC 0.35 μm 2p4m CMOS process and the self-designed post-CMOS process. By means of the special net electrode design under the mirror, the micromirror array has a fill factor of more than 90%. Individual mirror pixels are 200 μm$\times$ 200 μm. Mirror deformation resulting from residual stress of the CMOS process is effectively decreased via a proof mass reservation design. To prevent the device from the side sticking phenomenon in a wet etching release process, this device is released by HF vapor etching technique. The design, modeling, simulation and measurements are presented. Preliminary measurement results demonstrate that the micromirror can achieve a 128 nm ($\lambda/4$) vertical displacement with a driving voltage of 3 V and the resonant frequency is 3.6 kHz. With the advantages of a high fill factor and low driving voltage, the phase-shifting micromirror array has potential as a spatial light modulator in holographic data storage systems in the future.

Acknowledgements

The authors would like to thank the Taiwan National Chip Implementation Center (CIC) for technical supports.

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