Temperature-Dependent RF Small-Signal and Noise Characteristics of SOI Dynamic Threshold Voltage MOSFETs

Sheng-Chun Wang, Pin Su, *Member, IEEE*, Kun-Ming Chen, Kuo-Hsiang Liao, Bo-Yuan Chen, Sheng-Yi Huang, Cheng-Chou Hung, and Guo-Wei Huang, *Member, IEEE*

***Abstract*—In this paper, temperature-dependent RF small-signal and noise characteristics of silicon-on-insulator (SOI) dynamic threshold voltage (DT) MOSFETs are experimentally examined. In the low-voltage regime, both the cutoff and maximum oscillation frequencies (f_t and $f_{\max}$) tend to increase with temperature. In addition, the inherent body-related parasitics and the series resistance have much more impact on $f_{\max}$ than f_t. Besides, we found that the noise stemmed from the body resistance (R_b) would contribute to the output noise current, and degrade the minimum noise figure ($\mathrm{NF_{min}}$). Our study may provide insights for RF circuit design using advanced SOI DT MOSFETs.**

***Index Terms*—Body resistance, dynamic threshold voltage (DT) MOSFETs, noise, RF, silicon-on-insulator (SOI), small signal, temperature dependence.**

I. Introduction

DUE TO its larger current driving ability with low leakage current, the dynamic threshold voltage (DT) MOSFET is attractive for low-power applications [1]. Hence, the dc characteristics and modeling of the DT MOSFET have been widely studied since its introduction [2]–[4]. Moreover, the temperature effect on its dc characteristic has also been well investigated [4].

Several optimized silicon-on-insulator (SOI)- or bulk-based DT MOS fabrication processes with improved performance have been demonstrated [5], [6], and its ability of RF applications with high cutoff frequency (f_t) and maximum oscillation frequency ($f_{\max}$) has been reported as well [7]–[9]. However, the temperature effect on the RF characteristics of DT MOSFETs is rarely known.

Manuscript received March 02, 2010; revised April 06, 2010; accepted June 08, 2010. Date of publication August 03, 2010; date of current version September 10, 2010. This work was supported in part by the National Science Council of Taiwan.

S.-C. Wang and G.-W. Huang are with the National Nano Device Laboratories (NDL), Hsinchu 300, Taiwan, and also with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: scwang@ndl.org.tw; gwhuang@ndl.org.tw).

P. Su is with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: pinsu@mail.nctu.edu.tw).

K.-M. Chen, K.-H. Liao, and B.-Y. Chen are with the National Nano Device Laboratories (NDL), Hsinchu 300, Taiwan (e-mail: kmchen@ndl.org.tw; khliao@ndl.org.tw; bychen@ndl.org.tw).

S.-Y. Huang and C.-C. Hung are with the United Microelectronics Corporation (UMC), Hsinchu 300, Taiwan (e-mail: Samny_Huang@umc.com; Bigchoug_Hung@umc.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2010.2057175

To avoid a large leakage current flowing through the source–body junction, a DT MOSFET is usually biased in the low gate overdrive (V_{GT}) region. Therefore, it is crucial to examine the RF small-signal and noise characteristics under this regime.

This paper is an experimental investigation on the RF small-signal and noise characteristics of SOI DT MOSFETs and is organized as follows. The measurement environment and device structures/geometries are described in Section II. In Section III, the temperarue effect of body-related parasitics and series resistances on f_t and $f_{\max}$ will then be investigated. In Section IV, the RF noise behavior and its temperature dependence will be discussed for the first time. The temperature dependences of the equivalent thermal resistance and minimum noise figure will be examined as well. Finally, conclusions will be drawn in Section V.

II. Devices and Experiments

The RF SOI DT MOSFETs used in this work were fabricated using UMC 65-nm SOI technology. These RF devices were laid out in the multifinger (eight fingers) and multigroup (16 groups) structure with 1-μm channel width per finger.

On-wafer two-port common-source high-frequency S and noise parameters were measured using an ATN NP5B noise measurement system with Cascade microwave probes. Besides, to eliminate the inevitable parasitic accompanied with the probing pads, the S-parameters of the devices' corresponding dummy were measured and then used to perform the S and noise parameters' de-embedding procedure.

Fig. 1 shows the temperature dependences of threshold voltage (V_T) extracted by the constant current ($I_{\mathrm{th}} \equiv 50$ nA $\times$ W/L) method. Due to the negative temperature coefficient of the device's Fermi potential [4], V_T exhibits the negative temperature dependence for each channel length device.

The equivalent circuit for both RF small-signal and noise behaviors is depicted in Fig. 2. The inherent body-related parasitics include the source- and drain-side junction capacitances ($C_{j,sb}$ and $C_{j,db}$, respectively), the junction resistance ($R_{j,sb}$), the body resistace (R_b), and the body-transconductance (g_{mb}). The series resistances R_s, R_d, and R_g were determined using the proposed zero method [10], and the other parameters along with the channel noise current $\overline{i_d}$ can be extracted by the extraction method presented in [11]. Note that to keep the device

0018-9480/$26.00 © 2010 IEEE

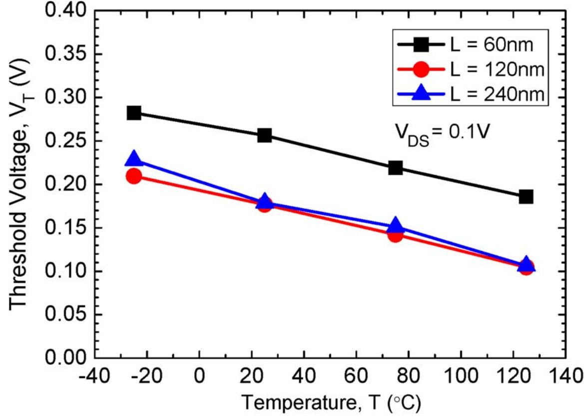


Fig. 1. Temperature dependence of the threshold voltage for SOI DT MOSFETs.

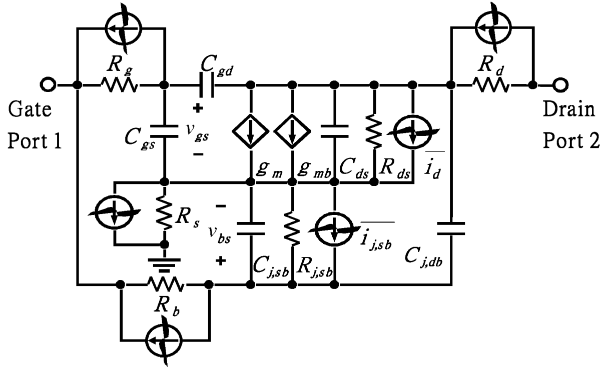
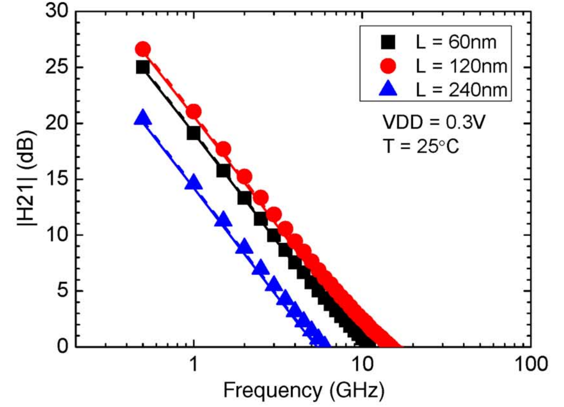


Fig. 2. RF small-signal and noise equivalent circuit for the SOI DT MOSFET.



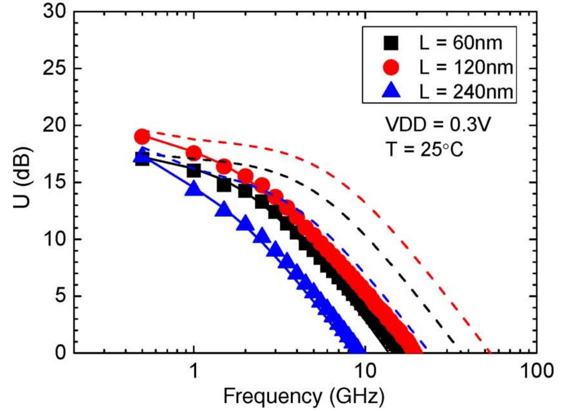


Fig. 3. (a) Short-circuit current gain $|H_{21}|$ and (b) unilateral power gain U with and without considering the series resistance effect (symbols: measured data; solid and dash lines: modeled results with and without considering the series resistance effect, respectively).

operating in the saturation region, we let $V_{\rm GS}(=V_{\rm BS})=V_{\rm DS}\equiv VDD$ in our experiments.

III. RF Small-Signal Characterization

The cutoff frequency (f_t) and maximum oscillation frequency $(f_{\max})$ are two common figures of merit used to characterize the RF performance of a device. Based on the equivalent circuit shown in Fig. 2 and neglecting the series resistances R_s, R_d, and R_g, the "intrinsic" f_t and $f_{\max}$ for the DT MOSFET biased in the low VDD regime can be approximately expressed as the following [12]:

$$f_t \approx \frac{g_m}{2\pi\sqrt{C_{\rm gs}(C_{\rm gs}+2C_{\rm gd})}} \approx \frac{g_m}{2\pi C_{\rm gs}} \tag{1}$$

$$f_{\max} \approx f_{\max 0}\left\{1+g_{mb}R_{\rm ds}\frac{C_{j,db}}{C_j}\right\}^{-0.5} \equiv f_{\max 0}\cdot\alpha_{\rm DT}. \tag{2}$$

In (1) and (2), $C_j=C_{j,sb}+C_{j,db}$,

$$\alpha_{\rm DT}=\left\{1+g_{mb}R_{\rm ds}\frac{C_{j,db}}{C_j}\right\}^{-0.5} \tag{3}$$

and

$$f_{\max 0}\approx\frac{f_t}{2}\sqrt{\frac{R_{\rm ds}}{R_i}} \tag{4}$$

where R_i is the input resistance, which can be extracted by optimizing $\mathrm{Re}(Z_{11})$.

The approximation in (1) and (2) holds in the low VDD regime, where $g_m/g_{mb}\gg 1$, $R_b/R_i\gg 1$, $g_{mb}R_b\gg C_{j,db}/C_j$, and $\omega R_b C_j\gg 1$ around $f_{\max}$.

Equation (1) implies that the inherent body-related parasitics of the DT MOSFET would have little influence on f_t. In the low VDD regime, since g_m tends to increase with temperature [4], [13], f_t would have a positive temperature coefficient. On the other hand, due to the less temperature-dependent behavior of $\sqrt{R_{\rm ds}/R_i}$ and the degradation factor $\alpha_{\rm DT}$, $f_{\max}$ tends to have the same temperature dependence as f_t [12]. That is, in the low VDD regime, both intrinsic $f_{\max}$ and f_t would increase with temperature.

To investigate the overall performance, however, the impact of the series resistance effect on $f_{\max}$ and f_t should be examined. Fig. 3 shows that the series resistance has much more significant effect on the unilateral power gain U (involved in the determination of $f_{\max}$) than the short-circuit current gain $|H_{21}|$ (involved in the determination of f_t) at $VDD=0.3$ V. Compared to the series resistances, the much larger input and output impedance in the low VDD regime would dominate $|H_{21}|$, and hence, f_t. The little series resistance effect on f_t can be also deduced from Fig. 4(a) and (b), where f_t has nearly the same temperature coefficient as g_m for each channel length device.

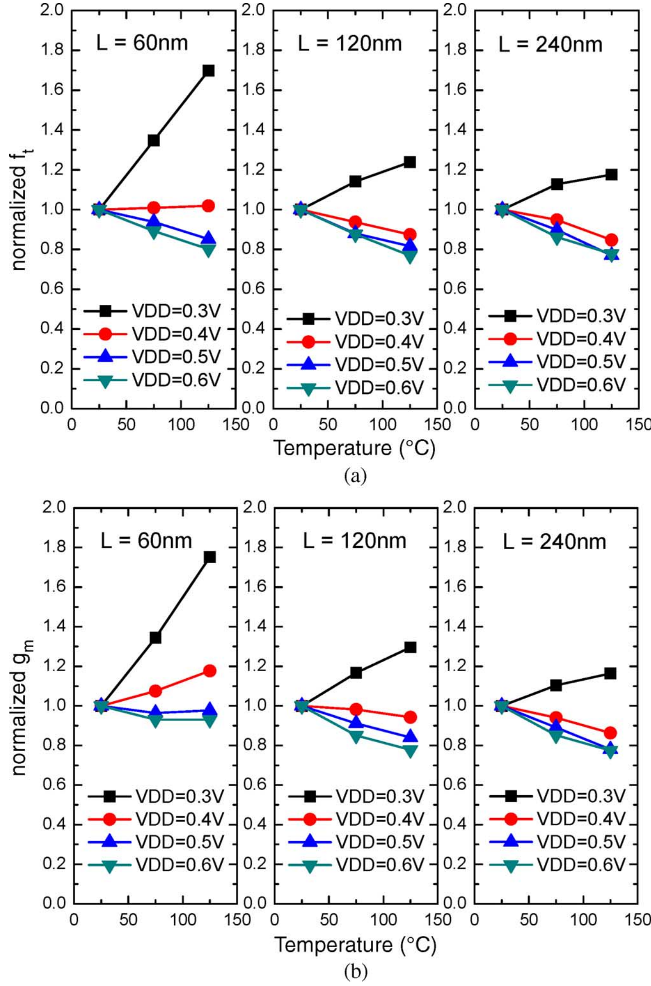
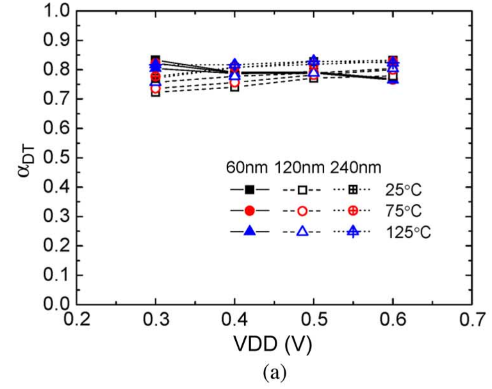


Fig. 4. Temperature dependences for: (a) f_t and (b) g_m. (Data normalized with respect to their corresponding values at $T = 25$ °C.)



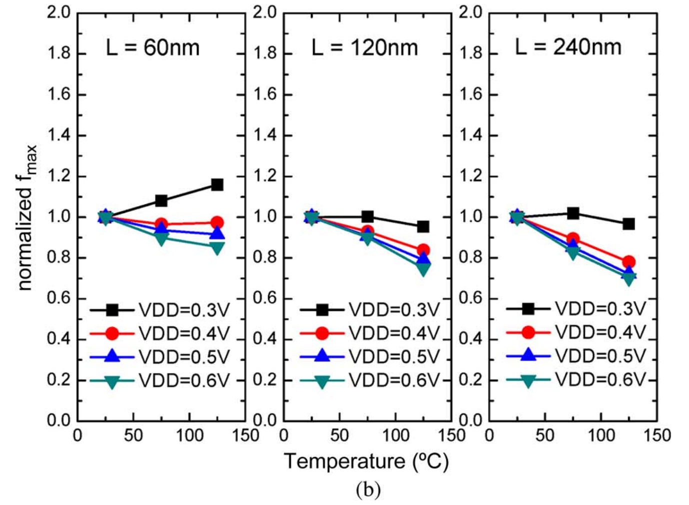


Fig. 5. Temperature dependences for: (a) α_{DT} and (b) $f_{\max}$. (Data normalized with respect to their corresponding values at $T = 25$ °C.)

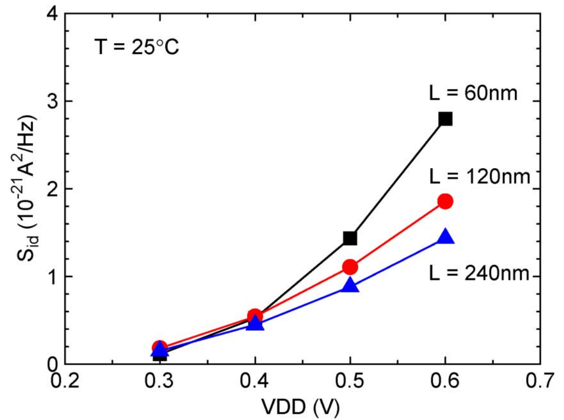


Fig. 6. Channel noise versus VDD.

This coincides with the implication in (1), which has assumed the series resistance is insignificant.

The input and output impedance matching for the maximum available power gain, and hence, $f_{\max}$, however, can be greatly influenced by the series resistances. Moreover, since the degradation factor α_{DT} is found to be nearly temperature independent for each channel length device, as shown in Fig. 5(a), the degraded temperature dependence of $f_{\max}$, shown in Fig. 5(b), would be mostly caused by the series resistance effect. That is, the larger resistances at higher temperatures would severely degrade $f_{\max}$.

IV. RF Noise Characterization

A. *Channel Noise and Equivalent Thermal Resistance*

The extracted power spectral density for the channel noise current $\overline{i_d}$ (denoted as S_{id}) is shown in Fig. 6, and is usually expressed as follows [14]:

$$S_{id} = 4k_B T \gamma g_{d0} \tag{5}$$

where $k_B \approx 1.38 \times 10^{-23}$ J/K is the Boltzmann constant, T is the ambient temperature in kelvin, g_{d0} is the channel conductance at zero drain–source voltage, and γ is the noise factor. Besides, [15] has shown that γ has a weak temperature dependence, and the temperature dependence of S_{id} is dominated by that of g_{d0} and T.

Fig. 7(a) and (b), respectively, shows the temperature dependences of S_{id} and g_{d0}. In the low VDD regime, since g_{d0} tends to increase with temperature [12], S_{id} would increase accordingly as predicted by (5). Note that (5) was originally derived for the device operating in the strong inversion region. However,

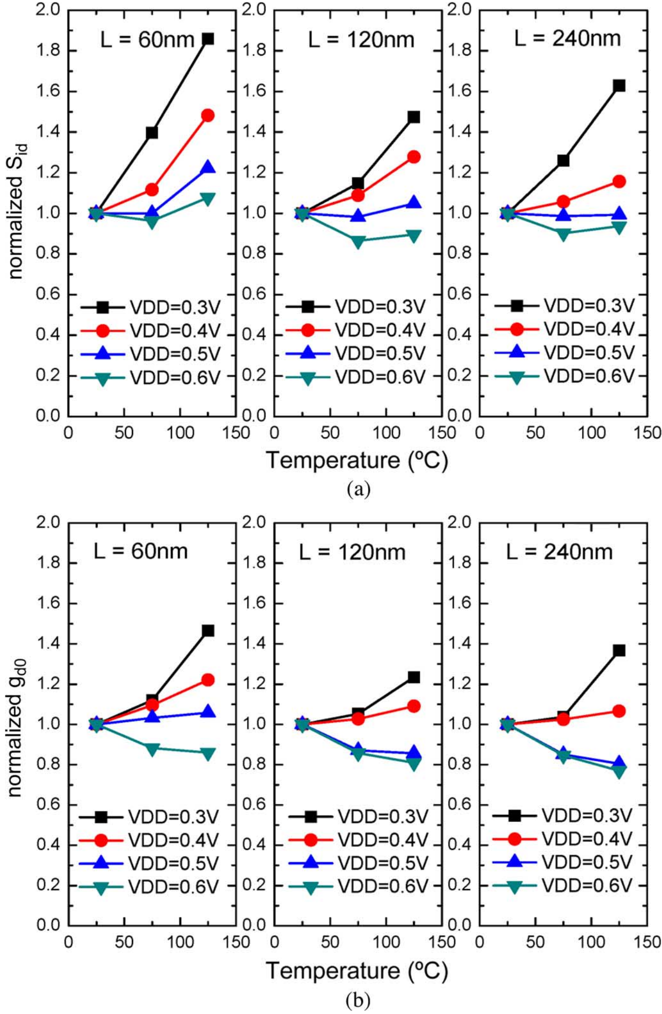


Fig. 7. Temperature dependences for: (a) S_{id} and (b) g_{d0}. (Data normalized with respect to their corresponding values at $T = 25$ °C.)

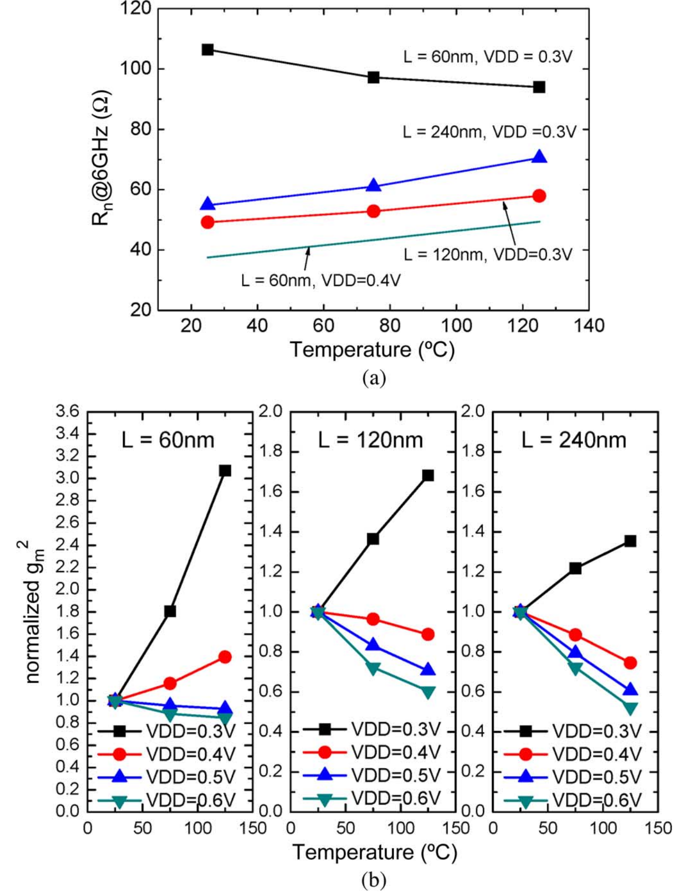


Fig. 8. Temperature dependences for: (a) R_n and (b) g_m^2. (Data normalized with respect to their corresponding values at $T = 25$ °C.)

in our experiments, the consistent prediction results for the temperature dependence of S_{id} shows that it seems to remain valid even for the medium or weak inversion applications.

The channel noise has a significant effect on the equivalent thermal resistance R_n for conventioanl MOSFETs. In fact, by neglecting the body trans-conductance, R_n for DT MOSFETs would be approximately the same as that for conventional MOSFETs as expressed in the following:

$$R_n \approx \frac{S_{id}}{4k_B T_0 g_m^2} + \frac{T}{T_0} R_g \quad (6)$$

where $T_0 = 290$ K is the reference temperature. Note that (6) indicates that in the low VDD regime, the body-related parasitics would have little influence on R_n.

Fig. 8(a) shows R_n versus temperature curves for each channel length device. Since V_T for $L = 60$ nm device is about 0.1 V higher than those for $L = 120$ nm and $L = 240$ nm devices in the whole temperature range (see Fig. 1), we first consider $VDD = 0.3$ V for $L = 120$ nm and $L = 240$ nm devices, and $VDD = 0.4$ V for the $L = 60$ nm device to keep approximately the same gate overdrive voltage. In this case, one can compare the temperature dependence for S_{id} in Fig. 7(a) and that for g_m^2 in Fig. 8(b). Since S_{id} tends to have the similar temperature coefficient as g_m^2, according to (6), R_n tends to increase with temperature mainly due to the increase of R_g and T.

For an $L = 60$ nm device operating at weaker bias condition, i.e., $VDD = 0.3$ V; however, g_m^2 tends to more deeply increase with increasing temperature than S_{id}. This could compete with or even overwhelm the contribution from "hot" R_g. Therefore, R_n tends to decrease with increasing temperature. This also shows the existence of the zero temperature coefficient for R_n, which occurs between $VDD = 0.3$ V and $VDD = 0.4$ V for the $L = 60$ nm device.

B. Output Noise Current and Minimum Noise Figure

Unlike R_n, the minimum noise figure $\mathrm{NF}_{\min}$ may be strongly influenced by R_b. Although the analytical expression for $\mathrm{NF}_{\min}$ is not easily derived, the noise contribution arising from R_b to the output noise current flowing into the drain terminal can be analyzed and regarded as an important factor determining $\mathrm{NF}_{\min}$.

The noise power spectral density arising from R_b (denoted as S_{iRb}) is considered as thermal noise, and can be expressed as follows:

$$S_{iRb} = 4k_B T / R_b. \quad (7)$$

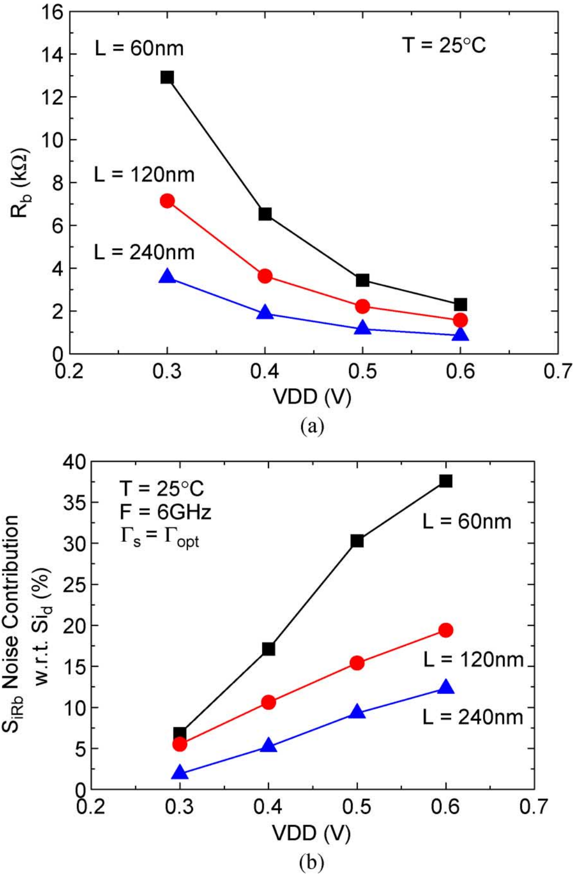


Fig. 9. (a) Extracted body resistance as a function of VDD. (b) Noise contribution from the body noise S_{iRb} to the output noise current with respect to that from the channel noise.

The extracted R_b values and their corresponding S_{iRb} contribution with respect to S_{id} counterpart to the output noise current and are shown in Fig. 9(a) and (b), respectively. We found that larger R_b in the low VDD regime would have less S_{iRb} noise contribution for each length device. This figure also shows that the shorter device with larger R_b would have more S_{iRb} contribution. It is worth noting that the smaller body cross-sectional area seen in the direction perpendicular to the channel current flow can account for the larger R_b present in the shorter device.

Through the sensitivity analysis of the variation of R_b to its noise contribution, as shown in Fig. 10, we can see that its noise contribution could be reduced with increasing R_b. In fact, the noise equivalent circuit for DT MOSFETs would be equivalent to that for conventional MOSFETs when R_b approaches infinity and can be removed in the equivalent circuit. Therefore, the larger R_b would play an insignificant role in determining $\mathrm{NF_{min}}$.

The minimum noise figure $\mathrm{NF_{min}}$ versus VDD is shown in Fig. 11. $\mathrm{NF_{min}}$ is sharply increased towards the weak inversion region, and this trend is consistent with that for the conventional bulk MOSFET [16]. Moreover, our experimental results show that $\mathrm{NF_{min}}$ has less temperature dependence in the low VDD regime. As shown in Fig. 10, in the low VDD regime, since the noise contribution of S_{iRb} to the output noise current for each temperature is not significant, R_b would have little effect on the temperature dependence of $\mathrm{NF_{min}}$.

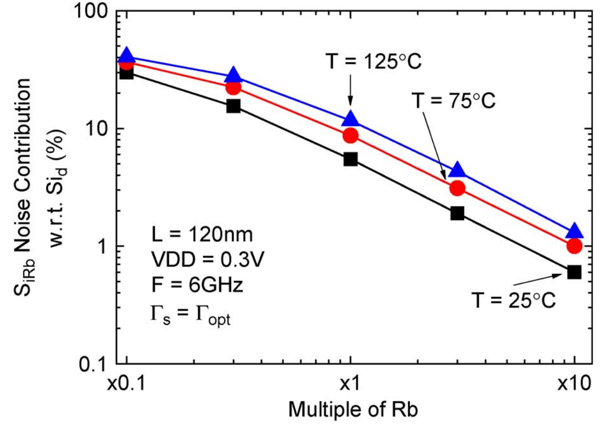


Fig. 10. Sensitivity analysis of the body resistance with respect to its noise contribution.

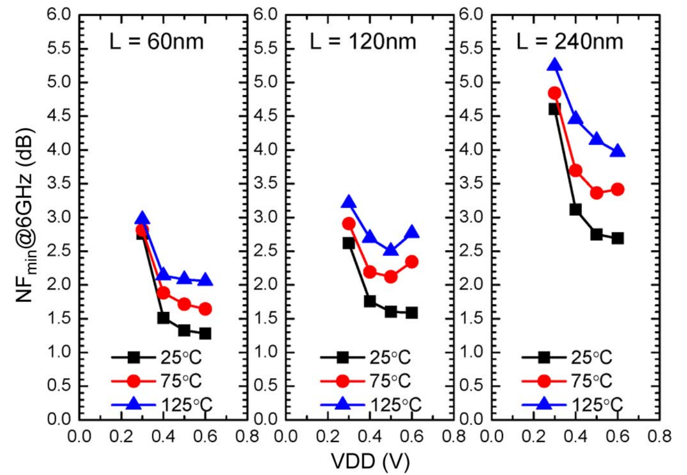


Fig. 11. $\mathrm{NF_{min}}$ as a function of VDD at different temperatures for various channel length devices. (Data normalized with respect to their corresponding values at $T = 25$ °C.)

V. Conclusions

We have investigated the temperature dependences of RF small-signal and noise behaviors for the DT MOSFET. In the low VDD regime, since g_m tends to increase with temperature, f_t would have a positive temperature coefficient. On the other hand, due to the less temperature-dependent behavior of α_{DT} and $\sqrt{R_{\mathrm{ds}}/R_i}$, $f_{\max}$ is found to increase with temperature as well. Moreover, the body-related parasitics and the series resistances are found to have more impact on $f_{\max}$ than f_t.

In the low VDD regime, the channel noise S_{id} has a positive temperature coefficient due to larger g_{d0} at higher temperature. In addition, compared to S_{id}, the much higher g_m^2 toward the weaker inversion region can cause R_n to have a negative temperature coefficient. Finally, it shows that, in the low VDD regime, the large R_b would have little impact on the temperature dependence of $\mathrm{NF_{min}}$.

Acknowledgment

The authors would like to thank the United Microelectronics Corporation (UMC), Hsinchu, Taiwan, for providing the devices used in this study.

REFERENCES

[1] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko, and C. Hu, "Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI," *IEEE Trans. Electron Devices*, vol. 44, no. 3, pp. 414–422, Mar. 1997.

[2] S. S. Rofail and K. S. Yeo, "Experimentally-based analytical model of deep submicron LDD MOSFETs in a Bi-MOS hybrid-mode environment," *IEEE Trans. Electron Devices*, vol. 44, no. 9, pp. 1473–1482, Sep. 1997.

[3] J. B. Kuo, K. H. Yuan, and S. C. Lin, "Compact threshold-voltage model for short-channel partially-depleted (PD) SOI dynamic-threshold MOS (DTMOS) devices," *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 190–196, Jan. 2002.

[4] J.-K. Lee, N.-J. Choi, C.-G. Yu, J.-P. Colinge, and J.-T. Park, "Temperature dependence of DTMOS transistor characteristics," *Solid State Electron.*, vol. 48, pp. 183–187, 2004.

[5] C. Wann, F. Assaderaghi, R. Dennard, C. Hu, G. Shahidi, and Y. Taur, "Channel profile optimization and device design for low-power high-performance dynamic threshold MOSFET," in *Int. Electron. Device Meeting Tech. Dig.*, Dec. 1996, pp. 113–116.

[6] A. Shibata, T. Matsuoka, S. Kakimoto, H. Kotaki, M. Nakono, K. Adachi, K. Ohta, and N. Hashizume, "Ultra low power supply voltage (0.3 V) operation with extreme high speed using bulk dynamic threshold voltage MOSFET (B-DTMOS) with advanced fast-signal-transmission shallow well," in *Proc. VLSI Technol. Tech. Symp. Dig.*, 1998, pp. 76–77.

[7] Y. Momiyama, T. Hirose, H. Kurata, K. Goto, Y. Watanabe, and T. Sugii, "A 140 GHz f and 60 GHz f DTMOS integrated with high-performance SOI logic technology," in *Int. Electron. Device Meeting Tech. Dig.*, 2000, pp. 451–454.

[8] T. Hirose, Y. Momiyama, M. Kosuhi, H. Kano, Y. Watanabe, and T. Sugii, "A 185 GHz $f\max$ SOI DTMOS with a new metallic overlay-gate for low-power RF applications," in *Int. Electron. Device Meeting Tech. Dig.*, 2001, pp. 33.5.1–33.5.3.

[9] C.-Y. Chang, J.-G. Su, H.-M. Hsu, S.-C. Wong, T.-Y. Huang, and Y.-C. Sun, "Investigation of bulk dynamic threshold-voltage MOSFET with 65 GHz 'nomal mode' ft and 220 GHz 'over-drive mode' ft for RF applications," in *VLSI Technol. Tech. Symp. Dig.*, 2001, pp. 89–90.

[10] S.-C. Wang, P. Su, K.-M. Chen, C.-T. Lin, V. Liang, and G.-W. Huang, "On the RF extrinsic resistance extraction for partially-depleted SOI MOSFETs," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 5, pp. 364–366, May 2007.

[11] S.-C. Wang, P. Su, K.-M. Chen, S.-Y. Huang, C.-C. Hung, V. Liang, C.-Y. Tzeng, and G.-W. Huang, "RF small-signal and noise modeling for SOI dynamic threshold voltage MOSFETs," in *Int. Solid-State Devices Mater. Conf.* , Sep. 2008, pp. 414–415.

[12] S.-C. Wang, P. Su, K.-M. Chen, S.-Y. Huang, C.-C. Hung, and G.-W. Huang, "Temperature dependences of RF small-signal characteristics for the SOI dynamic threshold voltage MOSFET," in *Proc. 4th Eur. Micro. Integr. Circuits Conf.*, Sep. 2009, pp. 69–72.

[13] A. A. Osman and M. A. Osman, "Investigation of high temperature effects on MOSFET transconductance (gm)," in *Proc. 4th Int. High-Temperature Electron. Conf.*, Albuquerque, NM, Jun. 1998, pp. 301–304.

[14] A. F. Tong, W. M. Lim, K. S. Yeo, C. B. Sia, and W. C. Zhou, "A scalable RFCMOS noise model," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 5, pp. 1009–1019, May 2009.

[15] S.-C. Wang, P. Su, K.-M. Chen, C.-T. Lin, V. Liang, and G.-W. Huang, "Temperature dependence of high frequency noise behaviors for RF MOSFETs," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 8, pp. 530–532, Aug. 2008.

[16] K.-H. To, Y.-B. Park, T. Rainer, W. Brown, and M. W. Huang, "High frequency noise characteristics of RF MOSFET's in subthreshold region," in *IEEE RF Integr. Circuits Symp. Dig.*, Jun. 2003, pp. 163–167.

Sheng-Chun Wang received the B.S. and M.S. degrees in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 1999 and 2001, respectively, and is currently working toward the Ph.D. degree at Chiao Tung University, Hsinchu, Taiwan.

In 2001, he joined the National Nano Device Laboratories, Hsinchu, Taiwan, as an Assistant Researche. His current research interests focus on the small-signal and noise characterization and modeling for RF CMOS devices.

Pin Su (S'98–M'02) received the B.S. and M.S. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1992 and 1994, respectively, and the Ph.D. degree in electrical engineering and computer sciences from the University of California at Berkeley, in 2002.

From 1997 to 2003, he conducted his doctoral and postdoctoral research in SOI devices at the University of California at Berkeley. He was also one of the major contributors to the unified BSIMSOI model, the first industrial standard SOI MOSFET model for circuit design. Since August 2003, he has been with the Department of Electronics Engineering, National Chiao Tung University, where he is currently an Associate Professor. He has authored or coauthored about 100 research papers in refereed journals and international conference proceedings. His research interests include silicon-based nanoelectronics, modeling and design for advanced CMOS devices, and device/circuit interactions in nano-CMOS.

Kun-Ming Chen received the M.S. degree and Ph.D. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1996 and 2000, respectively.

In 2000, he joined the National Nano Device Laboratories, Hsinchu, Taiwan, as an Associate Researcher, and in 2007, became a Researcher. He was engaged in research on microwave device processes and characterization.

Kuo-Hsiang Liao received the M.S. degree in electronic engineering from National Changhua University of Education, Taiwan, Taiwan, in 2005.

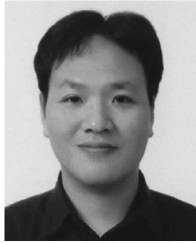
In 2005, he joined the National Nano Device Laboratories, Hsinchu, Taiwan, as an Assistant Researcher. He was engaged in research on RF device characterization and modeling.

Bo-Yuan Chen was born in Miaoli, Taiwan, in 1980. He received the M.S. degree in materials science and engineering from National Dong Hwa University, Hualien, Taiwan, in 2006.

In 2006, he joined the National Nano Device Laboratories, Hsinchu, Taiwan, as an Assistant Researcher. He was engaged in research on III–V compound semiconductors and RF device characterization.

Sheng-Yi Huang received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2001, and the M.S. and Ph.D. degrees in electronics engineering from National Chiao Tung University Hsinchu, Taiwan, in 2003 and 2007, respectively.

Since 2003, he has been with the Advanced Technology Development Division, United Microelectronics Corporation (UMC), Hsinchu, Taiwan, where he is involved with RF-related technologies. His current research focuses on advanced mixed-mode and RF CMOS design including device modeling, noise characterization, power behavior, and reliability studies.



Cheng-Choug Hung received the B.S. and M.S.E.E. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 1996 and 1999, respectively.

He is currently an RF Device Development Manager with the Advanced Technology Department, United Microelectronics Corporation (UMC), Hsinchu, Taiwan. His current responsibility/research focuses on RF CMOS technology characterization/delivery, including active and passive devices.

Guo-Wei Huang (S'94–M'97) was born in Taipei, Taiwan, in 1969. He received the B.S. degree and Ph.D. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1991 and 1997, respectively.

In 1997, he joined National Nano Device Laboratories (NDL), Hsinchu, Taiwan, where he is currently a Researcher and Manager of the High-Frequency Technology Division. Since August 2008, he has been an Adjunct Associate Professor with the Department of Electronics Engineering, National Chiao Tung University. His current research interests focus on characterization and modeling techniques of high-frequency devices, and characterization and verification of RF integrated circuits (RFICs)/monolithic microwave integrated circuits (MMICs).