Flip-Chip-Based Multichip Module for Low Phase-Noise V-Band Frequency Generation

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***Abstract*—This paper reports on a flip-chip (FC)-based multichip module (MCM) for low phase-noise (PN) V-band frequency generation. A high-performance $\times 8$ GaAs metamorphic high-electron mobility transistor monolithic microwave integrated circuit (MMIC) multiplier and a low PN 7-GHz GaAs InGaP heterojunction bipolar transistor (HBT) MMIC oscillator were used in the module. The microstrip MMICs were FC bonded to an Al_2O_3 carrier with patterns optimized for low-loss transitions. The FC-based module was experimentally characterized to have a PN of −88 dBc/Hz @ 100-kHz offset and −112 dBc/Hz @ 1-MHz offset with an output power of 11 dBm. For comparison, the MMICs were also FC bonded as individual chips and the performance was compared with the bare dies without FC bonding. It was verified that the FC bonding has no detrimental effect on the MMIC performance. The tests revealed that the FC module provided improved performance. To our best knowledge, this is the first FC-based module for millimeter-wave frequency generation. The module also presents one of the best PN reported for millimeter-wave frequency sources.**

***Index Terms*—Flip-chip (FC), frequency generation, interconnection, millimeter wave, monolithic microwave integrated circuit (MMIC), multichip module (MCM), multiplier, oscillator, phase noise (PN), V-band.**

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I. Introduction

Low phase-noise (PN) millimeter-wave frequency generation is a critical issue for future multigigabit/second wireless communication systems. The millimeter-wave frequency bands are capable of carrying high data rates thanks to the large amount of bandwidth available, e.g., the license-free industrial, scientific, and medical (ISM) bands around 60 GHz [1], or the recently allocated E-band (71–76 and 81–86 GHz) [2]. Further increased data rates may be reached with spectral efficient modulation formats, e.g., higher order quadrature amplitude modulation (QAM) [2]. However, the spectral-efficient modulation also puts stringent requirements on signal purity, i.e., low PN, which is challenging at millimeter-wave frequencies. One solution could be to operate the local oscillator (LO) at a lower frequency and use frequency multipliers [3] to reach the target frequency. It is believed that the overall PN will be lower with this approach as the Q factor of the resonant tank in the oscillator is reduced with increased frequency [4]. The use of frequency multipliers to create millimeter-wave signals also decrease or even totally diminish the need of frequency dividers for phase locking.

Although it is possible to design single-chip solutions where the oscillator and multiplier are integrated on the same monolithic microwave integrated circuit (MMIC), it may be advantageous to address a multichip module (MCM) [5]–[7] approach enabling higher flexibility in choice of technology for each chip. However, MCM packaging at millimeter-wave frequencies is also challenging, the interconnections between the MMIC chips and the MCM carrier may decay the assembly performance, e.g., conventional bond-wires give a significant contribution to the parasitic inductance, and thus, induce unwanted effects at millimeter-wave frequencies [8]. In this respect, flip-chip (FC) interconnection has been regarded as a promising packaging technology for cost-effective module assembly in millimeter-wave systems due to its shorter interconnect length, higher throughput, and smaller package size [9]–[16]. Furthermore, considering large-scale production with small chip ($<5 \times 5$ mm^2) and pad ($<1 \times 1$ mm^2) size and good wafer-bumping yield, the FC is cheaper than bond-wire [16]. For millimeter-wave applications, the regular chip and pad size is normally smaller than this range. For these reasons, the FC-based multichip module (FC-MCM) is considered as the most promising packaging scheme for millimeter-wave wireless applications.

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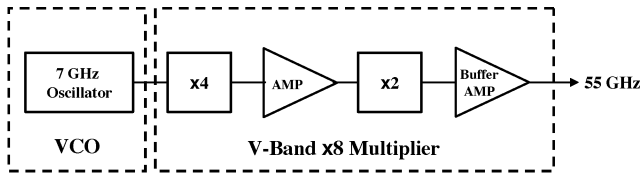

Fig. 1. Block diagram of the V-band frequency source realized in this study.

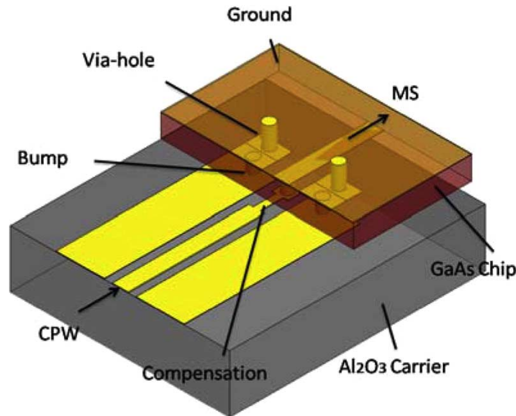

Fig. 2. Simulated FC interconnect structure (single transition).

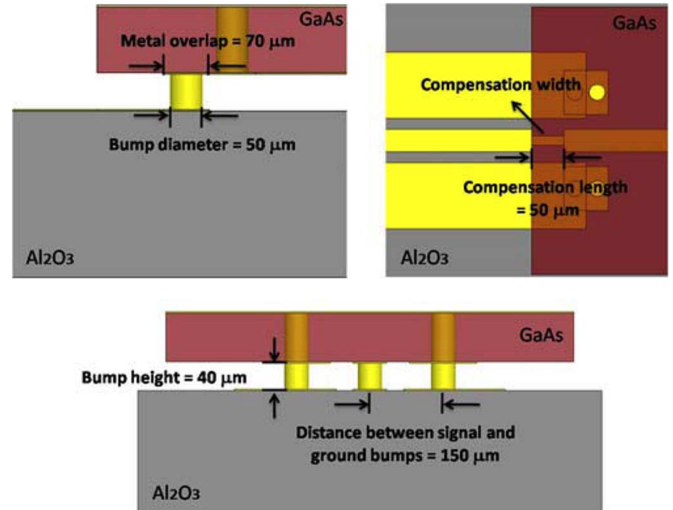

Fig. 3. Illustrations of the important parameters for the FC interconnect.

In this paper, we report on an FC-MCM for V-band frequency generation. Fig. 1 illustrates the block diagram of the V-band frequency source realized in this study. The module consists of the high-performance V-band $\times 8$ metamorphic high-electron mobility transistor (mHEMT) MMIC multiplier reported in [3] and the 7-GHz low PN cross-coupled InGaP HBT MMIC oscillator reported in [17]. This paper is organized as follows. In Section II, the optimum FC design by electromagnetic (EM) simulation will be presented and discussed. In Section III, the in-house process flow of FC assembly will be presented. Sections IV and V present the measurement setups and measurement results for the MMIC circuits, respectively. Finally, this work is concluded in Section VI.

II. Design and Optimization of the FC Transitions

In this work, the oscillator and $\times 8$ multiplier MMICs were designed with microstrip (MS) transmission lines as most of the commercial available MMICs. However, most of the reported FC studies have been made using coplanar waveguide (CPW) MMICs [9]–[14], which is considered to be more compatible with FC technology. Hence, the FC structure design for MS MMICs needs to be investigated. The design and optimization of the interconnect structure was carried out by using the simulation tool, Ansoft High Frequency Simulation Software (HFSS) 11 for the 3-D EM field analysis, which predicts a reliable S-parameter of the millimeter-wave interconnect structures [18]–[20]. Fig. 2 shows the simulated FC interconnect structure with the MS transmission line on the GaAs chip and CPW transmission line on the Al_2O_3 carrier.

The important parameters of the FC design such as bump diameter, bump height, metal pad overlap, and compensation have been discussed and investigated in [9], [11], and [12]. Among these parameters, the compensation, reducing the excess parasitic capacitance at the vertical bump transition by adding an inductive counterpart, is the most effective way to optimize the interconnect performances since extra process steps and fabrication cost are not needed [11]. Two approaches, one with staggered bumps and the other one employs a high impedance-line section, were proposed to reduce the return loss of the FC interconnect [9], [11]. The staggered-bumps approach needs an additional chip area and requires customized chip design. Therefore, the approach of employing a high-impedance line section before the bump transitions is more advantageous.

During the EM simulation, the bump dimensions and metal pad overlap were fixed by the fabrication process. The diameter of the bump was 50 μm, the bump height was 40 μm, and the metal pad overlap was 70 μm. The center-to-center distance between signal and ground bumps was 150 μm. The illustrations of these parameters are indicated in Fig. 3. Figs. 4 and 5 show the simulated return loss ($S11$) and insertion loss ($S21$), respectively, of the FC interconnect with different compensation widths. As can be seen, the thinner the high-impedance line compensation, the better the interconnect performance. From Fig. 4, the return loss was improved about 3 dB per transition at 60 GHz compared to the structure without compensation. Besides, the insertion loss was about 0.5 dB per transition at 60 GHz after optimization (Fig. 5). The final dimensions of the compensation line were 30 μm in width and 50 μm in length, which is acceptable for commercial low-cost film mask processes. Table I shows the parameters of the optimized FC design.

III. Fabrication of the FC-Based Modules

One of the advantages with MCMs compared to highly integrated single chips is the flexibility to adapt technology for the individual chip functions; in a single-chip solution, the technology is a tradeoff between the different chip functions. The V-band LO module reported in this work is assembled from a low-PN 7-GHz fixed-frequency cross-coupled oscillator designed and implemented in a GaAs InGaP HBT [17] process and a $\times 8$ GaAs mHEMT multiplier chain optimized for input frequency in the range of 6.5–8 GHz [3]. The InGaP HBT process

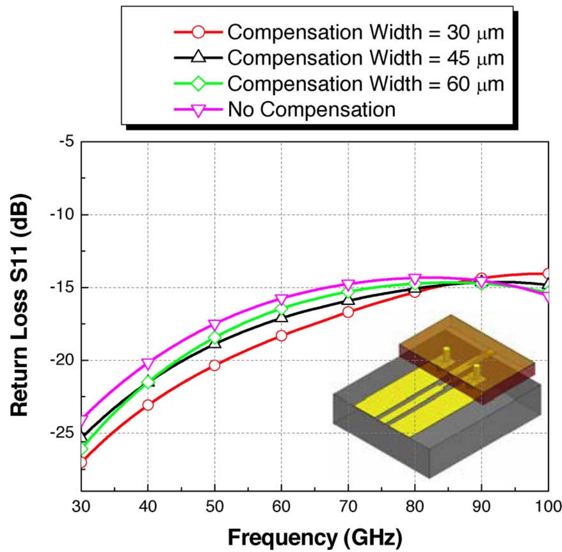

Fig. 4. Simulated return loss ($S11$) of the FC interconnect (single transition) with different compensation widths.

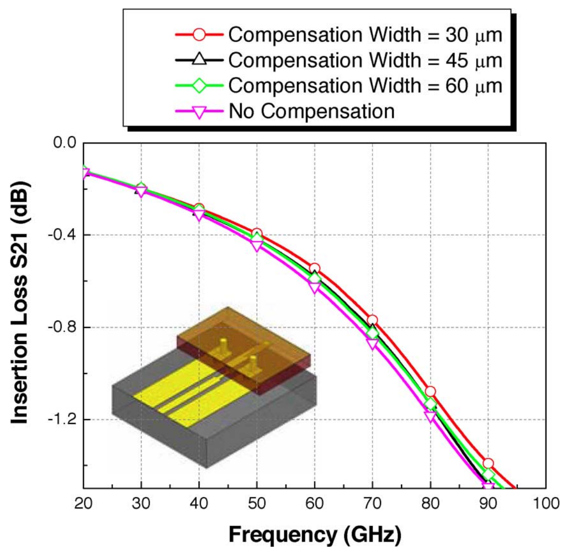

Fig. 5. Simulated insertion loss ($S21$) of the FC interconnect (single transition) with different compensation widths.

TABLE I
PARAMETERS OF THE OPTIMIZED FC DESIGN

Parameter	Value
Characteristic impedance of the CPW on Al_2O_3	50 Ω
Bump height	40 μm
Bump diameter	50 μm
Metal overlap	70 μm
Distance between signal and ground bumps (depends on the circuits)	150 μm for x8 143 μm for oscillator
Compensation width	30 μm
Compensation length	50 μm

is an excellent choice for low PN oscillators thanks to the good low-frequency noise properties and the high breakdown voltage [4]. The cross-coupled topology is chosen for its relatively good PN properties and ease of startup [21]. To simplify the bias scheme, a fixed-frequency oscillator is used instead of a voltage-controlled oscillator (VCO) as the major goal is to demonstrate the concept of building practice providing a low PN at V-band.

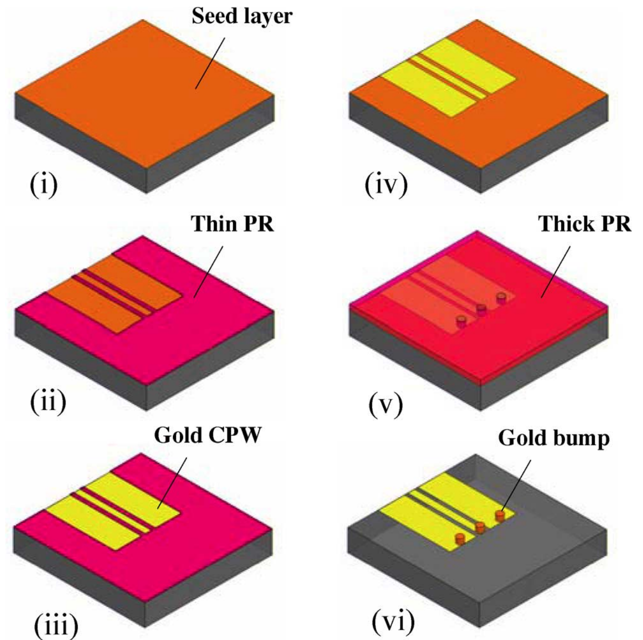

Fig. 6. Process flow of the Al_2O_3 carrier for FC assembly.

A. Process Technology for the Al_2O_3 Carrier

The Al_2O_3 carrier used for FC assembly of the MMICs was in-house fabricated in the Compound Semiconductor Laboratory (CSDLab), National Chiao Tung University (NCTU), Hsinchu, Taiwan [15]. Alumina (Al_2O_3) was chosen as the packaging carrier because of its good electrical characteristics for high-frequency applications ($\varepsilon_r = 9.7$ and $\tan\delta = 0.0002$). Moreover, Al_2O_3 has a thermal expansion coefficient (CTE $\sim$ 7 ppm/°C) very close to that of GaAs (CTE $\sim$ 5.8 ppm/°C), which can minimize potential thermal stress between the MMICs and the carrier, e.g., caused by temperature variations. The thickness of the Al_2O_3 carrier used in this study is about 254 μm (10 mil). Fig. 6 shows the process flow of the Al_2O_3 carrier used for FC assemblies. Gold (Au) metal, formed by cyanide-based electroplating, was used as the metallization of the transmission line and the vertical transition bumps. Firstly, Ti and gold metal were *in-situ* deposited using an E-gun evaporator onto the Al_2O_3 carrier with the thickness of 300 and 500 Å to form a continuous seed layers for gold electroplating. Ti was used as an adhesion layer. A thin photoresist (PR) was then patterned on the carrier for electroplating of the CPW circuits. After the electroplating of the gold circuits, the thin PR was removed. The wafer was then covered by a thick PR patterned to define the positions of the gold bumps that were formed by electroplating. By controlling the electroplating current density and time, the required bump height was achieved. The gold-bump height and diameter in this study were 40 and 50 μm, respectively. The seed layers were then removed with a KI/I_2 solution for the removal of

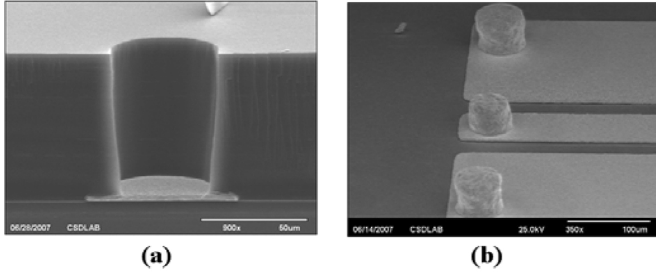

Fig. 7. (a) Cross-sectional SEM image of the thick PR profile before gold bump electroplating. (b) SEM image of the electroplated gold circuits and bumps on the Al_2O_3 carrier.

gold metal and HF dilute solution for the removal of the Ti metal. Fig. 7 shows the scanning electron microscope (SEM) image of the thick PR profile and the electroplated gold circuits and bumps on the Al_2O_3 carrier.

B. Chip Assembly Process

The MMIC oscillator and the $\times 8$ multiplier chips were FC bonded onto the Al_2O_3 carrier by the Au-to-Au thermo-compression method using a PP-5 TSV assembly machine from JFP Microtechnic, Marcoussis, France. After optimization, the temperature of the work holder was set to 300 °C and the bonding force was adjusted to 20 grams per bump, which was maintained for a bonding time of 60 s. As reference to the FC bonded module, the oscillator and multiplier were also attached using silver epoxy on a piece of brass and connected with conventional bond-wire technology. For further comparison, the individual oscillator and multiplier MMICs were also FC bonded and compared with the bare chip performances.

IV. Circuit Characterization

All the measurements were performed in the Microwave Electronics Laboratory (MEL), Department of Microtechnology and Nanoscience (MC2), Chalmers University of Technology, Göteborg, Sweden. The output power, oscillation frequency, and PN of the oscillators were measured using an HP8565EC spectrum analyzer. For characterization of the $\times 8$ multiplier, an HP83650B frequency synthesizer was used as the input signal source and the HP8565EC spectrum analyzer complemented with HP11974V V-band external mixers was used for measuring output power, PN, and oscillation frequency. S-parameter measurements of the $\times 8$ multiplier were also carried out using an Agilent precision network analyzer (PNA) E8361A. For comparison, the MMIC chips were measured before and after FC assembly.

The FC mounted V-band LO modules were characterized using the same spectrum analyzer and mixers as used for the $\times 8$ multiplier.

V. Measurement Results and Discussions

A. 7-GHz Cross-Coupled HBT Oscillators

Fig. 8 shows the chip photograph and circuit schematic of the cross-coupled HBT oscillator. There are two circuits in the same chip. The circuit on the right side is the fixed-frequency oscillator used in this study. Since the two circuits were not separated by dicing, the circuit on the left side was used as additional support by designing dummy bumps underneath its pads. The total chip area is 1.8×2 mm ^{2}. Fig. 9 shows the photograph of the FC bonded HBT oscillator. To investigate the influence of the FC mounting, an EM simulation was carried out in ADS Momentum. Fig. 10 shows a cross-sectional view of the simulated resonant tank of the oscillator with the effect from the FC carrier taken into account. A 40-μm-thick layer of air layer and a 254-μm-thick Al_2O_3 layer were added to represent the FC carrier in the Momentum substrate definition. Fig. 11 shows the simulated phase of the input impedance $\phi(Z_{\rm in})$ versus frequency before and after FC assembly. From the phase-frequency curve in Fig. 11, the Q factor can be calculated as

$$Q = \frac{-\omega_0}{2} \left| \frac{\partial \phi(Z_{\rm in})}{\partial \omega} \right|_{\omega=\omega_0}. \quad (1)$$

The calculated Q factors before and after the FC are estimated to be 28 and 33, respectively, i.e., 18% improvement in Q factor

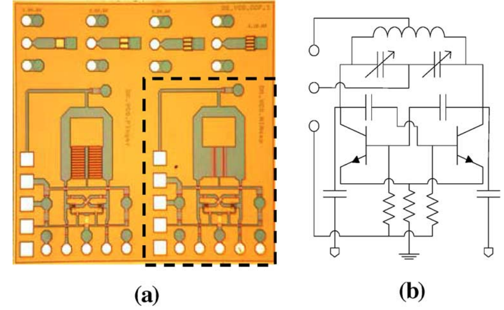

Fig. 8. (a) Chip photograph (right-hand side) and (b) circuit schematic of the cross-coupled HBT oscillator.

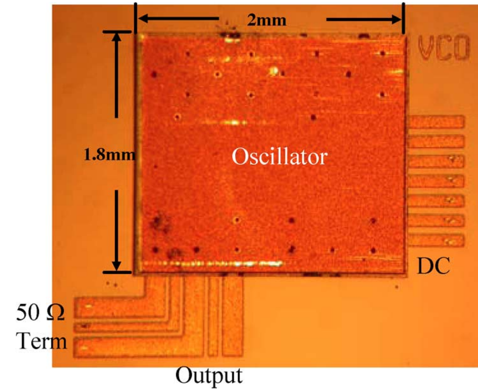

Fig. 9. Photograph of the FC bonded HBT oscillator.

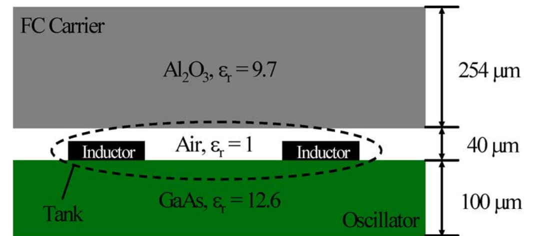

Fig. 10. Cross-sectional view of the simulated resonant tank of the oscillator taking the FC effect into account.

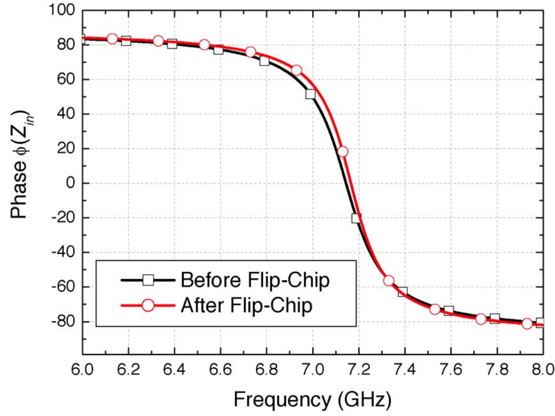

Fig. 11. Simulated phase of the input impedance $\phi(Z_{\rm in})$ of the oscillator versus frequency before and after FC assembly.

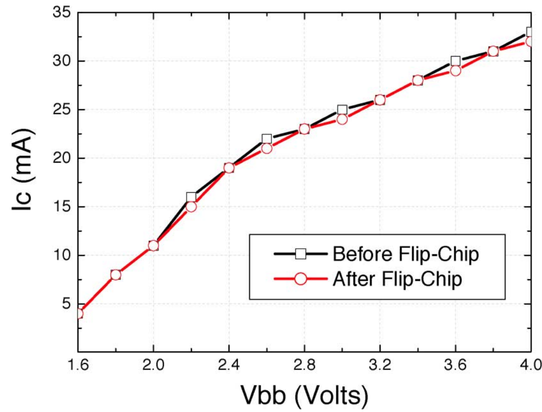

Fig. 12. Measured collector current of the oscillator before and after FC assembly. The collector bias voltage is $Vcc = 8$ V.

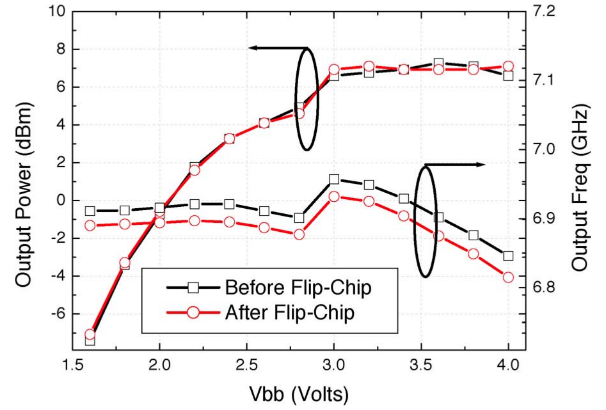

Fig. 13. Measured output power and frequency of the oscillator as function of the base voltage (Vbb) before and after FC.

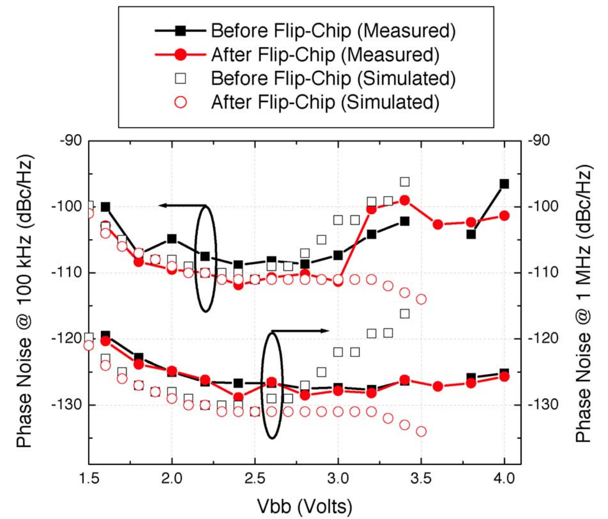

Fig. 14. Measured and simulated PN of the oscillator before and after FC assembly. The collector bias voltage is $Vcc = 8$ V.

of the resonant tank after FC assembly. In both cases, the resonant-frequency was 7.2 GHz, the shift in resonant frequency due to Al_2O_3 is negligible.

As seen in Fig. 8, the cross-coupled oscillator has a balanced output. The characterization of the circuit was accomplished by measuring one of the outputs, while the other was terminated in a 50-Ω load. Both outputs were also externally attenuated 3 dB to reduce the loading of the oscillator. Fig. 12 shows the measured dc current consumption of the oscillator, i.e., Ic versus Vbb at $Vcc = 8$ V, before and after FC assembly. After the FC, the current consumption was lower. Although the reduction was marginally within the range of the measurement accuracy, a slight reduction could be expected due to the improved tank Q. Fig. 13 shows the measured output power and oscillation frequency versus base voltage (Vbb). After FC assembly, the output power remained the same and the oscillation frequency was shifted as little as 25 MHz (0.35%).

To predict the oscillator PN, the S-parameters from the Momentum simulation were inserted into the oscillator equivalent circuit and the PN simulated with the harmonic balance tool in Agilent Technologies Advanced Design System (ADS). Fig. 14 shows measured and simulated PN for the flip-chipped oscillator and the probed MMIC oscillator compared to simulations. As can be seen in Fig. 14, the PN was improved after FC assembly, probably due to the better Q factor resulting from the mounting effect of the FC. The simulation and measurement results correspond well below $Vbb = 3$ V. Above $Vbb = 3$ V, the simulated results do not agree with the measurements, the reduced PN in simulation is most likely an artifact from model limitations when the oscillator goes into the voltage limited region. After FC assembly, the lowest PN are -112 dBc/Hz @ 100-kHz offset and -128 dBc/Hz @ 1-MHz offset. Compared to the previous publications [22]–[29], this is the lowest PN reported for an FC assembled oscillator. Table II presents the key figures of the FC oscillator in this work compared to FC oscillators in the open literature. To be able to compare PN of oscillators operating at different frequencies, the results are bench-marked after a normalized PN ($\mathrm{PN_{norm}}$) at 1-GHz and 100-kHz offset, calculated using Leeson's equation [30]

$$\mathrm{PN_{norm}} = \mathrm{PN_{dB}} - 20\log\left\{\frac{100 f_0}{\Delta f}\right\} = \mathrm{PN_{dB}} - 40 - 20\log\left\{\frac{f_0}{\Delta f}\right\} \tag{2}$$

TABLE II
FC OSCILLATOR IN THIS WORK COMPARED TO FC OSCILLATORS IN OPEN LITERATURE

Flip-Chip Oscillator	Device Technology	Frequency (GHz)	Phase Noise (dBc/Hz)	Normalized Phase Noise (1 GHz, 100 kHz offset)
[22]	CMOS	2.4	-108 @ 600 kHz offset	-100
[23]	CMOS	4	-126 @ 1MHz offset	-118
This Work	HBT	6.9	-111.33 @ 100 kHz offset -128.83 @ 1 MHz offset	-127.8
[24]	pHEMT	27	-84 @ 1 MHz offset	-92.6
[25]	pHEMT	27.55	-109 @ 1 MHz offset	-117.8
[26]	AlGaAs/In GaAs FET	31.7	-90 @ 1 MHz offset	-100
[27]	Gunn	34.45	-83.7 @ 100 kHz offset	-114.4
[28]	Gunn	58.74	-87.67 @ 100 kHz offset	-123
[29]	Gunn	76	-104 @ 1 MHz offset	-121.6

where f_0 is the oscillation frequency in gigahertz and $\mathrm{PN}_{\mathrm{dB}}$ is PN measured at an offset frequency Δf (in kilohertz). The figure-of-merit (FOM) $\mathrm{PN}_{\mathrm{norm}}$ resembles the conventional oscillator FOM [30] apart from the fact that it does not include the power consumption, which is intentionally omitted as it mixes up two parameters into the same FOM. The dc power consumption of the oscillator in this work is $P\mathrm{dc} = 8 \times 20 = 160$ (in milliwatts), which would yield a FOM of -187 using the definition in [31], which is very competitive. However, it is better to present PN and power consumption individually. The requirements on PN must first be fulfilled. It must then be verified that the power consumption is not too high for the application in mind.

Despite normalization in terms of oscillation and offset frequency, the comparison in Table II has limitations, e.g., it does not differ between fixed-frequency oscillators and VCOs. It is reasonable to question whether the good result is reached for our FC demonstrator (see Table II), thanks to the fact of using a fixed-frequency oscillator instead of a MMIC VCO. Most likely, a similar demonstrator based on a VCO would have about 6–8-dB higher PN, the difference between a MMIC oscillator and a VCO [17]. In this regard, our demonstrator would still be well placed in the comparison, none of the VCOs in Table II achieves PN better than this range. Another interesting aspect worth mentioning in the discussion of Table II is that most of the cited works are using high-Q passives on the FC motherboard, while this work demonstrates the FC of a bare-die MMIC oscillator so it is easy to see that FC assembly does not degrade the PN (see Fig. 14).

It should be mentioned that data compared in this work are measured with the HP8565EC spectrum analyzer, the MMIC oscillator was also measured using a dedicated PN measurement system Agilent 5500A with better noise floor. A PN as low as -117 dBc/Hz at 100 kHz off-set was then reached [17]. However, the Agilent 5500A system cannot be used at V-band frequencies. For this reason, we refer to the result from the spectrum analyzer in order to have a fair comparison to the V-band measurements.

B. V-Band $\times 8$ mHEMT Multiplier

Fig. 15 shows the circuit schematic of the mHEMT multiplier by eight ($\times 8$). It includes an input matching common-gate stage followed by a quadruper ($\times 4$), a feedback amplifier, a doubler ($\times 2$), and a buffer amplifier at the output. The topology was chosen for realization of a highly integrated V-band LO chain with high output power and good harmonic suppression. The input matching and interstage amplification were designed to occupy minimum chip area [3]. For measurements, the amplifiers were biased at $V\mathrm{gs} = -0.1$ V and $V\mathrm{ds} = 2.0$ V; the quadrupler and doubler were biased at $V\mathrm{gs} = -0.6$ V and $V\mathrm{ds} = 2.0$ V. Fig. 16 shows a photograph of the $\times 8$ multiplier before and after FC assembly. As can be seen, the lower circuit is the $\times 8$ multiplier used in this study. Since the circuits were not separated by dicing, the upper circuit (useless part) was used as additional support by designing dummy bumps underneath its pads. The total chip area is 2.8×4.2 mm^2.

To investigate the input and output matching of the multiplier, the S-parameter of the $\times 8$ multiplier was measured and compared before and after FC assembly. As can be seen in Fig. 17, in the frequency range of 7–12 GHz, the input matching is better than -15 dB, which is an improvement compared to the data before the FC. Similarly, the output return loss $S22$ was improved 5–10 dB (from 53 to 67 GHz) after FC assembly (see Fig. 18). The significant improvement is due to the flipping onto the CPW line, which ameliorates the matching to probes a lot at higher frequencies. In our later designs, the output RF pads on the chip were simulated, optimized, and modified to a short part of the CPW with a couple of via-holes to each ground plane (for frequencies higher than 50 GHz). There are many publications dedicated to a similar mollified RF pad. In conclusion, we would define the improvement as a consequence of connection to the CPW and the improvement according to the graph, which demonstrates the influence of compensation at high frequencies.

After the S-parameter measurements, the output power characteristics as function of input power and frequency were investigated. Fig. 19 presents the comparison of the measured output power versus input power before and after FC assembly. The input frequency was set at 7 GHz instead of 8.1 GHz, where the best $S11$ was obtained according to Fig. 17. The reason for using 7 GHz is that it is the oscillation frequency of the cross-coupled HBT oscillator that is connected to the input of the $\times 8$ multiplier in the V-band MCM frequency source. Fig. 19 shows that the output power was essentially unaffected by FC assembly. Only a small shift in the saturation point was detected. After the FC, the saturation occurs at lower input power, probably due to better input and output matching. Under variation of the input frequency with constant input power $P\mathrm{in} = 0$ dBm (see Fig. 20), the peak-output power shifted to lower frequency (from 56 to 54 GHz). An increased bandwidth was also observed, as expected, which is due to the improvement in the output matching (Fig. 18).

C. FC-Based V-Band MCM Frequency Source

It is now demonstrated that the FC does not have any significant negative effect on either the cross-coupled oscillator MMIC or the $\times 8$ multiplier MMIC. The next step is to combine the two into one FC MCM frequency source with hybrid device

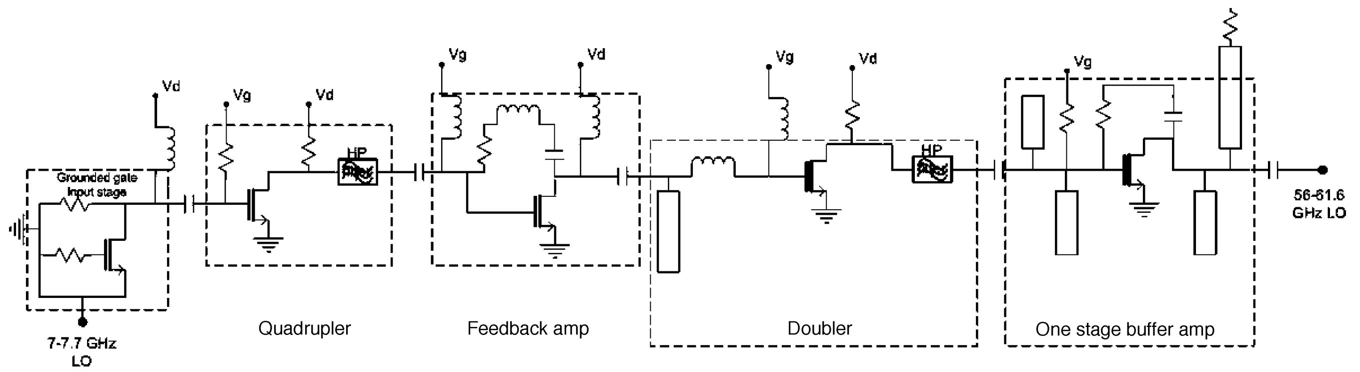

Fig. 15. Circuit schematic of the ×8 mHEMT MMIC multiplier.

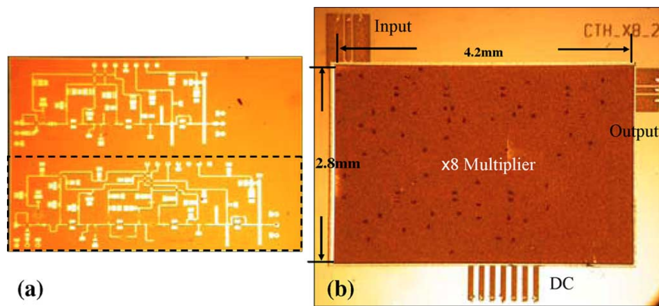

Fig. 16. Photographs of the ×8 mHEMT MMIC multiplier (a) before and (b) after FC assembly.

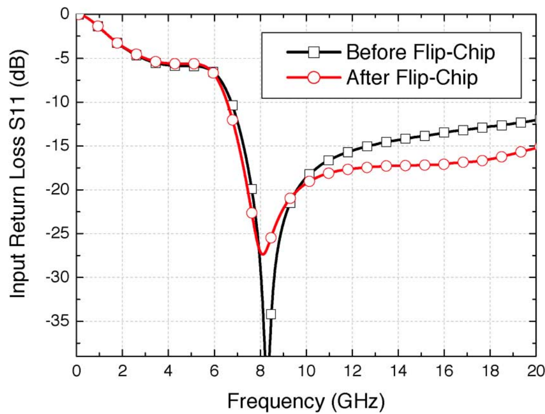

Fig. 17. Measured input return loss $S11$ of the ×8 multiplier before and after FC assembly.

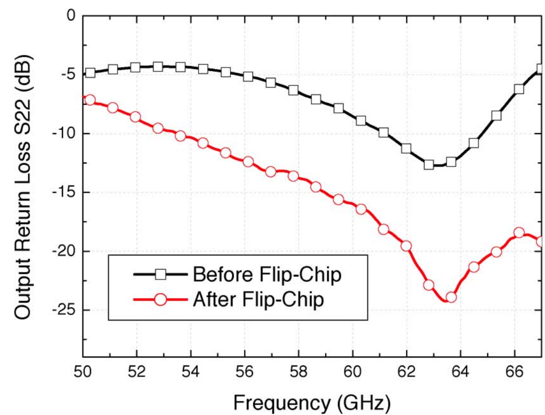

Fig. 18. Measured output return loss $S22$ of the ×8 multiplier before and after FC assembly.

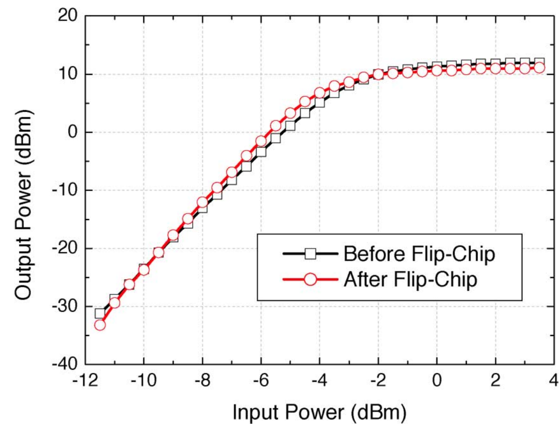

Fig. 19. Measured output power of the ×8 multiplier versus input power before and after FC assembly (Input frequency = 7 GHz).

technology on the Al_2O_3 carrier. Meanwhile, a bond-wire connected module was also realized for comparison. Fig. 21 shows the photographs of the FC and bond-wire assembled V-band LO MCMs. For the FC scheme, there are three transitions in the module, which are: 1) oscillator output to CPW on Al_2O_3 (7 GHz); 2) CPW on Al_2O_3 to ×8 input (7 GHz); and 3) ×8 output to CPW on Al_2O_3 (55 GHz). For the bond-wire scheme, the measurements were carried out by probing directly on the MMIC circuits, which means that there is only one bond-wire transition from the oscillator output to the ×8 input (7 GHz) in the module. In Fig. 13, the output power of the oscillator is around 7 dBm. Moreover, the loss from the oscillator output to the ×8 input at 7 GHz can almost be ignored for both FC and bond-wire schemes since the output power of the oscillator is 6 dBm and the loss of about 1 dB due to the chip-to-chip transmission still keeps the ×8 in compression at 0 dBm, as shown in Fig. 19. The bond-wire version, as a result, was expected to have higher output power at the ×8 output because, in this case, the transition from the MMIC to Al_2O_3 carrier was not included in the measurement. Fig. 22 presents a comparison of the measured output power and oscillation frequency versus oscillator base-voltage (Vbb) of the FC and bond-wire assembled LO MCMs. As indicated in Fig. 21(a), the carrier for the FC-based module is prepared for the termination of the nonused output.

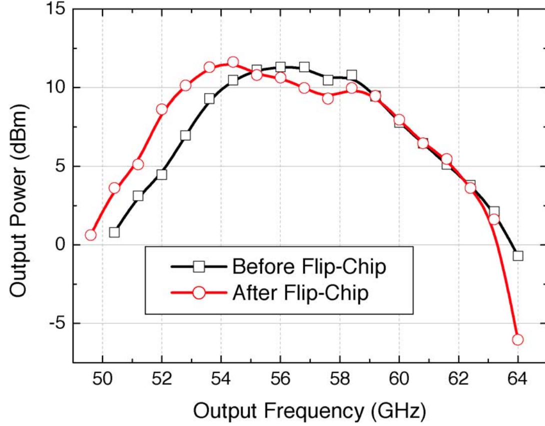

Fig. 20. Measured output power of the $\times 8$ multiplier versus frequency before and after FC assembly (Input power = 0 dBm).

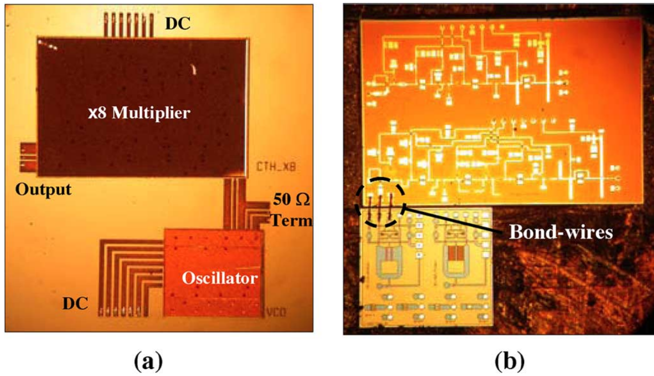

Fig. 21. Photograph of the: (a) FC and (b) bond-wire assembled V-band LO MCM module.

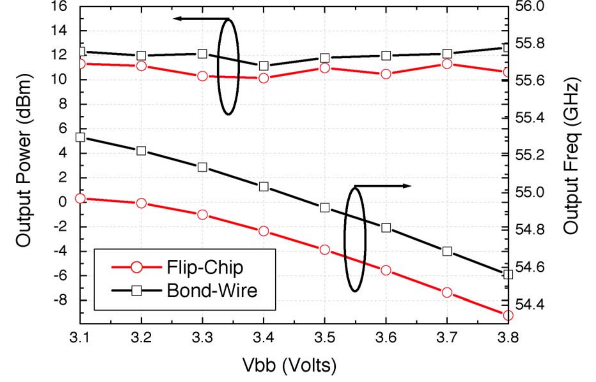

Fig. 22. Measured power and frequency characteristics of the FC and bond-wire assembled MCM LO module.

TABLE III
SUMMARY OF THE FC AND BOND-WIRE MCM LO MODULES

	Flip-Chip LO Module	Bond-Wire LO Module
Transitions	3	1
Output Power (in average)	11 dBm	12 dBm
Output Frequency	54.35 GHz ~ 55 GHz	54.56 GHz ~ 55.3 GHz
Tunable Frequency Range	650 MHz	740 MHz
PN @ 100 KHz (Vbb = 3.1 V)	-88 dBc	-86 dBc
PN @ 1 MHz (Vbb= 3.1 V)	-111.54 dBc	-109.4 dBc
Carrier Size	5.5 x 4.5 mm^2	4.6 x 4.2 mm^2
$(f)_{011}$ Cavity Resonance Frequency @ TE_{011}	43 GHz	48 GHz

In principle, this output could be connected to a phase-locked loop (PLL) for phase locking. However, in the measurements, it was terminated in a 50-Ω load preceded by 3-dB attenuation. For the bond-wire module shown in Fig. 21(b), there is no possibility to terminate the nonused output. To ensure that this would not affect the result, the FC-based module was measured both with and without termination and no significant difference was observed in the results. As expected, the bond-wire version had about 1-dBm higher output power compared to the FC version due to the excluded transition at the output port. The best PN was measured at an oscillator base–voltage $Vbb = 3.1$ V and collector–voltage $Vcc = 8$ V. The bond-wire version exhibited a PN of -86 dBc/Hz @ 100-kHz offset and -109 dBc/Hz @ 1-MHz offset; while the FC version exhibited a PN of -88 dBc @ 100 kHz and -112 dBc @ 1 MHz. The 2-dB lower PN for the FC mounted version can be explained by the better Q factor providing lower oscillator PN, as is demonstrated in Section V-A.

In Fig. 22, it is seen that the oscillation frequency can be altered $>1\%$ with the base voltage, but the signal stability is good only for a few discrete bias points, e.g., $Vbb = 3.1$ V, where the best PN is measured. The sensitivity to the applied base voltage is likely resulting in the fact that the $\times 8$ multiplier loads the oscillator output. A buffer amplifier at the output of the oscillator could alleviate this problem.

Table III summarizes the performance of the FC and bond-wire LO MCMs. The PN obtained for the FC-MCM frequency source is the lowest reported for V-band frequency sources in the open literature [32]–[43]. A comparison to other publications is given in Table IV, the results are bench-marked after the normalized PN presented in (2). The power consumption of the multiplier is in the order of 200 mW. Adding the power consumption of the oscillator, the total power consumption is still below 400 mW, yielding a PN-power FOM $\mathrm{FOM} = -180$, which is excellent for a V-band frequency source [31].

For applications, the assembled MMIC module has to be packaged into a metal house with coaxial connectors or waveguide interfaces, which might cause instability of the output signal due to the cavity resonances. For a rectangular cavity, as shown in Fig. 23, the cavity resonances could happen in the following frequencies [44]:

$$(f)_{mnp} = \frac{1}{2\sqrt{\varepsilon\mu}} \sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2 + \left(\frac{p}{c}\right)^2} \tag{3}$$

where ε is the material permittivity, μ is the material permeability, and m, n and p are integers. Here, the TE_{011} mode is the dominant mode since it occurs at the lowest frequency at which a cavity resonance can exist [45]. $(f)_{011}$ of the FC module and bond-wire module are found to be 43 and 48 GHz, respectively. This means that the resonances could occur if the

TABLE IV
SUMMARY AND COMPARISON OF MILLIMETER-WAVE FREQUENCY SOURCES IN OPEN LITERATURE

Reference	Frequency Source	Device Technology	Frequency (GHz)	Phase Noise (dBc/Hz)	Normalized Phase Noise (1 GHz, 100 kHz offset)	Output Power (dBm)	Interconnect
[32]	VCO	SiGe Bipolar	36-46.9	-110 @ 1 MHz offset	-122.4	8.9	Bond-Wire
[33]	VCO	AlInAs/InGaAs HBT	38	-82 @ 100 kHz offset	-113.6	10	No
[34]	VCO	SiGe BiCMOS	40	-99 @ 1 MHz offset	-111	-	No
[35]	VCO	InGaP HBT	40.5	-83 @ 100 kHz offset	-115.1	0	No
[36]	VCO	InGaP-GaAs	40.8	-95 @ 100 kHz offset	-127.2	5.3	No
[31]	VCO	SiGe HBT	43	-86 @ 100 kHz offset	-118.7	-17	No
[37]	PLL	SiGe BiCMOS	48	-98 @ 1MHz offset	-111.6	-	No
This Work	Oscillator + x8 Multipiler	HBT + mHEMT	55	-112 @ 1 MHz offset	-126.8	11	Flip-Chip
[38]	Oscillator + Doubler	MESFET + pHEMT	55.6-60.3	-90 @ 1 MHz offset	-105.3	3.5	Bond-Wire
[39]	VCO	DH-HEMT	55.9	-103 @ 1 MHz offset	-117.9	11.1	No
[40]	VCO	CMOS	56.4-57.6	-113.6 @ 10 MHz offset	-108.7	-5	No
[28]	VCO	Gunn	58.74	-87.67 @ 100 kHz offset	-123	18	Flip-Chip
[41]	PLL	CMOS	61	-90 @ 1 MHz offset	-105.7	-7	No
[42]	VCO	InP HBT	62.4	-78 @ 100 kHz offset	-113.9	4	No
[43]	PLL	BiCMOS	75.67-78.5	-103.5 @ 1MHz offset	-121.2	-17.8	No
[29]	VCO	Gunn	76	-104 @ 1 MHz offset	-121.6	13.5	Flip-Chip

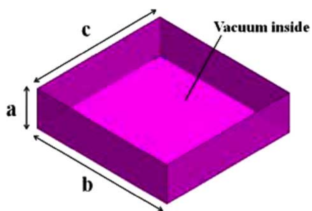

Fig. 23. Rectangular cavity with corresponding a, b, and c in (3).

operating frequencies of the modules are higher than 43 and 48 GHz. Due to smaller cavity size, $(f)_{011}$ of the bond-wire is higher than that of the FC. However, the bond-wire module excludes the other oscillator output for PLL implementation, which also occupies some additional space and increases the size of the bond-wire module. Moreover, the FC has a smaller footprint than the bond-wire. After considering these issues, we could expect the $(f)_{011}$ of the FC module would be higher than that of the bond-wire module.

Unfortunately, if we take the other components such as dc bias, protection circuits, connectors, and waveguide flanges into consideration, $(f)_{011}$ will be further reduced. One solution is aligning the MMICs in as narrow a row as possible, which results in higher resonance frequencies. Otherwise, another promising approach is using an absorber material to dampen the resonances [45].

It is worth mentioning that both the oscillator and multiplier chip have two circuits on the same chip. The module size can be reduced significantly if the circuits were separated by dicing.

VI. CONCLUSION

This work has successfully demonstrated FC assembly of a 7-GHz low PN cross-coupled HBT oscillator and a $\times 8$ mHEMT multiplier into an ultra-low PN V-band MCM frequency source. It has been a shown that FC bonding is an excellent assembly technology for the implementation of millimeter-wave frequency sources. Compared with the bare-die

measurements, the FC technology does not have any detrimental effect on the chip performance, neither for oscillators, nor for multipliers. On the contrary, the chip performance was improved. After the FC, the PN of the cross-coupled InGaP HBT oscillator was improved due to an increased Q factor of the resonant tank. A properly designed FC transition can also act as an additional matching network; an improved input and output matching was obtained for the $\times 8$ mHEMT multiplier chain using FC assembly. The FC assembled V-band MCM frequency source exhibits a PN of -88 dBc/Hz @ 100-kHz offset and -112 dBc/Hz @ 1-MHz offset. To the authors' best knowledge, this is the lowest PN ever reported for a V-band free-running frequency source.

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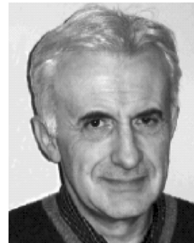

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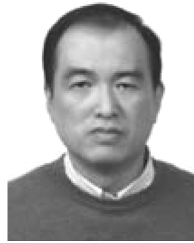

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