New CMOS-Compatible Micromachined Embedded Coplanar Waveguide

Chih-Peng Lin and Christina F. Jou

***Abstract*—This paper proposes a new robust micromachined embedded coplanar waveguide (CPW). The central and ground plates are partially bent and overlapped within the trench, and due to tight coupling of the E-field between the overlapped plates, the micromachined embedded CPW line is capable of a wide range characteristic impedance (17.9–92.3 Ω), in a compact size. Furthermore, the area in which the E-field radiates into the substrate of the micromachined embedded CPW is quite narrow compared to conventional CPWs, and therefore, the dielectric loss of the micromachined embedded CPW can be effectively suppressed. Compared with conventional CPW lines, the embedded CPW lines have shown a marked reduction in loss, especially in the low-impedance range. The micromachined embedded CPW lines on the high-resistivity silicon substrate ($\rho_s = 15\,000\ \Omega \cdot \text{cm}$) achieve a measured loss as low as 0.81 dB/cm at 50 GHz. Moreover, the fabrication process of the micromachined embedded CPW line is compatible with the CMOS process. These features make micromachined embedded CPW a promising transmission line for RF integrated circuit application.**

***Index Terms*—Coplanar waveguide (CPW), micromachining technology, transmission line.**

I. Introduction

COPLANAR waveguides (CPWs) are often preferred by circuit designers and used extensively in high-density RF and monolithic microwave integrated circuits because their various advantages such as uniplanar configuration and ease of fabrication. However, CPW-based transmission lines generally suffer from a limited usable impedance ranges, especially at high and low characteristic impedance (Z_0), and the loss of CPW lines tend to increase rapidly at higher frequencies [1], [2]. In order to solve these issues, a variety of modified CPW transmission lines with a number promising features have been proposed during the last decade. The main functions of the modified CPW lines are to reduce loss and increase the usable range of Z_0.

Silicon as a microwave substrate, has many advantages including its low cost and the fact that it is a mature technology. However, transmission lines and integrated passive devices generally suffer significant losses due to high dielectric loss of low-resistivity silicon substrate at RF frequency. The dielectric loss is the obstacle to the design of distributed passive components in integrated circuits of silicon. To solve this problem, a high-resistivity silicon substrate is widely used for microwave application because of its low dielectric loss. The performance comparison of various RF passive components on different substrates is presented in [3], and high-resistivity silicon has proven an excellent candidate for a substrate in RF integrated circuit (RFIC) design [3]–[5].

Another approach to loss reduction and increased Z_0 range is to modify the geometry of the transmission lines. For instance, by using membrane technology, the inner conductor can be suspended in the air, thus eliminating the dielectric loss at millimeter-wave frequencies for high-Z_0 lines. This design is classified as microshield lines [6]. The micromachining technique is considered the most practical method in this regard [7]–[12]. One micromachined CPW is called channelized CPW lines [7], the material underneath the coupled aperture is partially removed to form the free-space V-shaped grooves. The total propagation loss is minimized because most of the electromagnetic (EM) fields are distributed in the free-space V-shaped region and current density flow on the conductor is reduced. Another micromachined CPW, called an overlay CPW, has been proposed [8], wherein the edges of the central conductor are partially elevated and overlaid with the two outer ground plates. It achieves low-loss characteristics (< 0.95 dB/cm at 50 GHz) through the redistribution of the current over a broad area, and at the same time as the Z_0 range widens (25–80 Ω). However, as is commonly known, no present studies have yet achieved a robust structure and wide range Z_0 with a corresponding low loss by means of a simple fabrication process, which is also compatible with CMOS technology.

This paper demonstrates a robust new micromachined CPW structure called the embedded CPW. A schematic of the micromachined embedded CPW line is shown in Fig. 1(a): the central and ground plates are partially bent and overlapped within the substrate. The loss of the embedded CPW line can be kept to a fairly low degree even on a lossy silicon substrate. Therefore, high-resistivity silicon was selected to be the substrate in the following design, purely to show a comparable contrast of losses between the conventional CPW and the embedded CPW lines. The loss characteristics of the embedded CPW lines were studied in detail for various trench widths and overlapped metal lengths. Field simulations and comparative experiments have demonstrated the characteristics of the embedded CPW lines. The embedded CPW lines were fabricated on a high-resistivity silicon substrate showing a capacity of wide range characteristic

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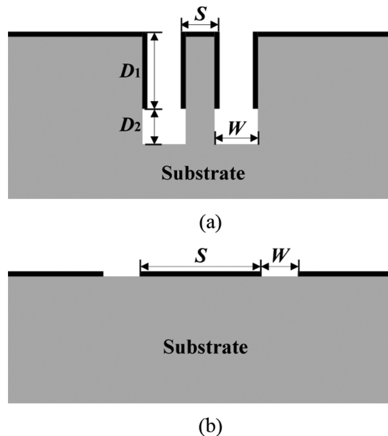

Fig. 1. Schematic diagrams of: (a) micromachined embedded CPW and (b) conventional CPW with associated parameters.

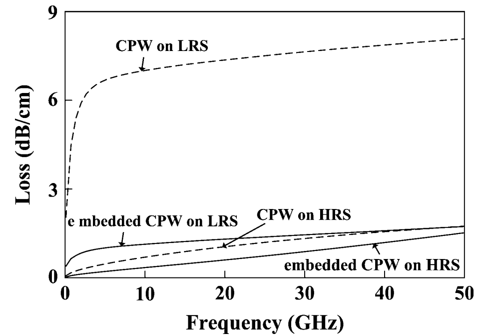

Fig. 2. Comparison of simulated losses for the conventional CPW and the micromachined embedded CPW lines fabricated on both the low-resistivity silicon (LRS, $\rho_s = 50\ \Omega \cdot$ cm) and high-resistivity silicon (HRS, $\rho_s = 15\,000\ \Omega \cdot$ cm) substrates.

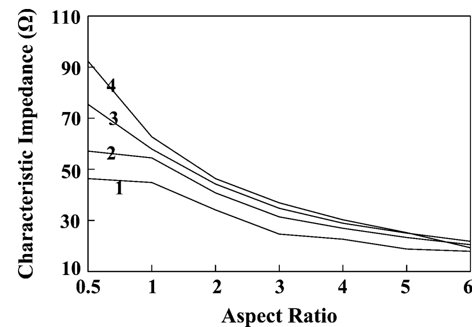

Fig. 3. Simulation results of aspect ratio (D_1/W) as function of characteristics impedance of the micromachined embedded CPW lines. Curve 1–4 is represented as $W = 10, 20, 30,$ and 40 μm, respectively.

impedance from 17.9 to 92.3 Ω with low measured loss (minimum 0.89 dB/cm at 50 GHz). The low loss was due to tight coupling of the E-field between the overlapped plates, effectively suppressing the dielectric loss.

II. Design and Simulation

Fig. 1(a) and (b) shows the schematic structures of the embedded CPW and the conventional CPW, respectively. In the embedded CPW design, the signal linewidth is defined as "$S + 2D_1$", and "W" is the trench width. The total trench depth is $D = D_1 + D_2$, which D_1 is the length of overlapped metal plates within the trench and D_2 represents the remainder of the trench depth. D_1/W is defined as aspect ratio (D_1/W). In this design, the total trench depth D was selected as 250 μm in order to reach a compromise between minimum loss and robustness.

The simulation was carried out at 50 GHz using a full-wave finite-element method, implemented through Ansoft Technologies' High Frequency Structure Simulator (HFSS). The simulation results of the loss in decibels/centimeters are shown in Fig. 2 in which both of the CPW and embedded CPW lines are designed to be 50 Ω and fabricated on both the lossy silicon (low-resistivity silicon, $\rho_s = 50\ \Omega \cdot$ cm) and the high-resistivity silicon ($\rho_s = 15\,000\ \Omega \cdot$ cm substrates. In Fig. 2, the embedded CPW lines showed low-loss performance on both lossy silicon and high-resistivity silicon substrate (below 1.7 dB/cm at 50 GHz). In contrast to the embedded CPW line, the loss of the conventional CPW line increased dramatically while it was on the lossy standard CMOS silicon substrate (more than 8 dB/cm at 50 GHz). A 1-cm-long conventional CPW fabricated on the lossy silicon substrate is impractical that the loss of the conventional CPW is significant higher than the embedded CPW, especially at a low-impedance range. Therefore, a high-resistivity silicon substrate was chosen in the following design to show a comparable contrast of losses between the conventional CPW and the embedded CPW lines. All transmission lines were fabricated by using a 525-μm-thick high-resistivity silicon substrate ($\varepsilon_r = 11.9$ and $\rho_s = 15\,000\ \Omega \cdot$ cm).

In Fig. 3, when W was fixed at 10, 20, 30, and 40 μm, Z_0 of the embedded CPW line could be designed by varying the aspect ratio. Low-impedance lines could be implanted by increasing the aspect ratio. On the other hand, high $-Z_0$ lines could also be implanted by reducing the aspect ratio without additional process difficulty. As shown in Fig. 3, the embedded CPW line is capable of a wide impedance range from 17.9 to 92.3 Ω. As W is fixed at 10 μm with aspect ratio $= 6$, Z_0 can reach as low as 17.9 Ω. As W is fixed at 40 μm with aspect ratio $= 0.5$, Z_0 can reach up to 92.3 Ω.

III. Parameter Study

The simulated losses as a function of Z_0 were shown in Fig. 4. The associated dimension of both the conventional CPW lines and embedded CPW lines is as follows.

1) Conventional CPW: $S = 20\ \mu$m for each $W; W = 3, 5, 10, 20, 30, 40, 60, 80,$ and 100 μm
2) Embedded CPW: $S = 20\ \mu$m for each $W; W = 10\ \mu$m, $D_1 = 5, 10, 20, 30, 40, 50,$ and 60 μm, $W = 20\ \mu$m, $D_1 = 10 \sim 120\ \mu$m, $W = 30\ \mu$m, $D_1 = 15 \sim 180\ \mu$m, $W = 40\ \mu$m, $D_1 = 20 \sim 240\ \mu$m.

As shown in Fig. 4, the characteristic impedance of the conventional CPW line could not be reduced below 26 Ω due to the limitations of photolithography. Moreover, the loss of the conventional CPW line increased rapidly when Z_0 was below 37 Ω, which showed that the conventional CPW line was impractical in low Z_0 application. In contrast with the conventional CPW line, the embedded CPW line has no difficulty to reach low Z_0 and maintain low loss at the same time. For the embedded CPW line, as $W = 40\ \mu$m, the loss can be maintained below 1 dB/cm for the entire range of Z_0 from 19.3 to 92.3 μm.

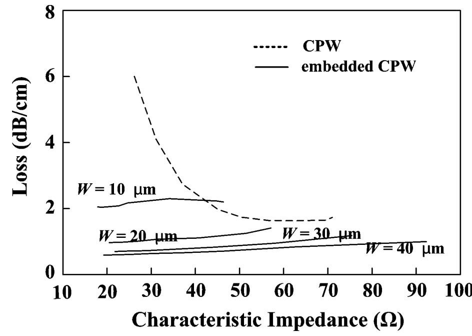

Fig. 4. Comparison of simulated losses as a function of Z_0 for different dimensions of the conventional CPW and the micromachined embedded CPW (as $W = 10, 20, 30$, and 40 μm that the aspect ratio (D_1/W) is varied from 0.5 to 6 for each W) on the 525-μm-thick high-resistivity silicon substrate.

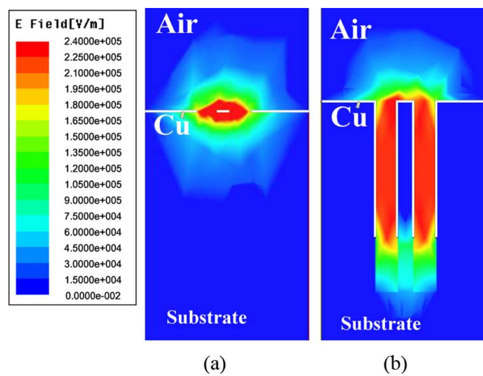

Fig. 5. Cross-sectional schematic of electric field distribution for: (a) conventional CPW and (b) micromachined embedded CPW.

In Fig. 5, the electric field distribution in the embedded CPW lines are simulated and shown in the cross-sectional view. Fig. 5(a) shows the conventional CPW line with $S = 20$ μm and $W = 30$ μm, and Fig. 5(b) shows the embedded CPW line with $S = 20$ μm, $W = 30$ μm, $D_1 = 180$ μm, and $D_2 = 70$ μm. As shown in Fig. 5(a), the E-field radiates into the substrate directly causing considerable dielectric loss. In contrast with the conventional CPW, the embedded CPW shows that the reduction of dielectric loss can be accomplished by confining most of the electric field to the air between the overlapped plates (D_1) within the trench (Fig. 5(b) shows the cross-sectional schematic of E-field distribution for the embedded CPW). The rest of the E-field will radiate into the bottom of the trench (D_2). Since the area in which the E-field radiates into the substrate of the embedded CPW is quite narrow compared to the conventional CPW, the dielectric loss of the embedded CPW can be suppressed efficiently. It is worth noticing in Fig. 5(b) that the E-fields radiating into the center of the substrate underneath the signal plate $(S + 2D_1)$ are the major causes of the loss in the embedded CPW. Therefore, by reducing the size of S, we cannot only reduce the dielectric loss, but also shrink the size. As we can see in Fig. 6, the simulation indicates that smaller S led to lower loss. In this paper, due to fabrication concerns, the length of S was selected to be 20 μm in order to reach a compromise between loss performance and fabrication difficulties.

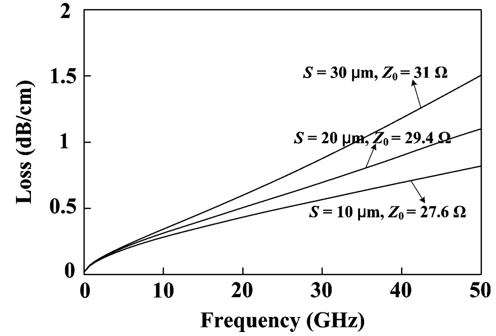

Fig. 6. Attenuation of the micromachined embedded CPW lines with variation on parameter S as $S = 10$ μm, $S = 20$ μm, and $S = 30$, respectively ($W = 30$ μm, $D_1 = 120$ μm, and $D_2 = 130$ μm for each line).

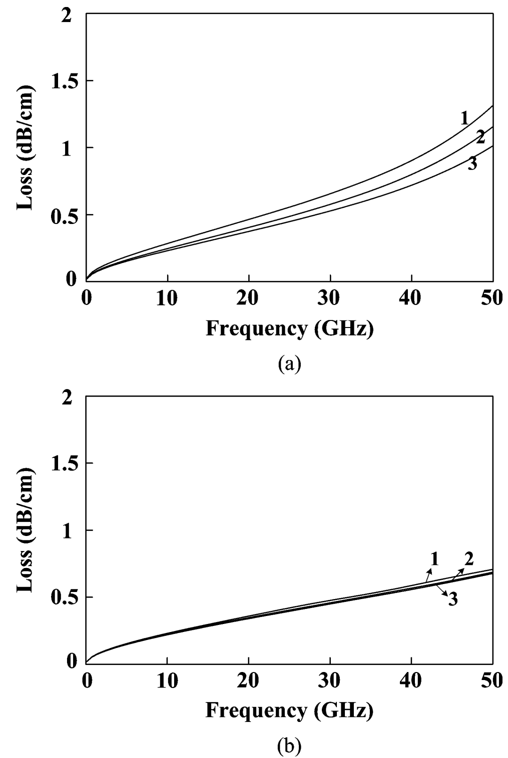

Fig. 7. Attenuation of the micromachined embedded CPW lines with variation on parameter: (a) D_2, curve 1–3 is represented as $D_2 = 0$ μm, 10 μm, and 20 μm, respectively ($S = 20$ μm, $W = 30$ μm, and $D_1 = 120$ μm for each line). (b) D_1, curve 1–3 is represented as $D_1 = 80$ μm, 90 μm, and 100 μm, respectively ($S = 20$ μm, $W = 30$ μm, and $D = 250$ μm for each line).

Fig. 7(a) shows that as $W = 40$ μm and D_1 is fixed at 160 μm, the loss decreases as D_2 increases (total trench depth D increases) due to a reduction in the dielectric loss. Fig. 7(b) shows that as $W = 40$ μm and $D = 250$ μm, the loss decreased as D_1 increased (ohmic loss decreases). Comparing Fig. 7(a) with Fig. 7(b), it can also be observed that the loss varied dramatically with D_2, while the loss reduction contributed by increasing D_1 was relatively small. Consequently, the loss mechanisms of the embedded CPW lines was dominated by the dielectric loss.

Miniaturization in RFIC design is considered a significant issue. For the embedded CPW lines, as W is fixed, Z_0 can be adjusted simply by varying the aspect ratio without increasing the

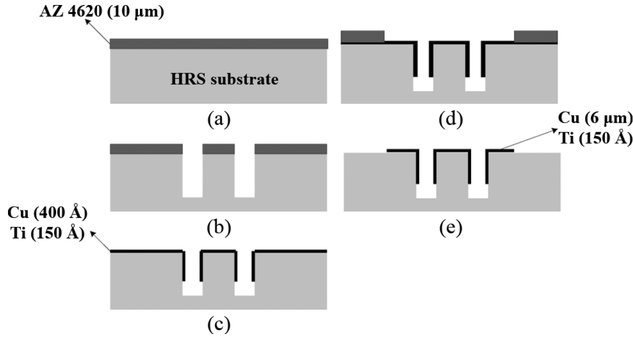

Fig. 8. Fabrication process flows for the micromachined embedded CPW line. (a) Photoresist coating. (b) Lithography (mask-1) then inductively coupled plasma deep etching of high-resistivity silicon substrate and photoresist removal. (c) Sputtering of Ti and Cu. (d) Lithography (mask-2) then electroplating of Cu. (e) Remove photoresist then stripping of Cu in unwanted position.

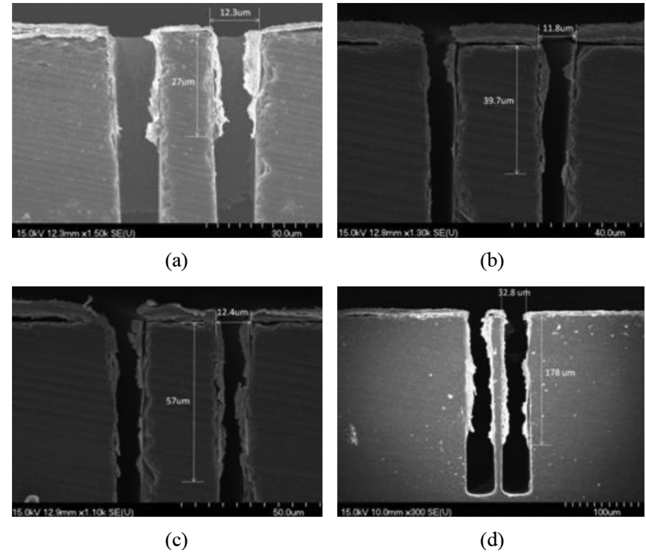

Fig. 9. Scanning electron microscope (SEM) photograph of different aspect ratio in the micromachined embedded CPW lines with corresponding process parameters. (a) Aspect ratio $= 1.8$; Ti: 5 mtorr, 5 min and Cu: 10 mtorr, 5 min. (b) Aspect ratio $= 3.3$; Ti: 5 mtorr, 10 min and Cu: 10 mtorr, 20 min. (c) Aspectratio $= 4.6$; Ti: 10 mtorr, 10 min and Cu: 20 mtorr, 10 min. (d) Aspect ratio $= 5.4$; Ti: 10 mtorr, 10 min and Cu: 20 mtorr, 20 min.

surface area $(2W + S)$. Unlike the embedded CPW lines, Z_0 of the conventional CPW was mainly affected by the geometrical parameters of W and S. As a result, to reach the same Z_0, the conventional CPW consumed a larger surface area than the embedded CPW did, especially at high Z_0: for instance, when $Z_0 = 70$ μm, the totally surface area of the conventional CPW was $2 \times 80 + 20$ μm, while the embedded CPW could achieve the same Z_0 using only $2 \times 10 + 20$ μm surface area. These results demonstrated that the embedded CPW lines could be very compact.

IV. Fabrication

The embedded CPW lines were fabricated on 525-μm-thick high-resistivity silicon substrates ($\rho_s = 15\,000\ \Omega \cdot$ cm with the length of 1 cm. Fig. 8 illustrates the entire fabrication process flow of the embedded CPW line. The fabrication of the embedded CPW is as follows.

1) Photoresist AZ4620 was spin-coated on the substrate [see Fig. 8(a)].
2) The desired trench position was defined by photolithography in which the hard-bake step was skipped for better trench formation. The trench was formed through inductively coupled plasma etching [see Fig. 8(b)]. For inductively coupled plasma etching, the etching selectivity between photoresist and silicon was 1:50. Therefore, the desired trench depth of 250-μm trench depth with very sharp sidewalls was easily achieved.
3) Metallization was performed through sputtering and electroplating technology.
   a) A 15-nm titanium-adhesion-layer and a 40-nm copper-seed-layer were sputtered [see Fig. 8(c)].
   b) The desired position to deposit was patterned with photoresit AZ 4620.
   c) Electroplating of copper to a thickness of about 6 μm [see Fig. 8(d)].

It is worth mentioning that while sputtering metal into the trench, if the aspect ratio of the trench were greater than the metal step coverage, the metal would only deposit on the sidewalls of the trench instead of covering the entire trench. This phenomenon was used to form the overlapping plate structure within the trench. Moreover, the desired depth of the sputtered metal on the sidewalls within the trench could be well controlled by adjusting chamber pressure and sputtering time, as shown in Fig. 9, with associated process parameters in the figure caption. In the final step, after the photoresist had been removed, a Cu stripper was used to remove the Cu from the unwanted areas [see Fig. 8(e)].

The fabrication process of the embedded CPW line was fairly simple; only two masks were required. Additionally, the fabrication process followed the CMOS process, showing the capability of integration with RFICs.

V. Measurement

A microphotograph of the fabricated embedded CPW line on the high-resistivity silicon substrate is shown in Fig. 10(a) and a cross-sectional view of the embedded CPW is shown in Fig. 10(c). The S-parameters of all the 1-cm-long lines were measured up to 60 GHz using an Agilent E8361A network analyzer and cascade wafer probe station. The system was calibrated by a short-open-load-thru (SOLT) to remove systematic errors in the test system and to define measurement reference. A set of open coplanar pads was also designed and fabricated adjacent to the lines, in order to de-embed the parasitic effects of the transmission line pads.

Thirteen sets of lines fabricated on high-resistivity silicon substrate have been measured to obtain S-parameters, including the embedded CPW lines ($S = 20$ μm, $W = 30$ μm, $D_1 = 10, 30, 100,$ and 150 μm, $S = 20$ μm, $W = 40$ μm, $D_1 = 40, 120,$ and 200 μm) and the conventional CPW lines ($S = 20$ μm, $W = 5, 10, 20, 30, 80,$ and 100 μm). The measured

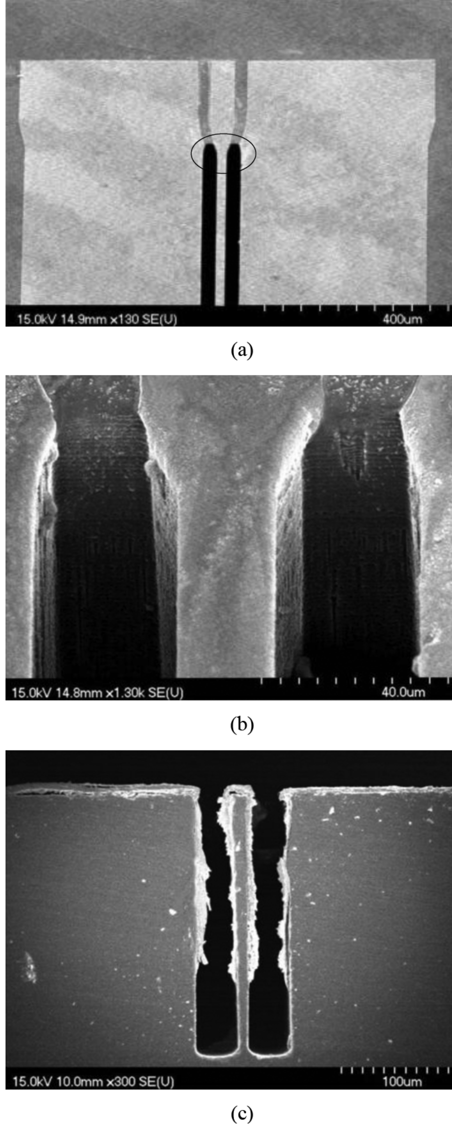

Fig. 10. SEM photograph of the micromachined embedded CPW line. (a) Probing pad from the top view. (b) Enlargement in the circled region in (a). (c) Cross-sectional view.

S-parameters are converted to $ABCD$-parameters, and using the following formula [14]:

$$Z_{0l} = \sqrt{\frac{B}{C}} \tag{1a}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l) & Z_{0l}\sinh(\gamma l) \\ \frac{\sinh(\gamma l)}{Z_{0l}} & \cosh(\gamma l) \end{bmatrix} \tag{1b}$$

(1a) to obtain Z_{0l}, and then extract propagation constant γ from (1b). Where Z_{0l}, and l are the characteristic impedance, the propagation constant and length of the transmission line, respectively. Therefore, the propagation constant could be determined as

$$\gamma = \frac{1}{l}\cosh^{-1}(A) = \frac{1}{l}\ln(A \pm \sqrt{A^2 - 1}).$$

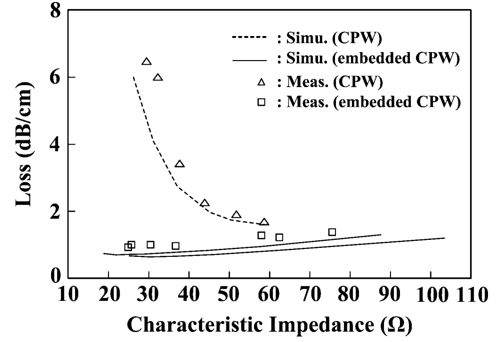

Fig. 11. Measured and simulated losses for the CPW ($S = 20$ μm, $W = 5, 10, 20, 30, 80$, and 100 μm) and the micromachined embedded CPW ($S = 20$ μm, $W = 30$ μm, $D_1 = 10, 30, 100$, and 150 μm; $W = 40$ μm, $D_1 = 40, 120$, and 200 μm).

The real part of γ is the attenuation constant that represents conductor and dielectric loss of the measured transmission lines.

The measured loss as a function of Z_0 is shown in Fig. 11. The measured results of the embedded CPW lines showed strong correlation with the simulated results. The discrepancy between simulation and measured losses should be caused by variations in the fabrication process. The measured loss of the embedded CPW lines was below 1.67 dB/cm of impedance range from 24.9 to 76.2 Ω. The minimum loss is 0.81 dB/cm was $Z_0 = 24.9\ \Omega$ ($S = 20$ μm, $W = 40$ μm, $D_1 = 200$ μm). Compared with the conventional CPW lines, the embedded CPW lines showed a substantial improvement on loss, especially in the low-impedance range. Fig. 11 clearly shows the advantage of the embedded CPW lines for low $-Z_0$ applications. As $Z_0 \sim 30\ \Omega$, there is a noticeable reduction in loss of 1.2 dB/cm in the embedded CPW versus 7 dB/cm of loss in the conventional CPW line.

Due to the minimal dielectric loss of the embedded CPW lines, the gradual loss reduction from high $-Z_0$ to low $-Z_0$ in this study may be attributed to an enhanced spreading of the current across a wider area as the aspect ratio increased.

VI. Conclusion

In this paper, a new CPW structure called the micromachined embedded CPW was demonstrated. The embedded structure was proposed to provide such promising features, such as a wide characteristic impedance range with low loss, while at the same time ensuring compact size and strong mechanical support. EM simulation and comparative experiments were utilized to fully characterize the embedded CPW lines. The embedded CPW lines on both a lossy silicon and high-resistivity silicon substrate showed fairly low losses. With the implementation of the high-resistivity silicon substrate, the embedded CPW lines showed relatively low measured loss below 1.67 dB/cm from 24.9 to 76.2 Ω at 50 GHz (minimum loss of 0.81 dB/cm as $Z_0 = 24.9\ \Omega$). Compared with conventional CPW lines, the embedded CPW lines showed a marked improvement on loss, especially in the low-impedance range. Moreover, the fabrication process of the embedded CPW lines was fairly simple and compatible with the CMOS fabrication process. These promising

features confirm the embedded CPW as a promising uniplanar transmission line base for RFIC applications.

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