High-Reliability Dynamic-Threshold Source-Side Injection for 2-Bit/Cell With MLC Operation of Wrapped Select-Gate SONOS in NOR-Type Flash Memory

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***Abstract*—For the first time, a high-performance ($\tau_{\rm PGM} = 200$ ns/$\tau_{\rm ERS} = 5$ ms) cell with superior reliability characteristics is demonstrated in a NOR-type architecture, using dynamic-threshold source-side injection (DTSSI) in a wrapped select-gate silicon–oxide–nitride–oxide–silicon memory device, with multilevel and 2-bit/cell operation. Using DTSSI enables easy extraction of the multilevel states with a tight $V_{\rm TH}$ distribution, a nearly negligible second-bit effect, superior endurance characteristics, and good data retention.**

***Index Terms*—Flash memory, multilevel states in a cell (MLC), NOR, silicon–oxide–nitride–oxide–silicon (SONOS).**

I. Introduction

THE silicon–oxide–nitride–oxide–silicon (SONOS) memory device has become one of the most popular candidates for replacement of conventional floating-gate memory when shrinking the tunneling-oxide thickness to 5 nm [1], [2]. One of the reasons is that the density of such Flash memory devices can be doubled without increasing the die size, which is a phenomenon known as 2-bit/cell operation [3], [4], under separated storage characteristics. Bit-1 and bit-2 can then be read out using the highly reliable reverse-read scheme [5].

Similar to 2-bit/cell operation, multilevel states in a cell (MLC) is another attractive approach for achieving high-density application in a Flash memory device [6], [7]. MLC operation entails construction of different levels of charge in the nitride trapping layer of a SONOS device. The different combination of charge states is then identified using a highly reliable method for distinguishing between each level of charge. However, owing to the larger sensor margin requirements required to precisely distinguish different charge levels, channel hot-electron injection with lower programming efficiency is not suitable for MLC operation due to its relatively high power consumption. In this brief, 2-bit/cell operation with MLC in a wrapped select-gate polysilicon–oxide–nitride–oxide–silicon (WSG-SONOS) memory is carried out using dynamic-threshold source-side injection (DTSSI) [8]. A fast programming speed with quite low power consumption was easily achieved for highly reliable 2-bit/cell with MLC in a WSG-SONOS memory device for a NOR-type array.

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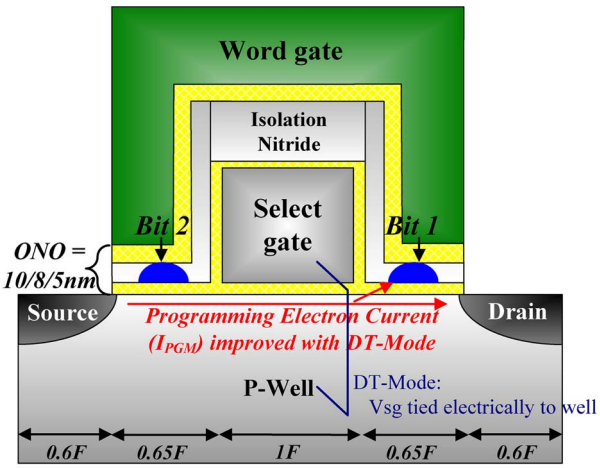
II. Experiments

Fig. 1 shows a cross section of the WSG-SONOS memory with 2-bit/cell operation in a NOR-type architecture. The equilibrium cell size is 3.5 F^2 for each bit, and 0.18-μm ground rule technology was used to fabricate the device. The channel length of the word gate is 0.65 F, which is defined by the distance between the select gate and the drain/source region. The channel length and width of the embedded MOSFET with *in situ* n^+-doped poly-Si select gate are 1 and 2 F, respectively. To execute DTSSI in a WSG-SONOS memory device, the select gate wrapped around the oxide/nitride/oxide layers is electrically tied to the p-well during programming. Additionally, the clear 2-bit/cell and multilevel operation schemes of the WSG-SONOS memory with DTSSI are also displayed in Fig. 1. Erasing and reading techniques were performed by band-to-band hot-hole injection and reverse read, respectively.

In this device, the thickness values of the blocking oxide/silicon nitride/tunneling oxide layers are 10.0, 8.0, and 5.0 nm, respectively, and the distance between the nitride trapping layer and select gate is 15 nm induced by the higher thermal growth rate on the side wall of the polysilicon select gate than on the single-crystal silicon [9]. As a result, the two physical bits can be separated by the embedded MOSFET structure of the WSG-SONOS memory in the NOR-type array, resulting in a better second-bit effect using the reverse-read scheme in a very short WSG-SONOS memory device.



Multi-level states: / DT-Mode:			"10" state, V_{WL}=9V	"01" state, V_{WL}=10V	"00" state, V_{WL}=11V		
Bit-1 operation	Mode	Time	V_{WL}	V_D	V_S	V_{SG}	V_{Well}
Program	DT	200ns	9~11V	4V	0V	0.45V	0.45V
Erase	BTBT	5ms	-4V	6V	0V	0V	0V
Read	Reverse	Sweep time	Sweep 0-8V	1.8V	0V	1.6V	0V

Fig. 1. Cross-sectional scheme of a 2-bit/cell WSG-SONOS memory device in DT mode. DTSSI is used to electrically tie the select gate to the p-well. The two physical bits are separated by the embedded MOSFET.

III. Results and Discussions

Fig. 1 shows the operation scheme of the WSG-SONOS memory programmed by the DTSSI (DT mode) method. To realize high-performance multilevel operations with the WSG-SONOS memory, the select gate was electrically tied to the p-well in DT mode. The "10," "01," and "00" states ($V_{\rm TH}$ shift more than 1, 2, and 3 V) can thus easily be obtained. Here, the constant sensing current method ($I_{\rm PGM} = 0.1\ \mu$A) was used in reverse-read mode ($V_{\rm BL} = 1.8$ V and $V_{\rm SG} = 1.6$ V) to distinguish between each state, and the "11" state was defined as the initial state in our memory devices [10], [11].

Fig. 2 shows the endurance characteristics of the WSG-SONOS memory with multilevel application under DT and normal modes, respectively. The normal mode here is used to demonstrate the WSG-SONOS device operated in the traditional source-side injection method without connecting the well and the select gate. The multilevel states are programmed at the same $V_{\rm WL} = 9$, 10, and 11 V in both modes with different programming times for DT mode ($\tau_{\rm PGM} = 200$ ns) and normal mode ($\tau_{\rm PGM} = 1\ \mu$s). In this cycling test, the bit line and select gate were biased at 4 and 0.45 V, respectively. Furthermore, an erasing time of 5 ms using band-to-band hot holes was selected for the recombination process with the word line and bit line biased at -4 and 6 V, respectively. The results demonstrate that the sensing margin between each bit can still remain highly accurate with almost no $V_{\rm TH}$ variation even after 10^4 program/erase (P/E) cycles.

The data retention characteristics of the WSG-SONOS with different multilevel states after 10^4 P/E cycles and unicycle test with 125 °C and 250 °C baking temperatures are observed in

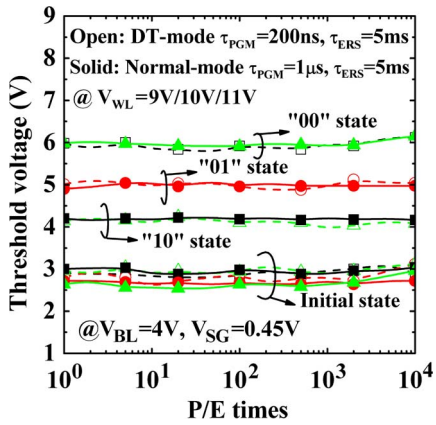


Fig. 2. Endurance characteristics across different multilevel states of the WSG-SONOS memory for DT and normal modes with the same $V_{\rm WL}$, $V_{\rm BL}$, and $V_{\rm SG}$, respectively.

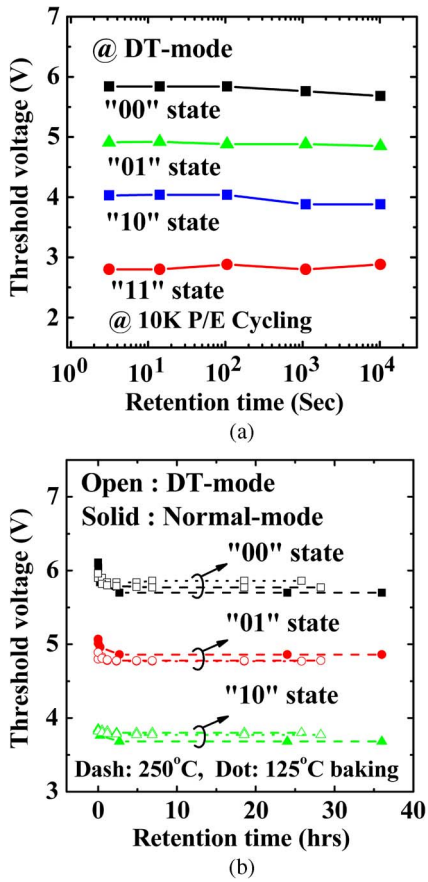


Fig. 3. Data retention characteristics for different multilevel states obtained from the WSG-SONOS memory (a) after 10^4 P/E cycles and (b) at low/high baking temperature 125 °C/250 °C, respectively.

Fig. 3(a) and (b), respectively. Due to the spatial distribution mismatch of carrier types, the lateral migration and redistribution of both electrons and holes would degrade the sensing margin through long retention time [12]. In addition, to exclude the defect annealing effect, the lower bake temperature at 125 °C was applied. V_t is almost stable, which implies a high quality of our tunneling oxide with few interface charging in our device. It is also obvious that V_t variations saturate in both bake temperatures even after long bake time. The higher baking temperature

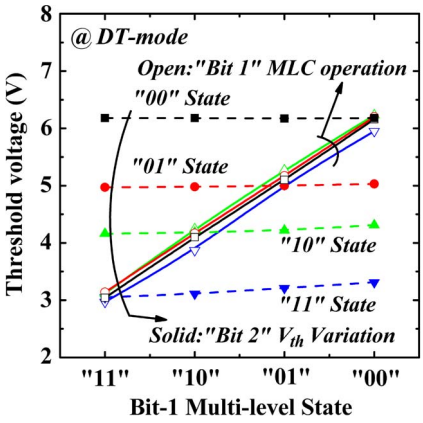


Fig. 4. Superior second-bit effect characteristics of WSG-SONOS memory for different multilevel states programmed using DT mode.

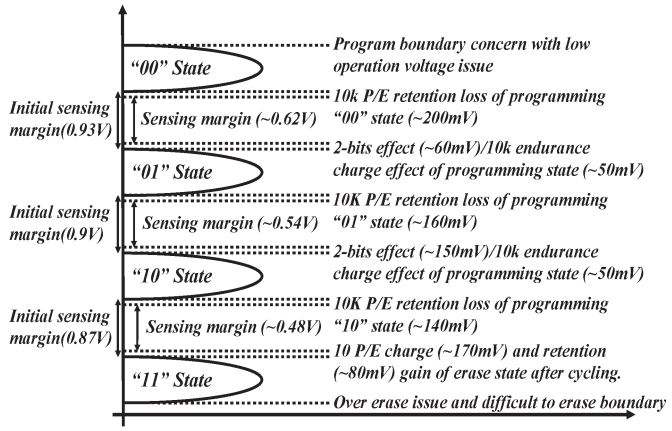


Fig. 5. Estimation of the sensing margin for multilevel operation of WSG-SONOS memory with nonideal reliability effects in a NOR array.

exhibit the larger V_t variations, which demonstrates that the higher thermal temperature increases the activation energy of the trapping charges in the silicon nitride and accelerates these high-energy electrons tunnel out from the trapping center or migrates and redistributes in the nitride trapping layer, resulting in variations in the threshold voltage for each multilevel state [13]. Fortunately, the memory window is preserved, remaining large enough to enable highly reliable distinguishing of the different states in the WSG-SONOS memory device with such a nonideal charge loss effect.

Crosstalk immunity can easily be obtained between the two physical bits for different multilevel states in the WSG-SONOS memory under reverse-read mode, as shown in Fig. 4. The bit-1 (neighboring the drain side, as indicated in Fig. 1) of the horizontal axis was programmed to different multilevel states ("10," "01," and "00" states) in DT mode, whereas bit-2 was kept in various multilevel states. In our device, when using $V_{\rm BL} = 1.8$ V and $V_{\rm SG} = 1.6$ V to discriminate the exact multilevel states, there is almost no crosstalk between these two bits in the WSG-SONOS memory. The results show that the storage characteristics of these two physical bits in a cell can reliably be distinguished. Briefly, the bit-line and select-gate biases should be optimized to avoid serious short-channel effects in a very short channel WSG-SONOS device, and then, a highly reliable multilevel with 2-bit/cell operation in DT mode can be achieved in a scaled-down WSG-SONOS memory cell.

In sum, the real sensing margins of our exemplary array for multilevel with 2-bit/cell operations under DT mode with nonideal reliability issues can then be preliminary estimated, as summarized in Fig. 5. The sensing margin of more than 0.45 V could still be maintained in our device through accelerated reliability tests. The results demonstrate that the WSG-SONOS device in a NOR-type array simultaneously achieves superior performance with high reliability for 2-bit/cell and multilevel applications using DTSSI.

IV. Conclusion

A novel high-performance DTSSI in WSG-SONOS memory with reliable multilevel application for 2-bit/cell operations has successfully been demonstrated in this brief. We obtained highly reliable multilevel operation using DTSSI to program our WSG-SONOS memory. The greater noise margin between each multilevel state provides higher flexibility for sensor amplification in circuit design and indicates the high potential of the WSG-SONOS memory programmed with DTSSI for high-reliability Flash applications in the future.

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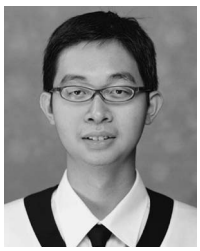

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