Gate and Drain Currents in Off-State Buried-Type p-Channel LDD MOSFET's

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Abstract—**The buried-type p-channel LDD MOSFET's biased at high positive gate voltage exhibit new characteristics: 1) the ratio of the drain to gate currents is about 1×10^{-3} to 5×10^{-3}; and 2) the gate and drain currents both are functions of only the gate voltage minus the n-well bias. Such characteristics are addressed based on the formation of the surface n^+ inversion layer due to the punchthrough of the buried channel to the underlying shallow p-n junction. The measured gate current is due to the Fowler–Nordheim tunneling of electrons from this inversion layer surface and the holes generated within the high-field oxide constitute the drain current. The n^+ inversion layer surface potential is found to be equal to the n-well bias plus 0.55 V. As a result, not only the oxide field but also the gate and drain currents are independent of drain voltage.**

I. Introduction

RECENTLY, the off-state MOSFET's or equivalently the gate-controlled reverse-bias diodes have been extensively investigated and the associated phenomena have been newly reported [1]–[7]. In the work of [1]–[7], the gate current is reported to be less than the drain current by several orders of magnitude and/or both are strong functions of drain voltage. Based on the off-state buried-type p-channel LDD-MOSFET's, however, we have found that not only is the drain current less than the gate current by several orders of magnitude, but also both are independent of drain voltage. In this letter, we will report such new I–V characteristics and the corresponding interpretations.

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II. Experiment

The devices were fabricated by a 0.8-μm twin-well polycide CMOS process. The starting material was p-type $\langle 100 \rangle$-oriented Si wafers with resistivity of 10 $\Omega \cdot$cm. Phosphorus (6.5×10^{12} cm^{-2}, 80 keV) was implanted to form the n-well region. BF_2 (2.8×10^{12} cm^{-2}, 80 keV) was used as the threshold voltage implant. The gate oxide was grown in dry O_2 at 920°C to a thickness of 180 Å. After gate poly deposition and phosphorus doping, a layer of WSi_2 (2500 Å) was deposited and annealed at 920°C to form the n^+ polycide gate. BF_2 (10^{13} cm^{-2}, 50 keV) was implanted to form the low-doped drain region. After the sidewall spacer (3000 Å) was formed, BF_2 (3×10^{15} cm^{-2}, 80 keV) was implanted to form the highly doped drain region.

With the source floating and the n-well grounded, each structure with the assigned drain terminal condition has been characterized by measuring the gate and drain currents as function of gate voltage ranging from 16 to 21 V. Fig. 1 shows the corresponding measurement results for three drain voltages, 0, −3, −5 V, and also with the drain floating. From Fig. 1 it can be clearly observed that 1) the drain current is less than the gate current with an I_D/I_G ratio of about 1×10^{-3} to 5×10^{-3}; 2) both the gate and drain currents are independent of drain voltage; and 3) the gate current is not affected when the drain is floated. Moreover, the characterization has been performed for n-well bias $V_{BB} = 0$ and 2 V under $V_D = -3$ V and the corresponding results are shown in Fig. 2. From Fig. 2 we can observe that as the n-well bias changes from 0 to 2 V, not only the gate current versus gate voltage characteristics but also the drain current versus gate voltage characteristics are shifted right by a value of about 2 V.

III. Discussion

Based on the observations mentioned above, the problem can be simply reduced to the Fowler–Nordheim tunneling in a single metal–oxide–p-n diode, i.e., as the gate voltage increases positively to deplete the p-channel re-

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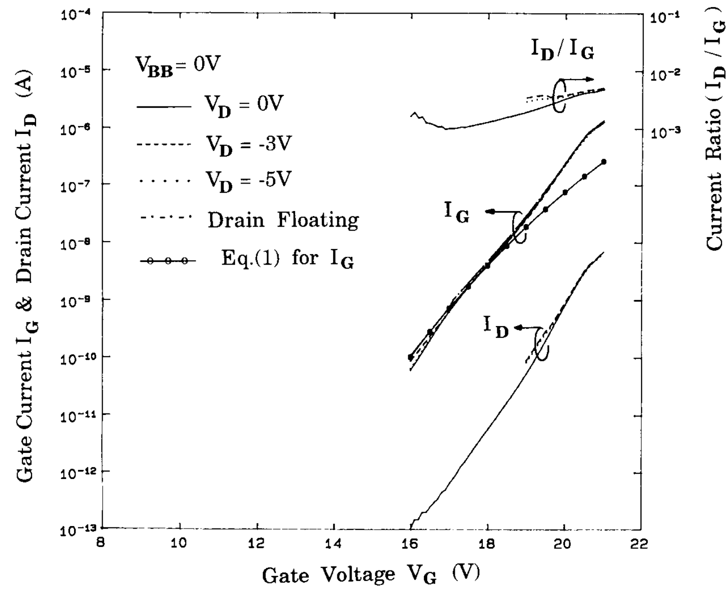

Fig. 1. Measured gate and drain currents as function of gate voltage for drain voltages of 0, −3, and −5 V where the corresponding current ratios are also shown. The measured gate I–V characteristic for the drain terminal floating is also shown. The calculated F–N current versus gate voltage with $\alpha = 4.12 \times 10^{-6}$ A/V^2 and $\beta = 2.42 \times 10^8$ V/cm in (1) is presented for comparison. Gate width is 100 μm.

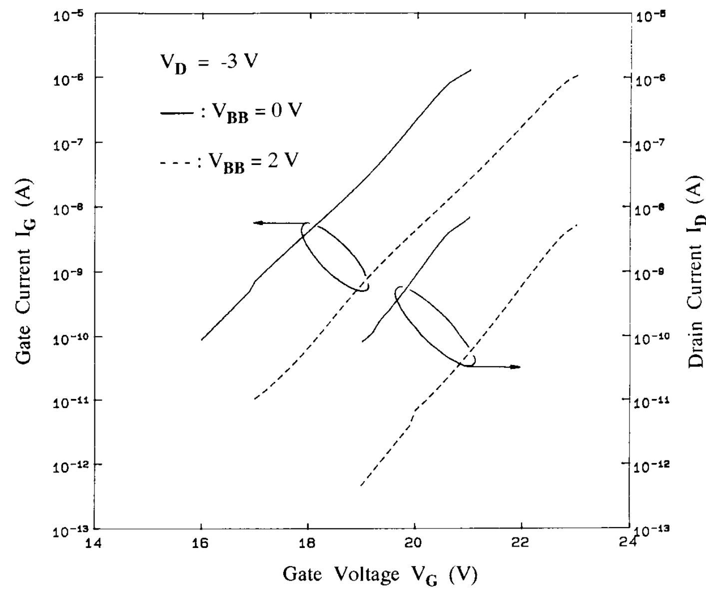

Fig. 2. Measured gate and drain currents as function of gate voltage for two n-well biases of 0 and 2 V under the same drain voltage of −3 V. Gate width is 100 μm.

gion under the oxide until the punchthrough to the shallow p-n junction occurs, the electrons will be injected from the n-well to the surface where an n^+ inversion layer under the oxide is thus formed. The device simulator PISCES-IIB is used to predict the potential distributions, from which we have concluded that the inversion-layer surface potential is equal to the n-well bias plus 0.55 V and is independent of both gate voltage and drain voltage. Simulation results are shown in Fig. 3 where the potential contours are plotted for $V_D = -3$ V, $V_G = 20$ V, and $V_{BB} = 2$ V. Similar results are obtained with $V_{BB} = 0$ V. This can be justified by the measurement of changing the n-well bias as shown in Fig. 2.

Therefore, the F–N tunneling of conduction-band electrons from the inversion surface dominates the gate current. To confirm this interpretation, the calculation of the F–N current I_G as function of oxide field E_{ox} is performed using the following equations [8]:

$$I_G = A_G \cdot \alpha \cdot E_{ox}^2 \cdot \exp(-\beta/E_{ox}) \quad (1)$$

and

$$E_{ox} = ((V_G - V_{BB}) - (V_{FB} + \varphi_s))/t_{ox} \quad (2)$$

where $A_G(=150\ \mu m^2)$ is the oxide area, $t_{ox}(=180$ Å) is the oxide thickness, $V_{FB}(=0.44$ V as measured by *CV* method) is the flat-band voltage, and $\varphi_s(=V_{BB} + 0.55$ V as mentioned above) is the associated surface potential. The values of the preexponential constant $\alpha(=4.12 \times 10^{-6}\ A/V^2)$ and the physical constant $\beta(=2.42 \times 10^8$ V/cm) have been obtained by fitting the low-level range of gate current in Fig. 1. These fitting values are close to those of $\alpha = 2.3 \times 10^{-6}\ A/V^2$ and $\beta = 2.385 \times 10^8$ V/cm as cited in [8]. The deviation at the high V_G values in Fig. 1 may be due to the enhancement of the local field in the oxide which is caused by the trapped holes [9].

One may propose several mechanisms such as band-to-band tunneling [1], [2], silicon valence-band electron tunneling [10], and hole generation within the high-field oxide [11], [12] to account for the observed drain currents. However, the band-to-band tunneling mechanism is not accepted here since it is a strong function of drain voltage [1]–[7]. The ratio of the silicon valence-band electron tunneling to the conduction-band electron tunneling has been estimated to be about 10^{-6} [11], [12]. Thus, the silicon valence-band electron tunneling mechanism cannot account for our measured ratio of 1×10^{-3} to 5×10^{-3}. According to the work of [11], not only the holes generated inside the high-field oxide are linked to the conduction-band electron tunneling from the n^+ inversion layer surface, but also both are function of only the oxide field. Therefore, the collection of the holes generated within the high-field oxide is suggested to be the origin of our measured drain currents.

Note that for the n-channel MOSFET's connected as

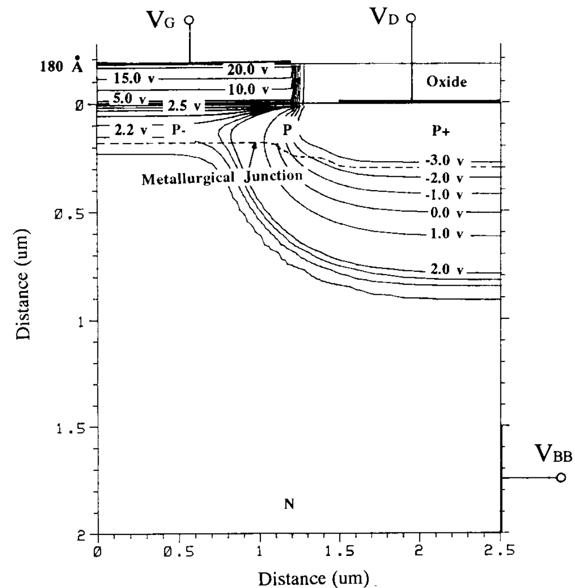

Fig. 3. Simulated potential contours corresponding to $V_D = -3$ V, $V_G = 20$ V, and $V_{BB} = 2$ V. The parameter of flat-band voltage $V_{FB} = 0$ V was used in simulation.

the gate-controlled n^+-p diodes with the n^+ inversion layer induced under the oxide, the gate and substrate hole currents have been shown to be due to the silicon conduction-band electron tunneling and the collection of the holes generated inside the oxide, respectively [11], [12]. Fig. 4 shows the corresponding gate and hole collection current densities versus oxide field for two oxide thicknesses of 154 and 200 Å (see [11, fig. 1]). In Fig. 4 we also present the results obtained from Fig. 1 where the drain current represents the hole collection current. Based on Fig. 4, it can be concluded that our *I–V* characteristics measured from the off-state buried-type p-channel LDD MOSFET's are analogous to those from the gate-controlled n^+-p diodes having the n^+ inversion layer. The relationships between the two are: 1) the drain hole current in our work corresponds to the substrate hole current in [11] and [12]; 2) the electrons within the surface n^+ inversion layer are provided by the injection from the n-well in our work while in [11] and [12] the n^+ inversion layer beneath the gate oxide is electrically connected to the n^+ drain region.

IV. Conclusion

The drain and gate currents measured from the off-state buried-type PMOSFET's have been found to be independent of drain voltage. The electron F–N tunneling from the n^+ inversion layer surface and the collection of the holes generated inside the oxide can be applied to reasonably explain our measured results. The analogies between the off-state buried-type p-channel LDD MOSFET's and

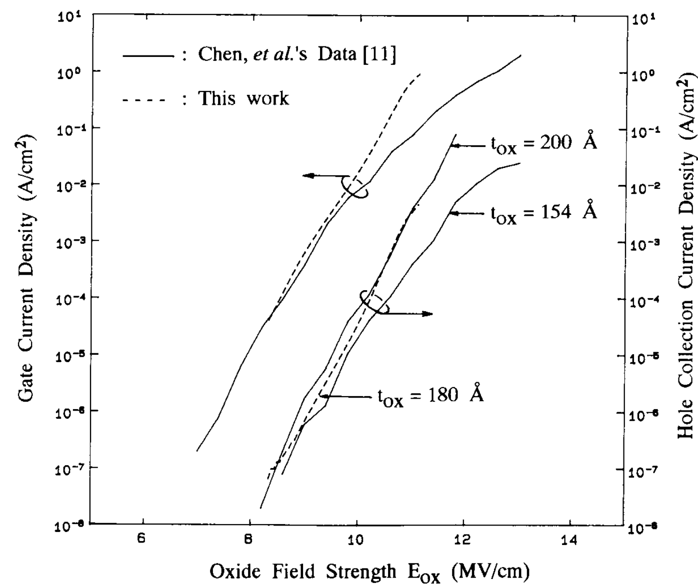

Fig. 4. Comparisons of the measured gate and hole collection current densities versus oxide field as cited in [11] and those corresponding to Fig. 1. Here the drain current in Fig. 1 represents the hole collection current and the substrate hole current in [11] represents the hole collection current.

the gate-controlled n^+-p diodes with the n^+ inversion layer have also been addressed.

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