Ultralow-Power Ni/GeO/STO/TaN Resistive Switching Memory

C. H. Cheng, Albert Chin, and F. S. Yeh

***Abstract*—Using novel stacked covalent-bond-dielectric GeO_x (GeO) on metal-oxide $SrTiO_3$ to form a cost-effective Ni/GeO/SrTiO/TaN resistive switching memory, an ultralow set power of small 4 μW (3.5 μA at 1.1 V), a reset power of 16 pW (0.12 nA at 0.13 V), and a large 10^6 memory window for 10^5-s retention at 85 °C are realized for the first time. A positive temperature coefficient is measured at low-resistance state and different from the metallic filament in metal-oxide resistive random access memory.**

***Index Terms*—GeO_2, resistive random access memory (RRAM), $SrTiO_3$ (STO).**

I. Introduction

ALTHOUGH the charge-trapping Flash (CTF) nonvolatile memory [1], [2] provides better scalability than a poly-Si floating-gate Flash device, the degraded retention at a highly scaled cell size is the fundamental challenge according to the *International Technology Roadmap for Semiconductors* [1]. The cross-point resistive random access memory (RRAM) [3]–[13] shows high potential for downscaling beyond metal–oxide–nitride–oxide–semiconductor CTF; unfortunately, the high set and reset currents are the basic limitation for high-density and low-power operation. Moreover, for array operation and vertical 3-D stacking, the small-size diode-driven RRAM is preferred [4] to one-transistor–one-resistance structure, but the conventional diode-driven unipolar RRAM suffered even higher power consumption from forming and reset operations.

To address these issues, we report a novel ultralow-power RRAM device with only 4-μW setting power, an ultralow reset power of 16 pW, and excellent retention window at 85 °C. Such record high performances were achieved using covalent-bond dielectric/metal oxide of $GeO_x/SrTiO_3$ (GeO/STO) with a negative temperature coefficient (TC) at low-resistance state (LRS) that is quite different from the positive TC and metallic filament in metal-oxide RRAM [3].

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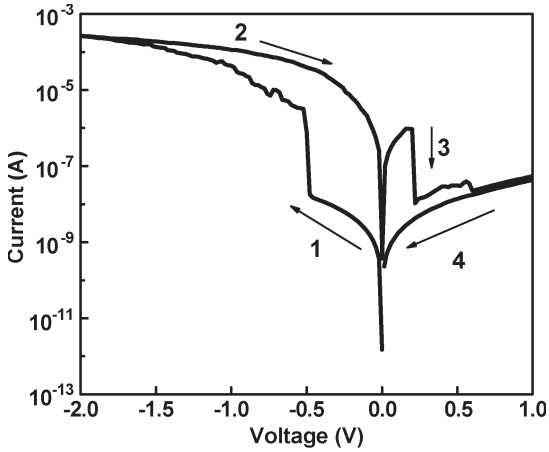


Fig. 1. Swept I–V curves of a conventional Ni/STO/TaN RRAM. The arrows indicate the bias sweeping direction.

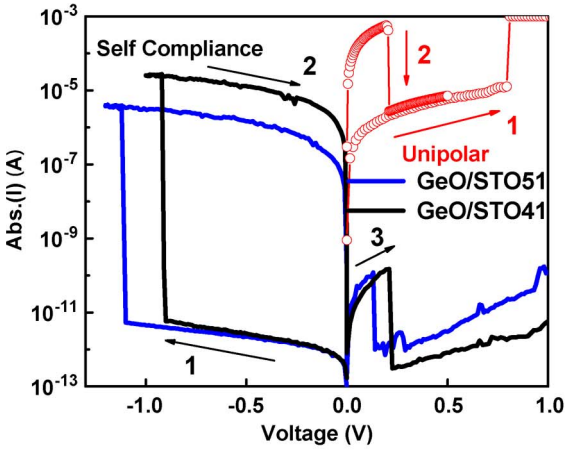
II. Experimental Procedure

The RRAM devices were fabricated on standard Si wafers. To permit VLSI backend integration, the process began with a 200-nm-thick SiO_2 layer on Si substrates. Then, 100-nm TaN was deposited by physical vapor deposition (PVD). After patterning the bottom TaN electrode, 12-nm-thick $SrTiO_3$ (STO) films with different Ar/O_2 ratios of STO41 $(Ar/O = 4/1)$ or STO51 $(Ar/O = 5/1)$ were deposited on $TaN/SiO_2/Si$ using PVD. After that, 8-nm-thick GeO_2 was deposited. Finally, 25-nm-thick Ni was deposited and patterned as top electrode by a metal mask with an area of 11 300 μm^2. For comparison, a Ni/STO/TaN device was also made. Here, the Ni provides a low-cost solution for high-work-function (5.1 eV) electrode, which has been implemented by high-κ DRAM capacitors [14].

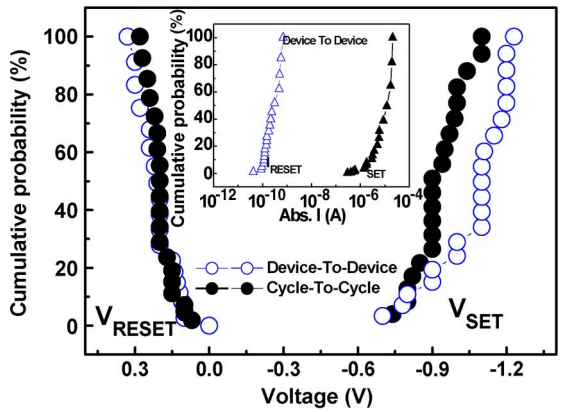
III. Results and Discussion

Fig. 1 shows the swept I–V curves of control Ni/STO/TaN RRAM. Good bipolar resistive switching characteristics were measured, where a large resistance window of 10^3 at -0.2 V is obtained. However, the very high 0.3-mA set current at -2 V is the basic limitation for the conventional STO RRAM.

To improve the device characteristics, the stacked Ni/GeO/STO/TaN RRAM devices were formed. As shown in Fig. 2(a), a very low self-compliance set current of 3.5 μA at -1.1 V (4 μW) and a large resistance window are reached at -0.2 V readout. The device can be reset from LRS to high-resistance state (HRS) at a very low voltage of only 0.13 V with an ultralow reset current of 0.12 nA (16 pW) that can be driven by a diode at reverse bias. The resistance window



(a)



(b)

Fig. 2. (a) Swept I–V curves of stacked Ni/GeO/STO/TaN RRAM devices with different oxygen-concentration STOs (STO41 and STO51). (b) $V_{\rm SET}$ and $V_{\rm RESET}$ distributions of RRAM devices. The inset shows the $I_{\rm SET}$ and $I_{\rm RESET}$ distributions.

depends strongly on the deposition condition: Even larger HRS/LRS of 3×10^6 is obtained under oxygen-deficient STO (STO51). This result indicates that the oxygen concentration in STO plays an important role in stacked GeO/STO RRAM. It is important to notice that this novel RRAM is different from the conventional unipolar mode that is also obtainable in the same device, as shown in Fig. 2(a), under a 3-V forming process and 1-mA current compliance. However, the high set current and high current compliance require a large size transistor to drive this unipolar mode RRAM. Although detailed mechanism of asymmetry in the I– V curve at $|V| < 0.1$ V is still under study, it may be related to the higher resistance by electron injection from TaN before completely resetting to HRS. The stacked Ni/GeO/STO/TaN RRAM devices have tight set/reset voltage distributions from cycle-to-cycle and device-to-device measurements shown in Fig. 2(b), which may be due to the hopping conduction explained in the following section. The stable set/reset current distributions in the inset of Fig. 2(b) is ascribed to the self-compliance property and hopping mechanism explained in the following sections.

To analyze the record lowest switching power, the temperature-dependent I–V characteristics were measured at both HRS and LRS. As shown in Fig. 3, the very small HRS current fits well the Schottky emission via high-work-function

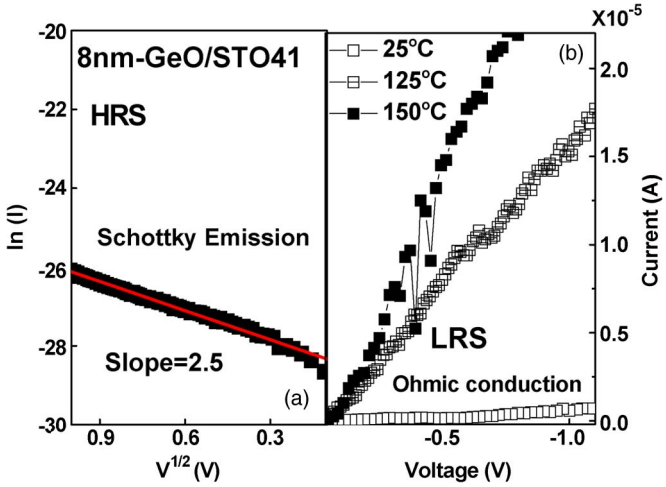
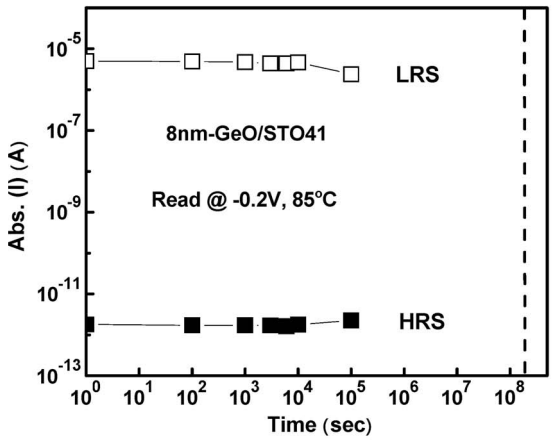
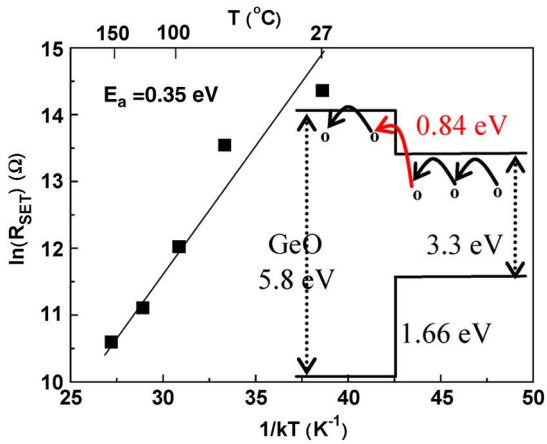


Fig. 3. I–V curves of HRS and LRS by fitting with Schottky emission and ohmic conduction mechanism, respectively.



(a)



(b)

Fig. 4. (a) Retention performance of Ni/GeO/STO/TaN RRAM devices. (b) LRS resistance as a function of temperature. The inset shows the energy band diagram and hopping conduction via GeO/STO.

Ni electrode and similar to MIM capacitors used for low leakage DRAM [14]. The current conduction at LRS follows the ohmic law, where current variation by trapping and detrapping is found and becomes more significant at higher temperatures.

The retention characteristics at 85 °C are shown in Fig. 4(a). A large memory window of 1×10^6 is measured for 10^5-s

TABLE I
COMPARISON OF DEVICE INTEGRITY DATA FOR VARIOUS RRAM DEVICES

Dielectric	Nb:STO [7]	Cu-MoO_X [8]	Al/PCMO [9]	NiO [4]	GeO/STO (This work)
T/B Electrode	Pt/Pt	Pt/Cu	Pt/W	Au/n-Si	Ni/TaN
I_{SET} @ V_{SET}	10mA @1V	100mA @2V	-1mA @-3V	0.6mA @3.9V	-3.5uA @-1.1V
I_{RESET} @ V_{RESET}	-10mA @-3V	-80mA @-1.5V	1uA @3V	5mA @1.4V	0.12nA @0.13V
On/Off Ratio	~10^2	15x	>10^2	~ 2x10^2	>10^5
Retention	2x10^6 @125°C	10^5 @85°C	10^5 @125°C	—	10^5 @85°C
$Power_{SET, RESET}$	10, 30mW	200, 120mW	3mW, 3uW	—	4uW, 16pW

retention at 85 °C. To further understand the potential mechanism, we have plotted the measured temperature-dependent resistance at LRS. As shown in Fig. 4(b), a negative TC is measured up to 150 °C and opposite to the positive TC in conventional metal-oxide RRAM [3]. Moreover, small SET/RESET currents are also obtained in the Ni/GeO/TaN RRAM device, where no metallic filament can be formed in covalent-bond GeO. This also supports the different conduction mechanisms from the conventional metallic filament. An activation energy of 0.35 eV is close to that of negative TC in highly defective Si ruled by hopping conduction [15], which suggests LRS mechanism to be related by hopping via defects in GeO/STO (inset). Since an improved device performance was reached at oxygen-deficient STO shown in Fig. 2(a), the main defects may be due to the positively charged oxygen vacancies [13]. Such weakly linked hopping conduction can be easily broken by injected electrons under a small voltage and leads to HRS, which is quite different from the large power to disrupt the metallic filament in metal-oxide RRAM. The hopping conduction also provides a large resistance [15] to reach a small self-compliance set current that is quite different from the large leakage current in conventional RRAM ruled by metallic filament.

Table I compares various RRAM devices. Our devices have merits of the lowest switching power and largest retention window ($> 10^5$) for multilevel cell.

IV. CONCLUSION

A low-cost covalent-bond-dielectric/metal-oxide Ni/GeO/STO/TaN RRAM has shown an excellent performance of ultralow 4-μW set and 16-pW reset power, and a large 10^6 memory window for 10^5-s retention at 85 °C, with small $4F^2$ size, capable of 3-D integration and simple process, and useful for embedded and stand-alone function.

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