An Extreme Surface Proximity Push for Embedded SiGe in pMOSFETs Featuring Self-Aligned Silicon Reflow

Da-Wen Lin, Chien-Liang Chen, Ming-Jer Chen, and Chung-Cheng Wu

***Abstract*—This letter proposes a novel process to modulate the distance, or proximity, between the tip of embedded silicon–germanium (e-SiGe) and the channel region in pMOSFETs. Traditionally, sophisticated etching treatment is adopted in a spacer structure; however, process-induced variation in the e-SiGe proximity may lead to serious variation in pMOSFET performance. In this letter, an extremely close proximity is achieved using self-aligned silicon reflow (SASR) in hydrogen ambient. As opposed to conventional approaches which have e-SiGe proximity determined by spacer width, the tip of e-SiGe with SASR can be positioned flush with the gate edge, as corroborated by both the TEM analyses and TCAD simulation. A significant improvement in pMOSFET performance is also measured.**

***Index Terms*—Embedded silicon–germanium (e-SiGe), MOSFET, reflow, self-aligned, strain.**

I. Introduction

DURING the past decade [1]–[12], embedded silicon–germanium (e-SiGe) has been widely utilized in modern CMOS technology with the aim to enhance pMOSFET performance. Not only can hole mobility benefit from lattice-induced mechanical strain but also source/drain series resistance $(R_{\rm sd})$ can be reduced with optimization of *in situ* doping techniques. Surface proximity push remains one of the most fundamental factors concerning the efficiency of e-SiGe. To address this issue, sophisticated etching treatment was adopted [6], [9]. However, as the tip of e-SiGe gets closer to the gate edge, the variation in proximity push resulting from the etching process is more pronounced, and in turn, the variation in strain and $R_{\rm sd}$ becomes more significant. In this letter, a novel technique featuring silicon reflow is instead adopted to produce an enhanced proximity push at the channel surface. Following an isotropic silicon-recess etch which creates a large curvature under a spacer structure, the silicon wafer is annealed in hydrogen ambient at a moderate temperature. This annealing process leads to silicon volume transfer, or reflow, [13]–[15] which can enlarge the top opening of the recessed profile while reducing the bottom region. Consequently, an undercut is formed beneath the spacer with an alignment to the gate edge. This leads to an extreme surface proximity push suitable for the subsequent e-SiGe epitaxy process. An improved $I_{\rm on}-I_{\rm off}$ performance is experimentally demonstrated on a 40-nm technology pMOSFET. In addition, improved drain-induced barrier lowering is obtained because of less e-SiGe encroachment in the bottom region. These analyses are supported by TEM photographs and TCAD simulation.

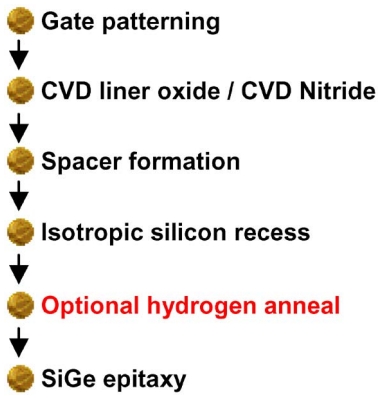

Fig. 1. Brief of process flow in the e-SiGe formation loop. An optional hydrogen annealing step is inserted before e-SiGe selective epitaxy process.

II. Silicon Reflow Experiment in Hydrogen Ambient

The undertaken process flow is briefly described in Fig. 1. After the gate patterning process, a spacer of ∼15 nm consisting of CVD oxide and nitride is formed. Silicon is then etched to form an isotropic recess. An optional hydrogen annealing step is performed before e-SiGe epitaxy process. During the hydrogen annealing process, the reflow of silicon occurs, particularly in the region where a large curvature exists. The silicon tends to reduce surface energy through a reduction in the curvature. It is believed that the CVD liner oxide and silicon are weakly bonded and can be separated during the hydrogen annealing process. In contrast, the gate oxide (thermally grown silicon oxide) and silicon substrate are strongly bonded. Silicon can therefore reflow with the aid of the hydrogen annealing process beneath the spacer, and this reaction will cease at the interface

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D.-W. Lin is with the Taiwan Semiconductor Manufacturing Company, Hsinchu 30078, Taiwan, and also with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan.

C.-L. Chen and C.-C. Wu are with the Taiwan Semiconductor Manufacturing Company, Hsinchu 30078, Taiwan.

M.-J. Chen is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan.

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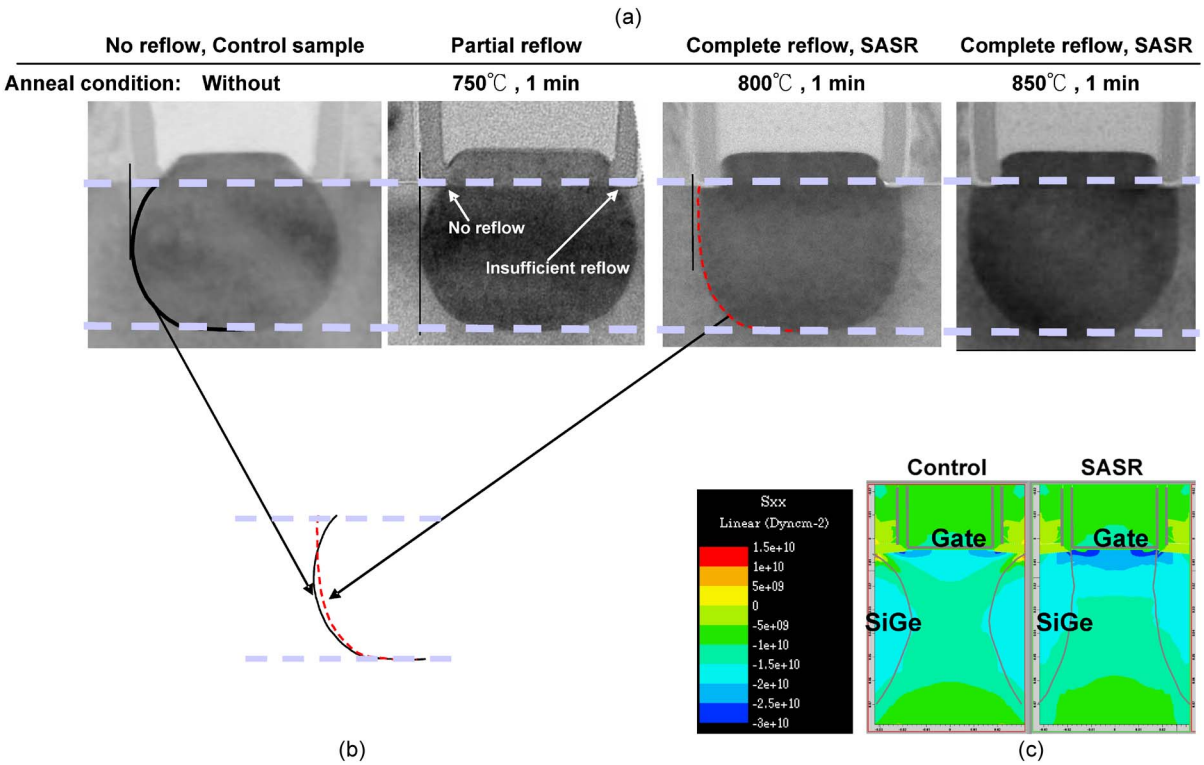

Fig. 2. (a) Cross-sectional TEM analyses of e-SiGe profile under different hydrogen annealing temperatures. Complete SASR occurs above a moderate temperature, which is 800 °C in this letter. A wide process window of annealing temperature is demonstrated. The hydrogen annealing time is 1 min for each process. (b) Comparison of e-SiGe contours between the control sample and SASR. SASR provides a closer proximity on the top and less e-SiGe encroachment at the middle and bottom regions. (c) Two-dimensional TCAD simulation of stress distribution along the channel direction. SASR provides higher compressive stress which improves hole mobility.

between silicon and gate oxide at an appropriate temperature. Fig. 2(a) shows the TEM results of silicon reflow under different annealing temperatures in the hydrogen ambient for 1 min. At a low annealing temperature (750 °C), insufficient and asymmetric silicon reflow under spacer is evident. An undercut is formed at one side between the gate and spacer edge, while no silicon reflow occurs at the other side. Under a moderate temperature (800 °C), the silicon reflows while stopping at the gate edge. With a 50 °C higher process temperature (850 °C), the interface between gate oxide and silicon does not split, and no further silicon reflow can occur. A self-aligned extreme e-SiGe surface proximity push with a large margin of process temperature is therefore achieved by exploiting a self-aligned silicon-reflow (SASR) technique. The contours of e-SiGe with and without SASR are schematically shown in Fig. 2(b). With SASR, the e-SiGe in the middle and bottom regions is pushed away from the gate edge due to the redistribution of silicon. Hence, a subsurface punch-through current can be suppressed, as will be discussed in the next section.

III. Device Analysis

TCAD simulation result is shown in Fig. 2(c), revealing a key advantage of SASR in strain engineering. The tip of the e-SiGe is pushed from the subsurface to the surface, thus reducing the e-SiGe proximity compared to the non-SASR case. The channel longitudinal compressive strain is increased by a factor of more than 15%, and thereby, a higher hole mobility in the channel region is expected.

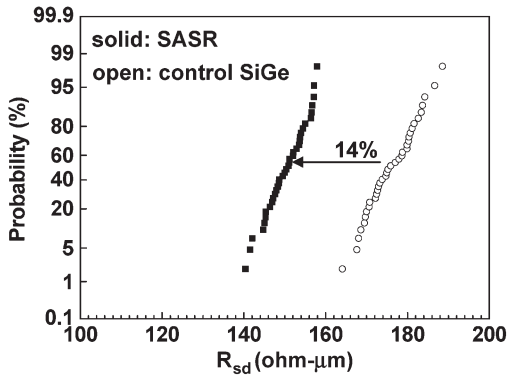

Fig. 3. SASR leads to lower source/drain series resistance. The tighter distribution implies that SASR mitigates the device variation resulting from the silicon-recess process.

In addition, since the hole mobility and boron doping activation level are higher in SiGe as compared to silicon, the use of SASR can lower the $R_{\rm sd}$, as long as the e-SiGe stays at the gate edge. Here, a 14% reduction of $R_{\rm sd}$ is obtained, as shown in Fig. 3, in terms of the statistical distribution with and without SASR, which is measured using the extraction method described in a previous work [16], [17]. The figure also clearly points out that a tighter distribution of $R_{\rm sd}$ is associated with SASR. This means that SASR can mitigate the process variation caused by isotropic silicon recess.

Unlike the conventional proximity push which may lead to potentially undesirable short-channel effect (SCE), SASR can actually resolve SCE because of less encroachment of e-SiGe in

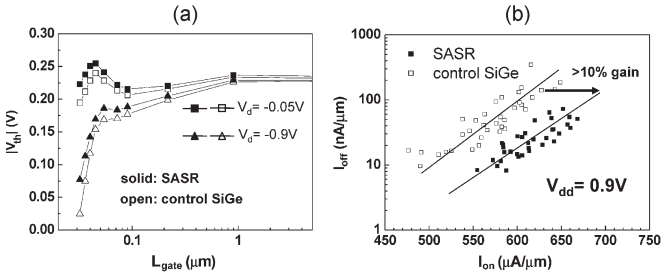

Fig. 4. (a) SASR leads to a better immunity against SCE because of a less e-SiGe encroachment in the middle and bottom regions. (b) More than 10% $I_{\rm on}-I_{\rm off}$ improvement is observed by implementing SASR.

the subsurface region, as shown in Fig. 2(b). This is confirmed by the measured threshold voltage versus gate length, as shown in Fig. 4(a). The figure shows that a higher degree of SCE suppression is achieved with the application of SASR. Finally, Fig. 4(b) shows the measured $I_{\rm on}-I_{\rm off}$ performance with and without SASR. Evidently, a more than 10% improvement is obtained with SASR, which can be attributed to the combination of the higher hole mobility and lower $R_{\rm sd}$, as mentioned earlier. The variation in $I_{\rm on}-I_{\rm off}$ performance is also significantly reduced in the presence of SASR.

IV. Conclusion

An integration-friendly and cost-effective process used for strain engineering, called SASR, has been, for the first time, highlighted in this letter. Owing to the nature of SASR in the hydrogen ambient, an extreme surface proximity push has been achieved without using sophisticated etching process. SASR is proven stable in a wide range of process temperatures, which is highly desired in the advanced CMOS manufacturing. A significant improvement in the device performance is experimentally demonstrated, along with the corroborative evidence in terms of the TEM pictures and TCAD simulation.

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