J Infrared Milli Terahz Waves (2010) 31:1063–1074
DOI 10.1007/s10762-010-9664-6

Wideband Matched CMOS LNA Design Using R-L-C Loading Network

Hui-I Wu · Qi-Yuan Horng · Robert Hu · Christina F. Jou

Received: 20 July 2009 / Accepted: 1 June 2010 /
Published online: 22 June 2010

Abstract This paper proposes a new methodology for designing and analyzing wideband matched CMOS LNA with *R-L-C* loading network, where validity of this new approach is supported by the agreement between the simulated input impedance of the LNA and its calculated counterpart. To demonstrate its feasibility, two wideband matched LNA's are designed using TSMC 0.18-μm RF-CMOS process. One is for 3–8 GHz application and the second one targets at 8–25 GHz frequency range. The measured results of both circuits will then be presented.

Keywords Wideband · Input matching · Low noise amplifier · LNA

1 Introduction

Wide-band low-noise amplifiers (LNA's) have been a critical component for both scientific community and the communication industry, such as radio astronomy receivers for the former and ultra-wideband (UWB) technologies for the latter [1–3]. Among the different circuit design methodologies proposed for wideband amplifiers, the distributed one is probably the most straightforward in realizing broad bandwidth [4, 5]. However, it tends to consume a lot of power while providing only modest gain. An amplifier using common-gate transistor as input stage can indeed have wideband matched impedance; nonetheless, the resulting circuit will have poor power gain and large noise figure [6]. Adding a delicate *L-C* circuit in front of the amplifier can improve its input matching over a wide bandwidth, but at the cost of additional noise generated by these passive components and, especially in the case of silicon, this deterioration is pronounced [7–9]. Recently, it becomes popular

H.-I. Wu (✉) · Q.-Y. Horng · C. F. Jou
Department of Communication Engineering, National Chiao Tung University,
1001 University Road, Hsinchu, Taiwan 300, Republic of China
e-mail: huiiwuhuiiwu@gmail.com

R. Hu
Department of Electronics Engineering, National Chiao Tung University,
1001 University Road, Hsinchu, Taiwan 300, Republic of China

applying current re-use method in designing wideband CMOS amplifiers; however, the stacking of one n-type and one p-type transistors requires a large bias voltage [10, 11].

In the case of high mobility transistor (HEMT), it has already been demonstrated that through the intrinsic gate-drain capacitor C_{gd}, the transistor's output *R-C* loading can alter its input impedance to the intended value over a wide bandwidth [12]. In spite of that, implementation of this large loading equivalent resistance is not that easy in the CMOS circuit. Thus, the input matching mechanism for wideband matched COMS LNA needs to be re-examined and modified if necessary, and that prompts the research described in this paper.

In the following section, after a brief review of the 0.18-μm RF-CMOS transistor's small-signal modeling, we propose what should constitute the first-stage transistor's loading: L_d, R_d, and C_d, as shown in Fig. 1, where L_d is an explicit element, and both R_d and C_d can be from the equivalent input circuit of the following-stage. Physically, the external source inductor L_s is critical in determining the low-frequency input matching, and the loading L_d starts playing a role as frequency increases. In both cases, C_d is used for setting Re[Z_{in}], and proper choice of R_d helps lowering S_{11} at high frequency. If the high frequency range means infinite, then L_d can indeed be omitted; otherwise, the importance of this L_d cannot be overlooked for finite-bandwidth wideband LNA, as this L_d could improve the input matching at the intended high frequency range. Without inserting any complicated passive (and lossy) circuit in front of the first-stage transistor, superior noise performance is expected for this type of amplifier.

A 3–8 GHz LNA is therefore fabricated using TSMC (Taiwan Semiconductor Manufacturing Company) 0.18-μm RF-CMOS process. To explore the high frequency performance of this commercial process, a second LNA targeting the 8–25 GHz frequency range is then designed. Measured results of both amplifiers will be presented too.

2 Analysis of wideband LNA design

To facilitate the circuit analysis, *S*-parameters of a TSMC 0.18-μm RF-CMOS transistor need to be numerically fitted to find its equivalent small-signal model, as shown in Fig. 2, where the substrate effect due to C_{sub} and R_{sub} has been included. For this 216-μm 27-finger n-type transistor biased at V_{gs}=0.65 Volt and I_d=7 mA, our model is valid up to 20 GHz at least, and

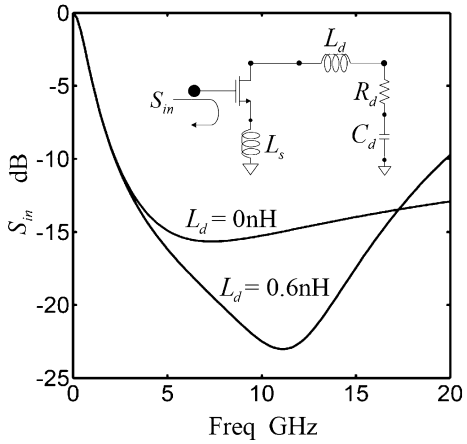

Fig. 1 The simulated input reflection coefficient S_{in} of the proposed transistor circuit with L_d=0 and 0.6nH, respectively, while C_d=0.13pF, R_d=25Ω, and L_s=0.3nH.

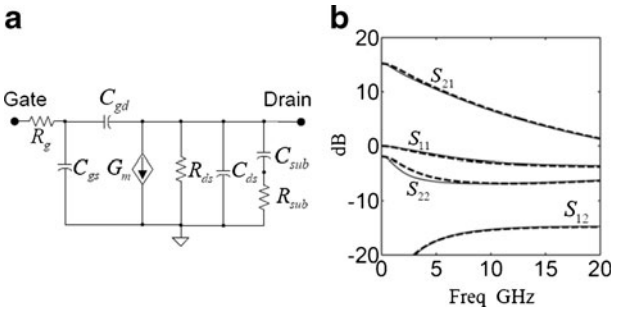

Fig. 2 **a** Small-signal model of a TSMC 0.18-μm RF-CMOS transistor biased at saturation region. **b** Simulated *S*-parameters from both the foundry provided design kit (solid lines) and our small-signal model (dashed lines).

the parameter values are tabulated in Table 1. Though *S*-parameter discrepancies can be observed with the omission of R_g, C_{ds}, R_{sub}, and C_{sub} , they are relatively minor; thus, to retain the physical meaning while simplifying the mathematical derivation, these four parameters are removed from that used in the following circuit analysis.

Mathematically, the input impedance Z_{in}, as indicated in Fig. 3, can be expressed as

$$Z_{in} = \left[Y_\alpha + \frac{1}{Z_\beta} \right]^{-1} \tag{1}$$

where Y_α is the admittance looking into the C_{gd} branch, and Z_β is the impedance looking into the C_{gs} branch. Both Y_α and Z_β can be derived as

$$\begin{aligned} Y_\alpha = & \left[\frac{1}{j\omega C_{gd}} + \frac{1}{j\omega C_d} + R_d + j\omega L_d \right]^{-1} + \left[\left(\frac{1}{j\omega G_m R_{ds} C_{gd}} + \frac{1}{G_m} + j\omega L_s \right) \right. \\ & + \left(\frac{1}{C_d / G_m C_{gd} + C_{gd} / j\omega L_s C_d} + \frac{1}{1 / j\omega G_m R_d C_{gd} + L_s / R_d C_{gd}} \right. \\ & \left. \left. + \frac{1}{L_s / j\omega C_{gd} L_d - 1 / \omega^2 L_d C_{gd} G_m} \right)^{-1} \right]^{-1} \end{aligned} \tag{2}$$

and

$$Z_\beta = \frac{1}{j\omega C_{gs}} + \frac{G_m L_s}{C_{gs}} + j\omega L_s \tag{3}$$

The corresponding equivalent circuit can be arranged as that of Fig. 4, where Y_α is the dominant branch and Z_β offers some modification [12]. Again, it is the C_d that determines

Table 1 Parameters in the small-signal model of the 216-micron 27-finger tsmc n-type transistor.

V_{gs}=0.65 Volt, I_d=7 mA

parameter	value	parameter	value
R_g	7Ω	C_{sub}	0.3pF
R_{ds}	452Ω	C_{ds}	0.063pF
R_{sub}	180Ω	C_{gd}	0.08pF
G_m	64mS	C_{gs}	0.2pF

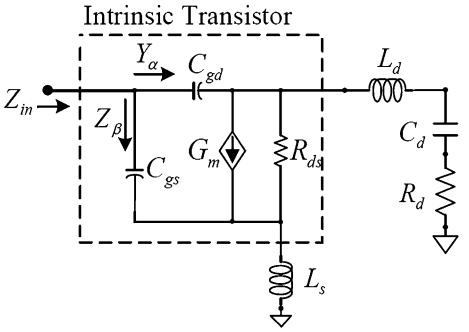

Fig. 3 The proposed transistor circuit used in the wideband analysis.

the matched Re[Z_{in}] (= C_d/G_mC_{gd}), as discussed in detail in [12]. With appropriate component values, the shape of the input reflection coefficient S_{in} resembles a hook, as shown in Fig. 5. The solid curve is the simulated result with C_d=0.13pF, R_d=25Ω, L_d= 0.6nH, and L_s=0.3nH; the overlapping dashed curve is the calculated counterpart using (1). On the S_{in} trajectory, there are two marked frequency points where the corresponding input impedance is purely real and close to 50Ω, and thus are good indices for this circuit's (slightly larger) available frequency range. By setting Im[Y_α] to zero, both f_L and f_H can be determined as

$$f_L = \frac{1}{2\pi\sqrt{L_s(C_{gd}+C_d)G_mR_{ds}}} \tag{4}$$

and

$$f_H = \frac{1}{2\pi\sqrt{(L_s+L_d)C_d}} \tag{5}$$

The calculated f_L and f_H are 4.09 GHz and 13.24 GHz in this case, and are very close to the simulated 5 GHz and 12.8 GHz, respectively. Apparently, with C_d used in determining Re[Z_{in}], f_L can now be set by L_s while f_H could be manipulated by L_d. Fig. 6 shows the simulated input reflection coefficient with different L_s, where curves 1–3 have L_s=0.3, 0.4, and 0.5nH, and all have their C_d=0.13pF, R_d=25Ω, and L_d=0.6nH. Fig. 7 illustrates the impact of L_d on S_{in}, where curves 1–3 are with L_d=0.3, 0.6, and 0.9nH, and all have their C_d=0.13pF, R_d=25Ω, and L_s=0.3nH. Figure 8 shows the simulated S_{in} with different R_d,

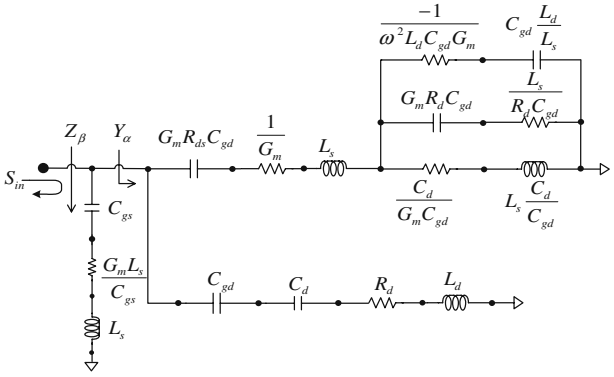

Fig. 4 Equivalent input schematic of the proposed transistor circuit. Y_α is the admittance looking into C_{gd} branch, Z_β is the impedance looking into C_{gs} branch, and S_{in} is the overall input reflection coefficient.

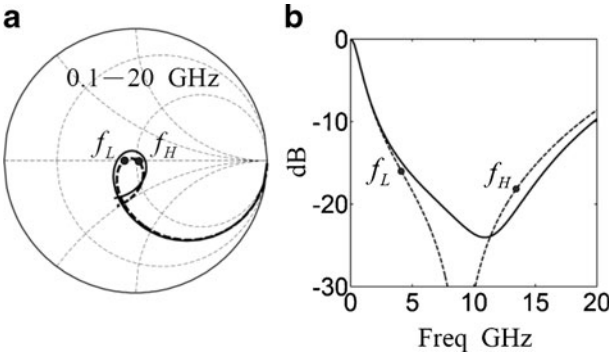

Fig. 5 Calculated and simulated input reflection coefficient of the proposed transistor circuit. **a** The solid curve on the Smith chart is the simulated result while the dashed curve is its calculated counterpart. Here f_L and f_H are the resonant low- and high-frequency points. **b** The same results expressed in dB vs. frequency.

where curves 1–3 have R_d=25, 45, and 65Ω, and all have their C_d=0.13pF, L_s=0.3nH, and L_d=0.6nH. Intuitive understanding of this matching mechanism can now be best described as follow:

(a) $f<f_L$: As series $R_dL_dC_d$ tends to be open-circuit at very low frequency and the effect of L_s is very small in this frequency range, the transistor's loading is now dominated by channel resistance R_{ds} (= 452Ω). The resulting Miller capacitance $G_mR_{ds}C_{gd}$ (= 2.31pF) puts the location of S_{in} in the capacitive region of the Smith chart. As frequency increases, the real part of input impedance will start to be affected by the loading C_d, as Re[Z_{in}] = C_d/G_mC_{gd}. The S_{in} trajectory can be determined by C_d and moves along the constant resistance circle in the capacitive region [12].

(b) $f_L \leq f < f_H$: As frequency continues to increase, the inductive voltage induced by L_s at the input is becoming more obvious, thus the inductive components of Z_{in} (originating from L_s) will resonate out the aforementioned Miller capacitance $G_mR_{ds}C_{gd}$. On the Smith chart, S_{in} will now pass-by the zero point and enter the inductive region; therefore, it is apparently that f_L can be set by L_s. Since the loading resistor R_d (= 25Ω) can also generate a small Miller capacitance $G_mR_dC_{gd}$ (= 0.125pF), a further bending of the still-inductive S_{in} on the Smith chart can be observed in this frequency range.

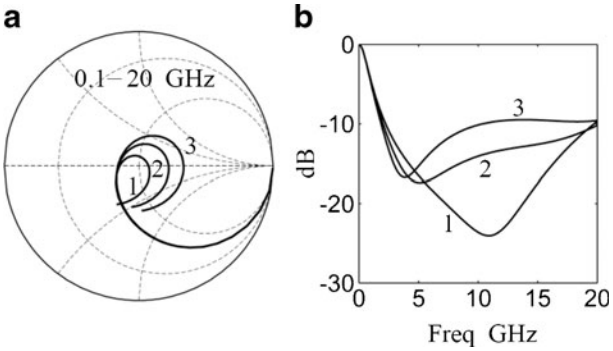

Fig. 6 Simulated input reflection coefficient of the wideband transistor circuit with different values of L_s. **a** On the Smith chart, curves 1–3 correspond to L_s=0.3, 0.4, and 0.5, respectively, while C_d=0.13pF, R_d=25Ω, and L_d=0.6nH. **b** The same results expressed in dB vs. frequency.

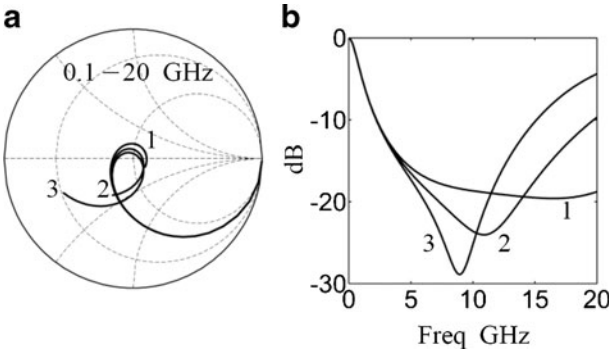

Fig. 7 Simulated input reflection coefficient of the wideband transistor circuit with different values of L_d. **a** On the Smith chart, curves 1–3 correspond to L_d=0.3, 0.6, and 0.9nH, respectively, while C_d=0.13pF, R_d=25Ω, and L_s=0.3nH. **b** The same results expressed in dB vs. frequency.

(c) $f \geq f_H$: When the inductor L_d begins to resonate out C_d, the loading circuit can be approximated as R_d at the resonance frequency; therefore, Z_{in} is predominated by the corresponding Miller capacitance $G_m R_d C_{gd}$, which means S_{in} on the Smith chart can be easily dragged into the capacitive region. A complete loop around the zero point is now constructed and we know that f_H can be changed by L_d. If the high frequency range means infinite, this L_d can indeed be omitted; otherwise, the importance of this L_d cannot be ignored in the case of finite-bandwidth wideband LNA. Thus far, the roles played by C_d, L_s, L_d, and R_d in achieving wideband input matching are well explained and can be easily understood.

3 Wideband LNA design

With the wideband matching mechanism fully analyzed, two CMOS LNA's, one covers the more common 3–8 GHz as an initial verification and the other the more challenging 8–25 GHz for exploring this type of circuits' potential and limitation, are designed and fabricated using TSMC 0.18-μm RF-CMOS process. Both the *S*-parameters and noise

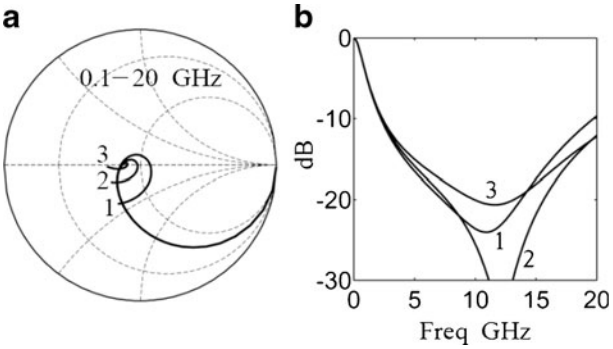

Fig. 8 Simulated input reflection coefficient of the wideband transistor circuit with different values of R_d. **a** On the Smith chart, curves 1–3 correspond to R_d=25; 45, and 65Ω, respectively, while C_d=0.13pF, L_s=0.3nH, and L_d=0.6nH. **b** The same simulated results in dB vs. frequency.

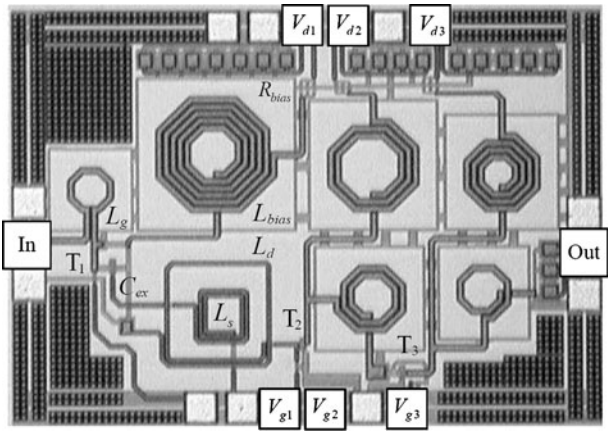

Fig. 9 Photograph of the 3–8 GHz LNA. The chip size is 1400×1000 μm^2. T_1, T_2, and T_3 are the three transistors.

figures of these two circuits are measured on-wafer at room temperature. Description of the circuits and their measured results will be presented below.

Figures 9 and 10 are the photograph and schematic of the 3–8 GHz LNA. It is mainly the 1nH source inductor L_s, 1.5nH inter-stage L_d, and 0.2pF loading capacitor C_d, that contribute to the wideband input matching. The coupling between L_s and L_d allows the reduction of the chip size. To reduce its power consumption, a slightly smaller transistor is used for the first stage. To ensure that the equivalent C_{gd} is still sufficient to sustain the wideband matching mechanism, an external capacitor C_{ex} is added. The large inductor L_{bias} on the drain branch is for DC bias purpose and has small impact on S_{11} in 3–8 GHz. Since this L_{bias} tends to introduce a negative Re[Z_{in}] at very low frequency, R_{bias} is used to stabilize this amplifier.

Figure 11 shows the measured and simulated *S*-parameters of this 3–8 GHz LNA where the both the S_{11} and S_{22} are below -10dB, S_{21} around 15dB, and S_{22} far below -20dB. For each measured scattering parameter, there are two simulated counterparts, technically SS and TT corners, to account for the inevitable process variation. The bias is set at V_{d1} = 1V and I_{d1}=9.5 mA for the first-stage transistor, V_{d2} = 1V and I_{d2}=7.5 mA for the second stage, and V_{d3} = 1V and I_{d3}=7.4 mA for the last stage. Figure 12 shows the same S_{11} and S_{22} on the Smith chart, and both resemble the familiar wideband hook shape. Figure 13

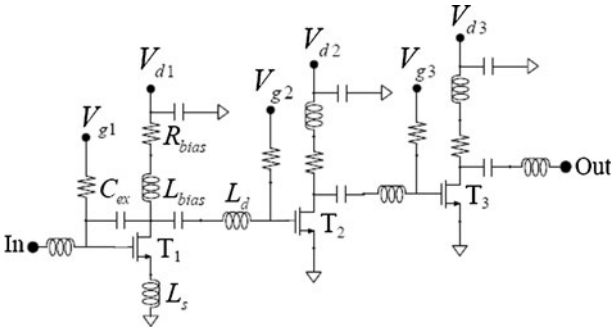

Fig. 10 Schematic of the 3–8 GHz LNA.

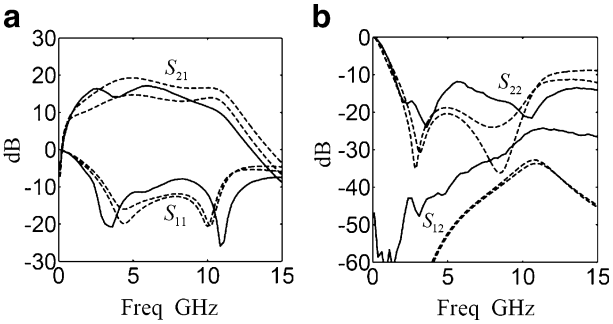

Fig. 11 Measured and simulated *S*-parameters of the 3–8 GHz wideband LNA. **a** S_{21} and S_{11} where the solid curves are the measured results and the dashed curves are their simulated counterparts in two circumstances. **b** S_{12} and S_{22}.

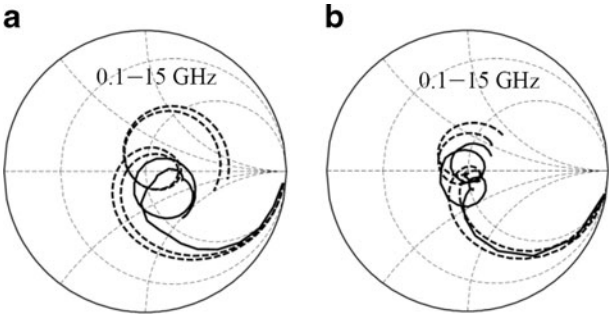

Fig. 12 Measured and simulated S_{11} *and* S_{22} of the 3–8 GHz wideband LNA on the Smith chart. **a** The solid curve is the measured S_{11} and the two dashed curves are the simulated counterparts. **b** Measured and simulated S_{22}.

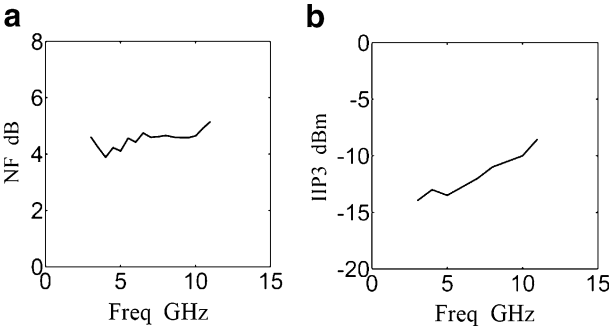

Fig. 13 The measured noise figure and IIP3 of the 3–8 GHz wideband LNA. **a** Noise figure. **b** IIP3.

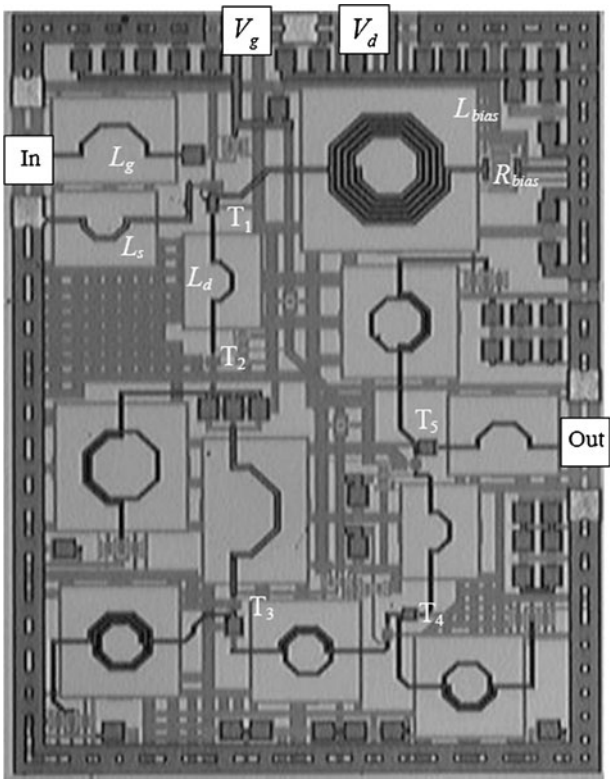

Fig. 14 Photograph of the 8–25 GHz CMOS LNA. The chip size is 945×1245 μm^2. T_1, T_2, T_3, T_4, and T_5 are the five transistors.

shows the measured noise figure and the linearity (IIP3) of this circuit. The total power consumption of this amplifier is 24.4mW.

Figures 14 and 15 are the photograph and schematic of the 8–25 GHz five-stage LNA where the design methodology is similar to that of the 3–8 GHz one. To simplify the bias

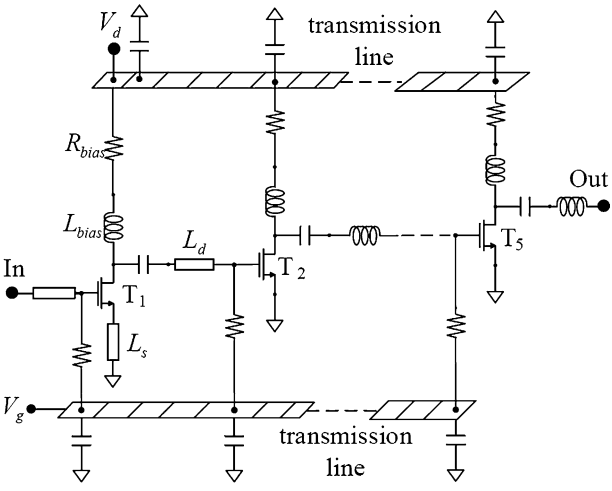

Fig. 15 Schematic of the 8–25 GHz CMOS LNA. There is only one drain bias and one gate bias needed for this 5-stage circuit.

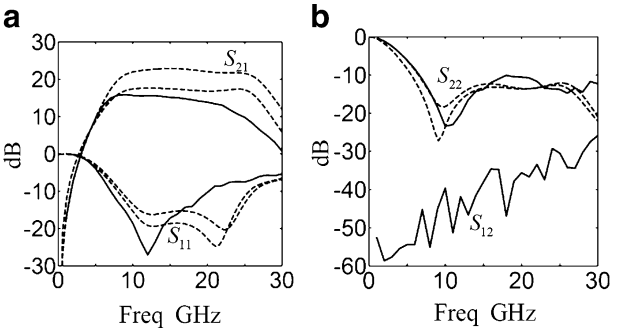

Fig. 16 Measured and simulated *S*-parameters of the 8–25 GHz wideband LNA. **a** Measured (solid) and simulated (dashed) S_{21} and S_{11}. **b** Measured and simulated S_{12} and S_{22}.

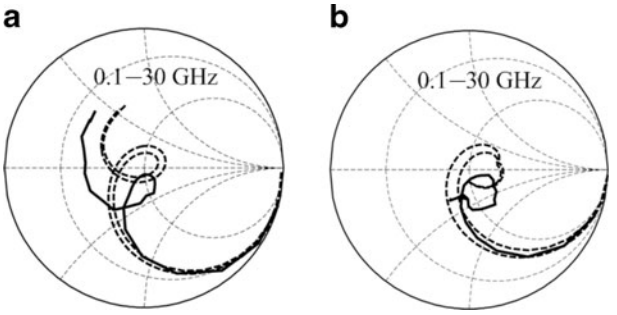

Fig. 17 Measured and simulated S_{11} *and* S_{22} of the 8–25 GHz wideband LNA on the Smith chart. **a** The solid curve is the measured S_{11} and the dashed curves are the simulated counterparts. **b** Measured and simulated S_{22}.

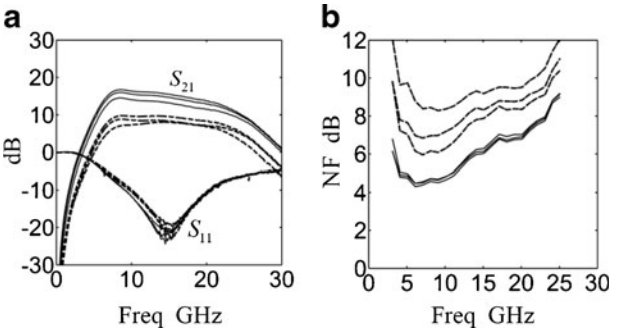

Fig. 18 Measured S_{21}, S_{11} and noise figure of the 8–25 GHz LNA. **a** Measured S_{21} and S_{11} where the solid curves are with V_d = 2V, I_d is 37, 50, and 62 mA; the dashed curves are with V_d = 1V, I_d is 31, 42, and 53 mA, **b** Measured noise figure with V_d = 2V (solid) and V_d = 1V (dashed) with different bias current.

scheme, only one drain bias and one gate bias are used. Isolation along the common drain bus between each stage is provided by the long transmission lines that surround the periphery of this chip. A small chip size of 945×1245 μm^2 can thus be obtained. With V_d= 1.8V and I_d=62 mA, both the measured and simulated S_{11} and S_{22} are below -10 dB, S_{21} around 15 dB, and S_{22} far below -20dB, as shown in Figs. 16 and 17. Apparently, an increase of the input inductor by the use of bond-wire can easily move the S_{11} loop upward on the Smith chart and surround the zero point, therefore, lowers the input reflection coefficient further. The total power consumption is 112mW. To explore this circuit's performance under different bias conditions, Fig. 18 shows the measured input reflection coefficient, gain, and noise figure at different bias conditions where the solid curves are at V_d = 2V, I_d is 37, 50, and 62 mA; the dashed curves are with V_d = 1V and I_d is 31, 42, and 53 mA, respectively.

4 Conclusion

In this paper, the input matching technique for common source wideband LNA design has been thoroughly analyzed. The agreement between the simulated input impedance of the LNA and its calculated counterpart confirms the accuracy of our analysis. To demonstrate its wideband potential, both the 3–8 GHz and 8–25 GHz low noise amplifiers using TSMC 0.18-μm RF-CMOS process are designed, fabricated and measured.

Acknowledgment The authors are very grateful for the support of the National Chip Implementation Center (CIC), Hsinchu, Taiwan, R.O.C., for chip fabrication and high frequency measurement.

References

1. WPAN High Rate Alternative PHY Task Group 3a (TG3a), IEEE 802.15, 2007 [Online]. Available: http://www.ieee802.org/15/pub/TG3a.html
2. N. R. Erickson, R. M. Grosslein, R. B. Erickson, and S. Weinreb, "A cryogenic focal plane array for 85–115 GHz using MMIC preamplifiers," IEEE Trans. Microwave. Theory Tech. 47(12), 2212–2219 (1999), Dec.
3. N. Wadefalk, *et. al.*, "Cryogenic wide-band ultra-low noise IF amplifiers operating at ultra-low DC power," IEEE Trans. Microwave Theory Tech. 51(6), 1705–1711 (2003), Jun.
4. X. Guan and C. Nguyen, "Low-power-consumption and high-gain CMOS distributed amplifiers using cascade of inductively coupled common-source gain cells for UWB systems," IEEE Trans. Microwave Theory Tech. 54(8), 3278–3283 (2006), Aug.
5. P. Heydari, "Design and Analysis of a Performance-Optimized CMOS UWB Distributed LNA," IEEE J. Solid-State Circuits. 42(9), 1892–1904 (2007), Sept.
6. L. Yang, K. S. Yeo, A. Cabuk, J. Ma, M. A. Do, and Z. Lu, "A novel CMOS low-noise amplifier design for 3.1-to 10.6-GHz ultra-wide-band wireless receivers," IEEE Trans. Circuits Syst. I. 53(8), 1683–1692 (2006), Aug.
7. A. Ismail and A. Abidi, "A 3–10-GHz low-noise amplifier with wideband LC-ladder matching network," IEEE J. Solid-State Circuits, 39(12), 2269–2277 (2004), Dec.
8. A. Bevilacqua, C. Sandner, A. Gerosa, and A. Neviani, "A fully integrated differential CMOS LNA for 3–5-GHz ultrawideband wireless receivers," IEEE Microwave Wireless Compon. Lett. 16(3), 134–136 (2006), Mar.
9. Y.-J. E. Chen and Y.-I. Huang, "Development of Integrated Broad-Band CMOS Low-Noise Amplifiers," IEEE Trans. Circuits Syst. I. 54(10), 2120–2127 (2007), Oct.

10. C.-T. Fu, and C.-N. Kuo, "3~11-GHz CMOS UWB LNA using dual feedback for broadband matching," in IEEE Radio Frequency Integrated Circuits Symp. Dig., San Francisco, California, pp. 67–70, 2006.
11. C.-T. Fu, C.-L. Ko, C.-N Kuo, and Y.-Z. Juang, "A 2.4–5.4-GHz Wide Tuning-Range CMOS Reconfigurable Low-Noise Amplifier," IEEE Trans. Microwave Theory Tech. 56(12), 2754–2763 (2008), Dec.
12. R. Hu, "Wide-band matched LNA design using transistor's intrinsic gate-drain capacitor," IEEE Trans. Microwave Theory Tech., 54(3), 1277–1286 (2006), Mar.