The Ballistic Transport and Reliability of the SOI and Strained-SOI nMOSFETs with 65nm Node and Beyond Technology

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Abstract- In this paper, the device performance in terms of its transport charactertitics and reliability of the MOS devices on the SOI and strained-SOI have been examined. *For the first time*, both the transport and reliability characteristics have been established from experimental SOI and SSOI nMOSFETs. It was characterized by two parameters, the ballistic efficiency and the injection velocity. Experimental verifications on nMOSFETs with both technologies with tensile-stress enhancement have been made. For **SSOI devices**, it shows the expected drain current enhancements. For the **reliability evaluations**, SOI shows a smaller lattice such that it exhibits a much worse hot carrier (HC) reliability, while SSOI device shows a poorer interface quality verified from the FN-stress experiment. In general, although SSOI exhibits a worse interface quality while its reliability is much better than that of SOI's. Moreover, SSOI device shows a very high injection velocity as a result of the high strain of the device which makes it successful for drain current enhancement.

Introduction- As device channel length continues to scale beyond 90nm, high-k or strained technology can extend its scalability. For the latter, recent efforts have been paid on the strain engineering [1-2], hybrid substrate technology [3-4], and process-induced strain [5] of CMOS devices. From the scattering theory [6], the two fundamental transport parameters, the **ballistic efficiency** and the **carrier injection velocity** from the source side, are strongly related to the strain techniques. On the other hand, none has been reported on the ballistic transport of SOI and SSOI devices.

In this paper, the drain current enhancement of SOI and SSOI devices will be presented. Verifications of the reliabilities will also been demonstrated. A general rule will be provided on which technology is more reliable and with high performance.

I. Device Preparation

SSOI device, as shown in Fig1, is built in a thin (70nm) top silicon film isolated from the substrate by buried oxide (145nm) in UMC 65nm SSDOI technology, and at the same time, biaxial tensile strain in the thin film is formed.[1] Moreover, for NMOS performance enhancement, CESLs are used to give uniaxial tensile strain. The device has 14Å (physical thickness) SION gate oxide. Devices with gate length from 65nm to 0.2um have been used. The control SOI devices were also made for comparison.

II. Results and Discussion

The drain current for a device in the ballistic regime is governed by

$$I_{dsat} = WC_{eff}V_{inj}B_{sat}(V_G - V_T) \quad (1)$$

where V_{inj} and B_{sat} are the injection velocity and the ballistic efficiency respectively. B_{sat} is further related to the backscattering or reflection coefficient, r_c, by $B_{sat} = (1 - r_c)/(1 + r_c)$ [2]. As illustrated in Fig. 2, a smaller r_c (or a larger B_{sat}) is desired since a larger r_c will reduce the drain current. Also, the larger the value of V_{inj} is the more enhancements the device gains. These two critical parameters B_{sat} and V_{inj} are dependent on the device structure, strain engineering etc.

A. Ballistic transport behavior in SSOI and SOI nMOSFETs

Table 1 shows the formulas to experimentally determine B_{sat} and V_{inj}. First, comparing SSOI nMOSFETs (SSOIs) and SSOI nMOSFETs (SOIs) in drain current enhancements, we found an average improvement of 22% for SSOIs from long to short channel devices, given in Fig. 3. Furthermore, Fig. 4 shows the I_{on}-I_{off} results between SSOIs and SOIs. It indicates SSOIs gain more than ~12.5% over SOIs. The ballistic transport behavior between SSOIs and SOIs, and the critical parameters, V_{inj}, B_{sat}, and ••• •••ratio, are then calculated in Fig. 5, Fig. 6, and Fig. 7, respectively. Fig. 5 indicates that injection velocities of SSOI short-channel nMOSFETs are much larger than those of SOIs. But, on other hand, in Fig. 6, B_{sat} is not enhanced very much in SSOI short-channel nMOSFETs. From this result, we see that SSOIs are subjected to worse channel interface quality than SOIs such that B_{sat} cannot be improved effectively. As a consequence, we conclude that ***SSOI nMOSFETs gains current enhancements owing to the injection velocity but not ballistic efficiency.***

B. Reliability Issues in SSOI and SOI nMOSFETs

As described above, we realize that bad channel interface quality might be an important issue in SSOI. To prove this, first I_DV_G-on and off curves are measured in Fig 8. During off-condition (V_{DS}=0.05V), SSOIs are smaller than SOIs, on the contrary, for on-condition(V_{DS}=1V), SSOIs are much enhanced than SOIs ones. Next, simulation results of the channel current density are shown in Fig. 9. Fig. 9 shows that, for off-condition, Fig. 9(b), the carriers transport close to the interface. In contrast, for on-condition, Fig. 9(c), the carriers transport far away from the interface. As an outcome of Fig. 8 and Fig. 9, for off-condition, the interface between channel and insulator is a dominant factor to the transport, thus the curve of SSOIs is degraded instead of enhanced due to bad interface quality. Furthermore, to understand the interface quality, SSOIs and SOIs are stressed by FN-stress and HC-stress. The results are shown in Fig. 10 and Fig. 11. After HC stress, SOI exhibits a much larger degradation, but after FN stress, SOI shows less degradation. On the other hand, for SSOIs after FN stress, the curves are seriously degraded than those after HC stress. Moreover, Fig. 12 shows the Chare Pumping (CP) currents for SOIs and SSOIs. It reveals that CP current level of SOIs after HC stress is higher than that after FN stress. For SSOIs, after FN stress, CP current is larger than that after HC stress. We may confirm that ***SSOIs exhibit severe damage after FN stress. In other words, SSOIs own much worse channel interface quality. This is why ballistic efficiency cannot be improved.*** Finally, impact ionization rates of SSOIs and SOIs are shown in Fig. 13. The impact ionization rate of SOIs is much higher than that of SSOIs. This can be explained that the lattice constant of SOIs, Fig. 14(a), is smaller than that of SSOIs, Fig. 14(b). The smaller the lattice constant is, the higher probability the impact ionization rate is, i.e., a larger hot-carrier effect.

A summarized result of the new results of SSOI devices and previous works is drawn in a roadmap as shown in Fig. 15 for V_{inj}. This is the first and complete roadmap which has been reported. From V_{inj} roadmap, in this work, SSOI nMOSFETs exhibits very high V_{inj} and reaches into the thermal limit region. While, we also show that SSOI nMOSFETs cannot enhance B_{sat} as a result of poorer interface. Moreover, in general, SSOI device exhibits much better HC reliability comparing to the SOI ones. As long as we can make good quality interface for SSOI, the SSOI device will be very useful in terms of performance and reliability.

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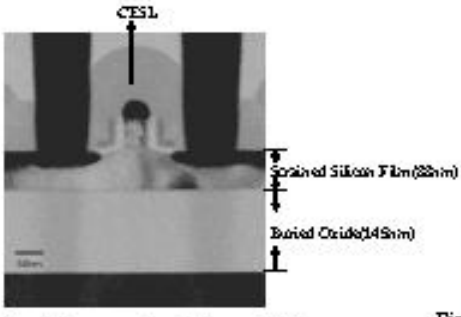

Fig. 1 A cross sectional view of SSOI MOSFET in TEM.

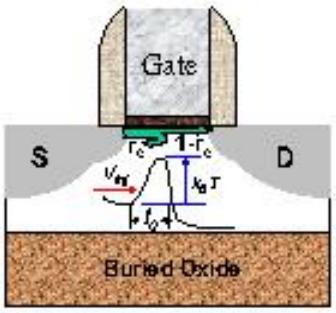

Fig. 2 The schematic showing the carrier transport. r_c is the reflection coefficient. k_BT is the barrier determining the injection velocity, V_{inj}.

$$I_{D,sat} = WC_{eff}V_{dsat}B_{sat}(V_G - V_{T,sat}) \quad (1)$$

where $I_{D,sat} @ V_G = V_{G,sat} = V, V_D = V_{D,sat} = V_{G,sat} - DIBL$

$$n = \frac{I_{D,sat} - I_{D,sat2}}{(V_1 - V_2) \cdot I_{D,sat}} \quad \text{and} \quad \eta = \frac{V_{G,sat} - V_{G,sat2}}{V_1 - V_2} \quad (2)$$

$$\frac{\lambda_0}{\lambda} = \frac{q}{0.5\left(n + \frac{\eta}{(V_G - V_{T,sat})} + 2\right)} \quad (3)$$

$$r_c = \frac{1}{1 + \frac{\lambda_0}{\lambda}} \quad \text{and} \quad B_{sat} = \frac{1 - r_c}{1 + r_c} \quad (4)$$

$$V_{inj} = \frac{I_{D,sat}}{WC_{eff}B_{sat}(V_G - V_{T,sat})} \quad (5)$$

Table 1 The formulas used to determine the two key parameters for device in the ballistic transport regime, injection velocity, V_{inj}, and ballistic efficiency, B_{sat}.

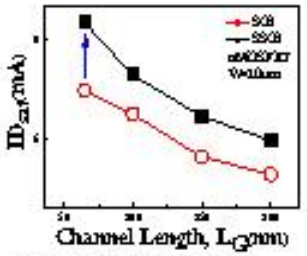

Fig. 3 Comparison of the ID_{sat} enhancements for nMOSFETs. SOI devices show 22% current gain over control SOI device.

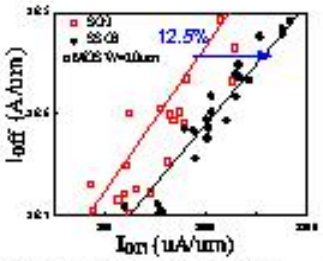

Fig. 4 The comparison of Ion Ioff between SSOI and SOI nMOSFETs. It shows that SSOI has a gain of 12.5% over that of SOI.

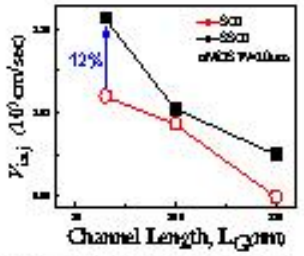

Fig. 5 Calculated injection velocity, V_{inj}. It gives larger(~12%) values of SSOI nMOSFETs in short channel devices.

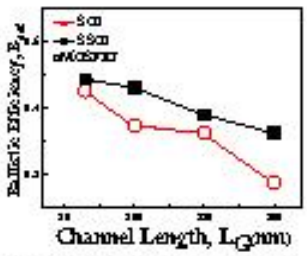

Fig. 6 Calculated ballistic efficiency, B_{sat}. The values of SSOI and SOI nMOSFETs are almost the same in short channel devices.

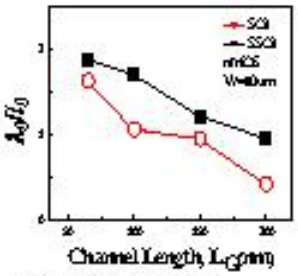

Fig. 7 Calculated carrier wavelength per mean free path, λ/λ_0.

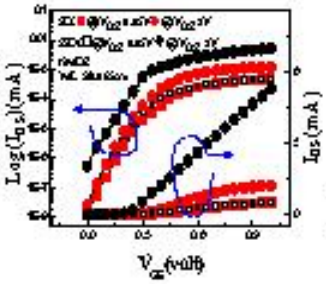

Fig. 8 I_{DS} V_{GS} on(V_{DS}=1V) and off(V_{DS}=0.05V) characteristics for SOI and SSOI nMOSFETs.

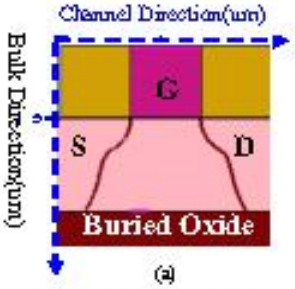

Fig. 9(a) Simulation of the structure for SOI and SSOI nMOSFETs by ISE TCAD.

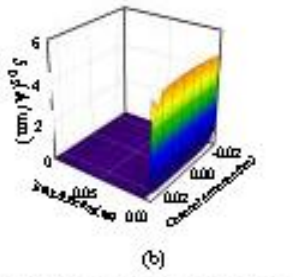

Fig. 9(b) Simulation result of the channel current density of I_{DS} V_{GS} off(V_{DS}=0.05V) for SOI and SSOI nMOSFETs by ISE TCAD.

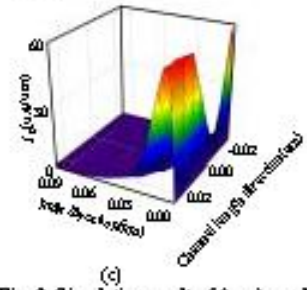

Fig. 9 Simulation result of the channel current density of I_{DS} V_{GS} on(V_{DS}=1V) for SOI and SSOI nMOSFETs.

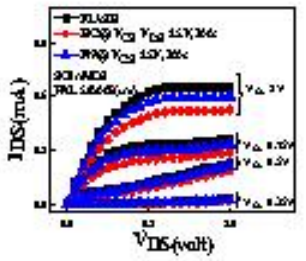

Fig. 10 I_{DS} V_{GS}@V_{GS}=1V of SOI. After HC stress, devices are degraded significantly.

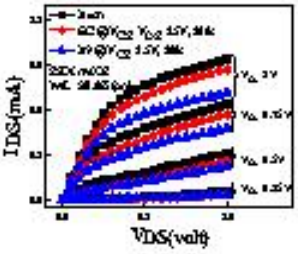

Fig. 11 I_{DS} V_{GS}@V_{GS}=1V of SSOI. After FN stress, devices are degraded significantly. It means that SSOI exhibits worse channel interface quality than SOI ones.

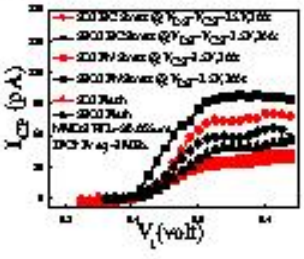

Fig. 12 Charge pumping currents of SOI and SSOI nMOSFETs before and after FN stress and HC stress.

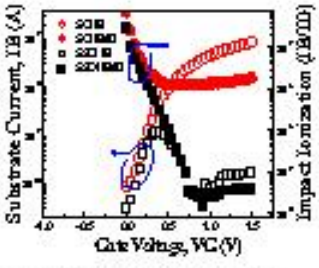

Fig. 13 I_{DS} V_{GS}@V_{GS}=1V of SOI and SSOI nMOSFETs. The impact ionization rates of SOI nMOSFETs are much larger than that of SSOI nMOSFETs.

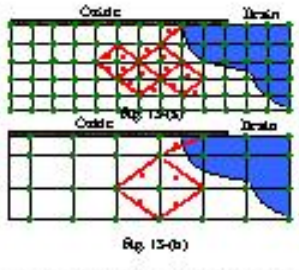

Fig. 14 As a result of different lattice constant of SOI and SSOI nMOSFETs, the impact ionization rates of SOI nMOSFETs are much higher.

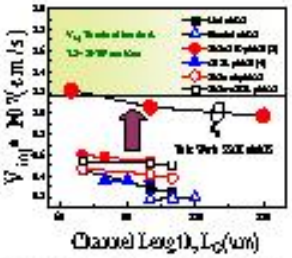

Fig. 15 A roadmap of the injection velocity from reported results and our new work. Note that our new results show a much higher V_{inj} comparing to previous works.

References

[1] K. Rim et al., in *Tech. Dig. IEDM*, p. 49, 2003

[2] J. Hoyt et al., in Tech. Dig. IEDM, p. 23, 2002

[3] S. S. Chung et al., *in Tech. Dig. IEDM*, p. 325, 2006.

[4] S. S. Chung et al., in *Symp. on VLSI Tech.*, p. 86, 2005.

[5] C. H. Ge et al., in Tech. Dig. IEDM, p. 73, 2003.

[6] M. Lundstrom, *IEEE EDL*, vol. 18, p. 361, 1997.