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Design, fabrication and calibration of a novel MEMS logic gate

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Abstract

This paper presents the design, fabrication and calibration of a novel MEMS logic gate that can perform Boolean algebra as well as logic devices composed of solid-state transistors. Unlike existing designs, the proposed design can perform either NAND gate or NOR gate functions using the same mechanical structure, but different electrical interconnects. The proposed design imposes three requirements on the fabrication process: two voltage levels carried on a suspended plate, metal-to-metal contact between shuttle electrodes and fixed electrodes, and a low process temperature (<300 °C). To fulfill these requirements, the residual stress in the fabricated device is substantial which could impair the functionality of the device. Therefore, a novel *in situ* film stress calibration method is developed to assist the development of the fabrication process. In a prototype design, the fabricated device is 250 μm long, 100 μm wide and of 3.97 μm gap. Experimental results show that the device can operate at 25/−25 V and 100 Hz, and achieve the proposed logic functions. In addition, several properties of this device are experimentally evaluated, including power consumption, on/off resistance, lifetime and resonant frequency.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Microelectromechanical switches (MEMS switches) have the advantages of no leakage current and low insertion loss, and are considered as one of the possible solutions for IC power management [1] and RF transmission lines [2, 3]. These MEMS switches are often designed to work with IC circuits consisting of solid-state devices and are responsible for only a small portion of the circuit functions because they perform only on/off functions. The limited capabilities of these MEMS switches limit their applications.

MEMS logic gates are MEMS switches that can perform Boolean algebra [4]. With this computation capability, MEMS logic gates are expected to have more applications than existing MEMS switches. Very few researchers have presented MEMS logic gate designs [1, 5, 6]. Their designs use four MOS-like MEMS devices to construct a logic device, which is very similar to the conventional MOS transistor logic gates. In our previous study [6], we proposed a MEMS logic gate design that did not stem from conventional MOS devices, and thus consumed less silicon area. That design can perform either NAND or NOR gate functions with the same mechanical structure but different electrical interconnects. These two advantages make this design a good candidate for implementing complicated digital circuits. However, due to a lack of metal-to-metal contact in our previous device, its feasibility was only verified by the mechanical properties and optical observations.

Metal-to-metal contact, between a shuttle electrode and a fixed electrode, reduces the contact resistance, and thus is crucial to MEMS switch designs. Currently, there are two methods for implementing this contact mechanism. One method uses metal for the material of the entire shuttle structure [7]; the other uses dielectric materials as the backbone of the shuttle structure and deposits a metal film on top of that [8]. Compared to the former approaches, the latter approach has the advantage of implementing multiple voltage levels on a shuttle structure. However, its fabrication process is relatively complicated. Besides, since the shuttle structure consists of multiple layers, it is likely to bend due to stress mismatch. This structure bending is usually not preferred in MEMS devices

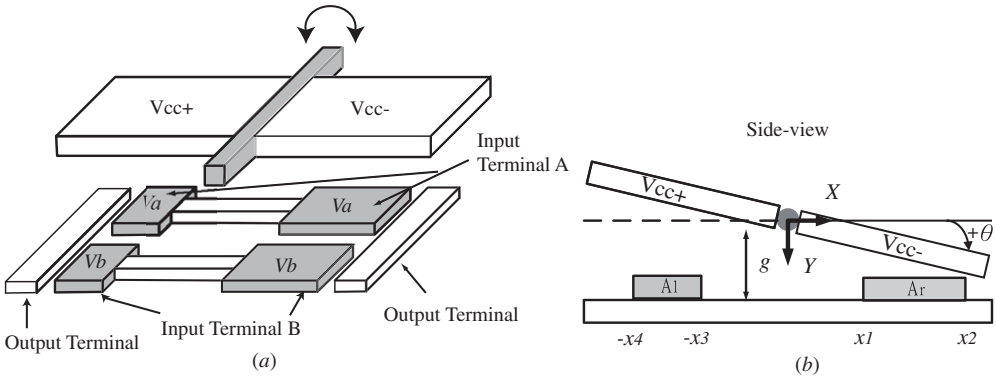


Figure 1. A torsional, two-layer MEMS logic gate design: (*a*) 3D view and (*b*) side view.

because it can seriously influence the reliability and dynamic properties of the devices [7–9].

The deflection profile of a suspended multi-layer structure is related to both boundary conditions and residual stress in each layer. This residual stress can be approximated by a mean stress and a stress gradient in thin film applications, whose values strongly depend on the fabrication process conditions [10]. Therefore, both the mean stress and stress gradient should be used to determine the bending of a multi-layer structure. Further, the stress measurement structures, which provide the information of the mean stress and stress gradient, should be *in situ* fabricated with the intended devices. Min *et al* [10] proposed an *in situ* film stress calibration method for a two-layer suspended structure. Their method uses a set of cantilever beams with the 'clamped' boundary condition to determine film stress. However, the mean stress of the base layer must be known beforehand. The approaches of using one film stress as a reference to calculate film stress of another, or simply ignoring the mean stress in a film, can be seen in many film stress calibration methods for multi-layer structures. Fang *et al* [11] proposed the film stress calibration method for single-layer suspended structures. Their method uses one cantilever beam with different boundary conditions, named 'nominally clamped', to simultaneously determine the mean stress and stress gradient. However, their approach on the deflection of a two-layer structure [12] ignored the mean stress of the base layer when calculating the curvature of a bi-layer structure, which may be inaccurate in many cases.

This paper proposes a new fabrication process so that our previous logic gate design [6] can have the metal-to-metal contact properties. Our unique logic gate design imposes three constraints on the fabrication process: two voltage levels carried on a suspended plate, metal-to-metal contact between shuttle electrodes and fixed electrodes, and a low process temperature (<300 °C) for CMOS compatibility. Thus, most existing MEMS fabrication processes cannot be directly applied. In this process, metal films are deposited onto a dielectric material to allow multiple voltage levels on a suspended plate. Due to low process temperatures, substantial residual stress in each film causes the two-layer structure to bend. We intend to lessen this bending problem by depositing a redundant film on the two-layer structure for stress mitigation. Specifically, this stress mitigation is achieved by two parts: engineering the film stress from its fabrication conditions and calibrating film stress using a newly developed *in situ* film calibration method. This film calibration method employs three test specimens with two different boundary conditions to provide the information of both the mean stress and stress gradient, which combines the advantages shown in [10] and [11]. Experimental results confirm the performance of the fabricated devices in many aspects, including logic function, power consumption, on/off resistance, lifetime and resonant frequency.

2. Operation principles of the proposed logic gate design

Figure 1 illustrates a simplified version of the proposed logic gate. The proposed design consists of shuttle electrodes on the top and fixed electrodes at the bottom. When the shuttle electrodes are biased at the voltages of V_{cc+} and V_{cc-}, and the fixed electrodes (input terminals A and B) are deployed by either V_{cc+} or V_{cc-}, the devised dimensions of actuation pads (A_l and A_r in figure 1) produce differential electrostatic force on both sides of the shuttle electrodes. Thus, the shuttle electrodes would carry out a see-saw motion and connect the output terminal at each end to export the corresponding output voltage. If the voltage level of V_{cc+} and V_{cc-} represents '1' and '0' in digital circuitry respectively, the input–output relations of this device can be the same as a logic gate consisting of solid-state transistors. For example, the design shown in figure 1 can function the same as a NOR gate. Besides, reversing the bias voltages on the shuttle electrodes can switch the logic function of this device from a NOR gate function to a NAND gate function.

Based on the intended operation of this device, the design task is to ensure that the tilting plate can rotate toward the designed direction and connect with the output terminal to export signals. This is accomplished mainly by the design of the actuation pad configurations, stiffness of the torsional flexures, dimple height, gap height and actuation voltages. The equations and design considerations were addressed in detail in our previous paper [6]. However, it should be emphasized here that the maximum tilting angle of the suspended plate is the key factor to the functionality of the device. And this is determined by the warping of the suspended plate, gap height and the dimple height.

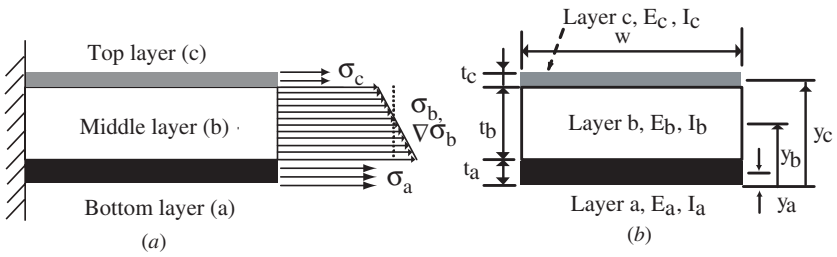


Figure 2. Stress distribution in a sandwich structure: (*a*) side view and (*b*) cross-section view.

3. Mitigation of residual stress in a multi-layer structure

In the proposed design, the suspended plate must consist of a dielectric film and metal films to carry multiple voltage levels. The suspended plate will likely bend due to the residual stress in each film. In this logic gate design, if the plate curls up, it could exceed the maximum operation angle and cause the state transition failure. If the plate bends down, it could touch the output terminals without applying any voltage. Furthermore, in this design, the dielectric material is oxide and the metal layer is gold/aluminum. The residual stress of oxide is compressive, while the gold/aluminum film is tensile. Therefore, it is very difficult to obtain a flat composite structure with these two layers. For this reason, a redundant aluminum film is deposited to form a sandwich structure to balance stress.

3.1. Three-layer beam deflection theory

According to the proposed design shown in figure 1, the defection of the suspended structure, due to mismatched residual stress, can be attributed to bending of the torsional flexures and the plate. Since the torsional flexure is constrained at both ends and its length is shorter than that of the plate, the bending stiffness of torsional flexures is approximately 20 times greater than that of the plate. For simplicity, the structure deflection due to torsional flexure is neglected.

As discussed before, both the mean stress and stress gradient in each layer should be considered when calculating the deflection of a multi-layer structure. However, in this case, the top and bottom layers are relatively thin compared to the middle layer. Therefore, the stress gradient in the top and bottom layers contributes less to the structure bending, and both are neglected. Figure 2(*a*) depicts the stress distribution in this sandwich structure.

To calculate the deflection of this sandwich structure, the neutral axis and the moment of inertia are first calculated for this multi-layer structure. The neutral axis is determined by finding the centroid of the cross section, which is considered as the equivalent width according to Young's modulus of each material. Using Young's modulus of the middle layer for normalization, equation (1) gives the equivalent width of each layer and the neutral axis (y_e) of the composite structure. Equation (2) gives the moment of inertia (I_e) of this sandwich structure, as calculated by the 'parallel axis theorem [13]':

$$w_a = \left(\frac{E_a}{E_b}\right) w, \qquad w_b = \left(\frac{E_b}{E_b}\right) w, \qquad w_c = \left(\frac{E_c}{E_b}\right) w,$$

$$y_e = \frac{y_a w_a t_a + y_b w_b t_b + y_c w_c t_c}{w_a t_a + w_b t_b + w_c t_c}, \tag{1}$$

$$I_e = I_a + w_a t_a (y_e - y_a)^2 + I_b + w_b t_b (y_e - y_b)^2 + I_c + w_c t_c (y_e - y_c)^2, \tag{2}$$

where w is the width of a sandwich structure, t_a, t_b and t_c are the thicknesses of each layer, E_a, E_b and E_c are Young's modulus of each layer, and I_a, I_b and I_c are the moment of inertial of each layer. Figure 2(*b*) shows a cross section of the sandwich structure. Assuming the 'small deflection', equation (3) describes the relation between the bending moments and the deflection of a cantilever beam:

$$M_e = \frac{2E_b I_e \delta_e}{L^2},$$
$$M_e = \sigma_a w t_a (y_e - y_a) - \sigma_c w t_c (y_c - y_e) - \sigma_b w t_b (y_b - y_e) + \frac{1}{6}\nabla\sigma_b w t_b^2, \tag{3}$$

where δ_e is the deflection of the sandwich structure and L is the length of the plate. Therefore, the deflection of a sandwich structure can be determined if the residual stress in each film is known.

3.2. In situ calibration of residual stress

We develop a new *in situ* stress calibration method, which combines the approaches shown in [10] and [11], to calculate the residual stress in thin films. This approach involves three types of the test specimens with two different boundary conditions (see figure 3). Structure *A* is a suspended structure with a 'nominally clamped' boundary condition. As suggested by [11], its mean stress and stress gradient can be determined by the following equation:

$$\sigma_b = \frac{E_b(-0.0043 t_b (94.186 + (-5.465 + t_b) t_b) + \rho_b \phi_b)}{\rho_b (1.022 - 0.014 t_b)(1.33 + 0.45 \nu_b)},$$
$$\nabla\sigma_b = \frac{E_b t_b}{2\rho_b}, \tag{4}$$

where ν_b is Poisson's ratio of the material b, and ρ_b and ϕ_b are the radius of curvature and the rotation angle at the constrained end, respectively, after the structure is released. These two values are better visualized in figure 4(*b*). Therefore, both the mean stress and stress gradient of the material b can be obtained by measuring the deflection profile.

Structure *B* has the 'clamped' boundary condition, which is the same as that discussed in [10]. This structure consists

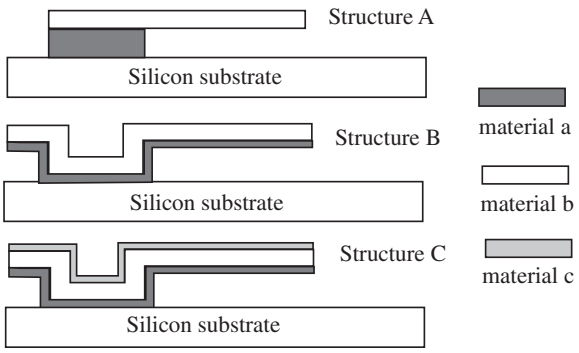


Figure 3. Three types of test specimens for stress calibration. Structure *A* consists of material *b* and a 'nominally clamped' boundary condition. Structure *B* consists of material *a* and *b*, and a clamped boundary condition. Structure *C* consists of material *a*, *b* and *c*, and a clamped boundary condition.

of two layers (materials *a* and *b*), and the top layer is the same as structure *A*. The deflection of this composite structure can be modeled as follows:

$$\begin{aligned} y_B &= \frac{y_a\omega_a t_a + y_b\omega_b t_b}{\omega_a t_a + \omega_b t_b}, \\ I_B &= I_a + \omega_a t_a (y_B - y_a)^2 + I_b + \omega_b t_b (y_B - y_b)^2, \\ M_B &= \sigma_a \omega t_a (y_B - y_a) - \sigma_b \omega t_b (y_B - y_b) + \frac{1}{6}\nabla\sigma_b \omega t_b^2, \\ M_B &= \frac{2E_b I_B \delta_B}{L^2}. \end{aligned} \tag{5}$$

Therefore, the mean stress of the material *a* can be determined by measuring the structure deflection after it is released and by the residual stress obtained from structure *A*.

Structure *C* is a sandwich structure whose two bottom layers are the same as structure *B*. Its deflection is modeled in equation (3). Therefore, the mean stress of the material *c* can be determined by measuring the structure deflection after the structure is released and by the residual stresses obtained from structures *A* and *B*.

Table 1. Material properties and film dimensions for stress calibration.

	Oxide	Gold/aluminum	Aluminum
Young's modulus (GPa)	75	75/80	80
Possion's ratio	0.24	0.43/0.26	0.26
Thickness (μm)	2.94	0.3	0.25
Length (μm)	125	125	125
Width (μm)	100	100	100

3.3. Experimental results of stress calibration

The three types of test specimens shown in figure 3 were fabricated *in situ* with intended MEMS devices for stress calibration. Materials *a*, *b* and *c* are gold/aluminum, oxide and aluminum, respectively. Table 1 lists the material properties and film thickness.

After release, the plate deflection profile was measured by a non-contact white-light interferometer. Figure 4 shows that the deflection of the structure *A* (δ_A) was measured as 4.78 μm, the radius of curvature (ρ_b) was 2.4×10^{-3} m, and the plate bend down angle (ϕ_b) was 5.55 mrad. Using equation (4), the mean stress of the oxide film was calculated to be compressive 270 MPa on average and the stress gradient was 40 MPa on average. The deflection of structure *B* (δ_B) was 3.16 μm. Using equation (5), the mean stress of this gold/aluminum film was tensile, 164 MPa on average. The deflection of structure *C* (δ_C) was measured as 0.4 μm. Using equation (3), the mean stress of the aluminum film was compressive, 68 MPa on average.

The residual stress values above indicate that the redundant aluminum film should be 0.3 μm to produce a non-warping sandwich structure.

4. FEM simulations

In the current logic gate design, the torsional flexure width of this device was designed to be 10 μm, and the gap for the electrostatic actuation was 3 μm. The expected bandwidth of the device was 40 kHz, and the actuation voltages of

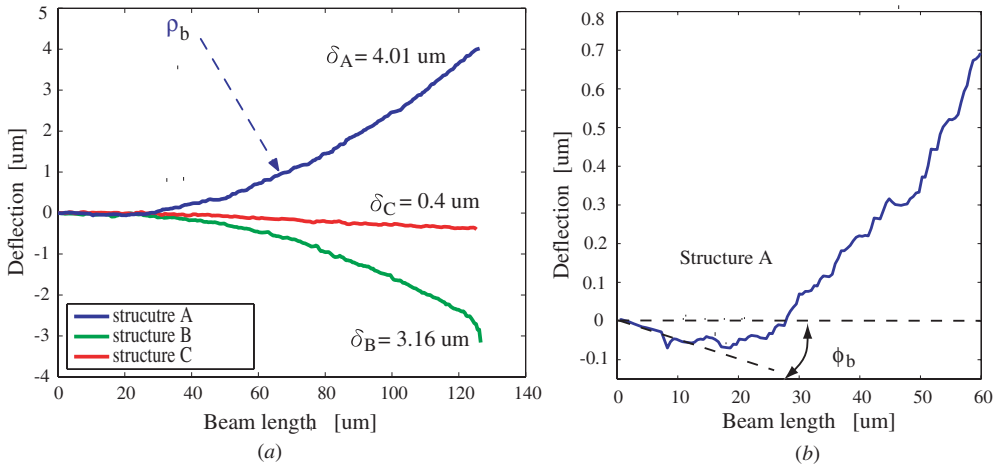


Figure 4. (*a*) Defection profiles of three test specimens. (*b*) Close-up view of the deflection profile of structure *A*.

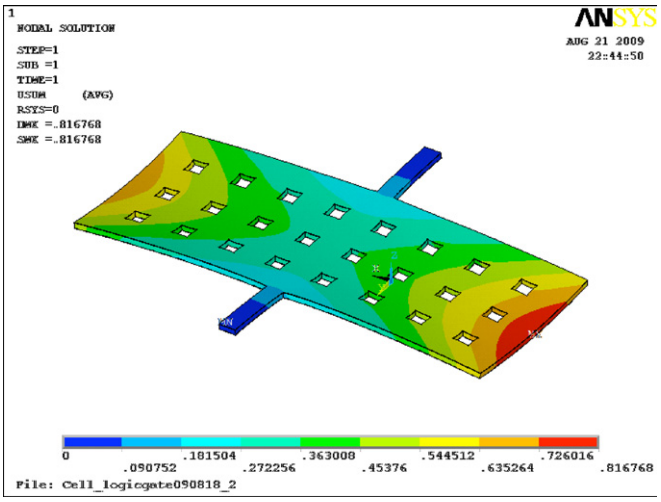


Figure 5. FEM simulations on the structure bending. The maximum deflection is 0.81 μm at the end of the plate.

Table 2. Specifications of the MEMS logic gate design.

Plate width	100 μm
Plate length	250 μm
Electrodes locations	40 μm, 100 μm
(x_1, x_2, x_3, x_4 shown in figure 1)	-80 μm,-100 μm
Torsion flexures width/length	10 μm/45 μm
Actuation voltages V_{cc+}, V_{cc-}	25, -25 Volts
Gap	3 μm
Dimple height	2 μm
Max. plate angle	$\pm 8 \times 10^{-3}$ rad
Pull-in voltage of inputs (1, 1) and (0, 0)	20.83/29.29 V
Resonant frequency	40 kHz

(V_{cc+}, V_{cc-}) were (25 V, -25 V). The maximum rotation angle of this device was designed to be 0.008 rad to comply with the upper limit of 0.015 rad. Table 2 lists other design parameters and specifications.

The film stresses, obtained from experimental results, were used to predict the structure bending of the proposed logic gate design. Figure 5 shows that the maximum plate deflection was 0.81 μm at the end of the plate, which implies that the plate tilting angle can be reduced by 0.006 rad if the fabricated device goes through the same process conditions as the test specimens.

Since the device dimensions and materials were different from what were reported in [6], we did the modal analysis again for the new design and compared it to the experimental results later on. The analysis showed that the first resonant mode was the designated torsional motion and the resonant frequency was 40.28 kHz; the second mode was a plate bending mode (up-and-down) and its resonant frequency was 89.29 kHz. These two resonant frequencies are somewhat close to each other and should be modified in the future.

Obviously, the operating voltage (25 V, -25 V) cannot work directly with current CMOS circuits. The high operating voltages mainly come from the 10 μm line width and the 3 μm gap, which are limited by the capability of our clean room facilities. Our simulation indicates that if the line width can be narrow down to 2 μm and the 1 μm gap, the proposed design can operate at (0, 1.5 V) with a operating bandwidth around 8 kHz. However, this requires very precise process controls. The current design only meant to verify the device feasibility as much as it can.

5. Fabrication process

Figure 6 shows the in-house developed MEMS process for fabricating the proposed logic gate design. This process is totally different from what was reported in our previous paper [6] in that it features the metal-to-metal contact and a low process temperature.

Beginning with (1 0 0) n-type silicon wafers, this process used dry oxide and silicon nitride deposition for stress buffering and electrical isolation. The first step was to pattern the metallization layer (gold, 0.1 μm) for the electrical interconnects and the bottom electrodes. In step 2, a 3 μm amorphous silicon layer was deposited as a sacrificial layer, which was used to form the gap of the device. This sacrificial layer was then patterned by two masks: the dimple mask and the deep trench mask. The dimple mask transferred 2 μm notches onto the sacrificial layer, and the deep trench mask defined the sidewalls of the anchor structure. In steps 3 and 4, an adhesion layer (chrome) was deposited on top of the sacrificial layer, followed by 0.1 μm of gold and 0.2 μm of aluminum. These metal layers formed the top electrodes. A 3 μm of silicon oxide layer was then deposited. This layer not only served as the backbone of the suspended structure, but also refilled the 3 μm trenches (deep trench mask) to protect the anchor structure. Next, a 0.25 μm aluminum film was sputtered for both a hard mask design and stress balance. After patterning the hard mask, the etch holes, micro flexures, suspended plate and electrodes were patterned on the oxide layer in step 5 and released with dry etching using sulfur hexafluoride SF_6-based plasma in step 6. A total of six masks were used to complete this process.

5.1. Fabrication process discussion

In this fabrication process, the suspended plate consisted of three thin films: aluminum, silicon oxide and gold/aluminum. To minimize the deflection of this composite structure, the residual stress in each layer should be carefully engineered. Since the gold film was deposited by a thermal evaporation process, it was difficult to control the film stress in this process. The oxide film was deposited by an Oxford PlasmalabSystem100 machine. With this machine, previous researchers [14] reported that the residual stress can be lowered using three process conditions: low [N_2O/SiH_4] ratio, low RF power and large gas flow. We performed several experiments to lower the film stress. Table 3 lists the optimal process parameters that we have found so far. Under these process conditions, the residual stress of silicon oxide was 270 MPa, as calculated by the proposed stress calibration method.

The residual stress of an aluminum film varies with its film thickness [12]. Besides, it is difficult to control the process conditions precisely. Therefore, although the previous

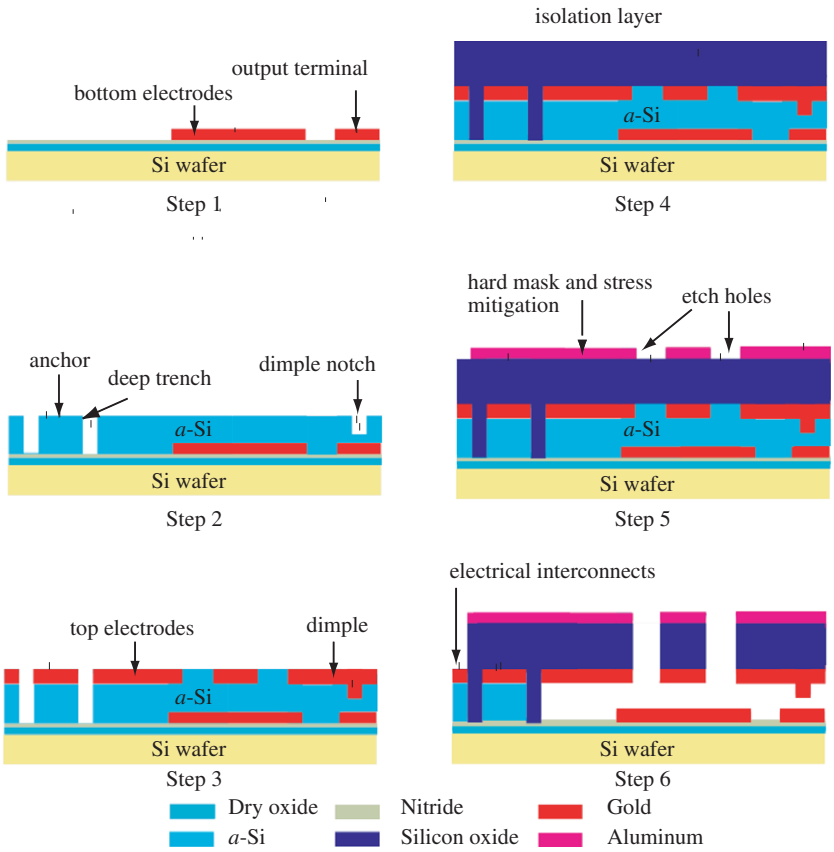


Figure 6. A process flow for fabricating the logic gate.

Table 3. PECVD process conditions for depositing silicon oxide.

T °C	300 °C
$\Phi_{N_2O}, \Phi_{SiH_4}$	525, 75(sccm)
$[N_2O/SiH_4]$	7
RF power	100 W
Cavity pressure	100 Torr

Table 4. Process conditions for etching an a-Si sacrificial layer.

T °C	14 °C
RF power	0 W
ICP power	1550 W
Cavity pressure	10 Torr
Selectivity: [a-Si/oxide]	50 : 1

analysis suggested a redundant 0.3 μm aluminum film for stress mitigation, the thickness of the aluminum film was set to 0.25 μm when fabricating the logic gate device.

The gap of this device was designed to be 1 μm, but it could be less when considering the uncertainties of structure bending and fabrication. For this reason, the isotropic dry etch method was used to release the structure instead of the frequently used wet etch method. When using the dry etch method, the etch selectivity between a sacrificial layer and a structure layer is the top concern. In this project, an Oxford PlasmalabSystem100 machine, which employed inductively couple plasma (ICP) and sulfur hexafluoride (SF_6) gas, was used to etch away amorphous silicon and released the structure. After several trials, we concluded that the high chamber pressure, high ICP power and low RF power on the substrate were three key conditions to achieving high etch selectivity between oxide films and amorphous silicon films. With an etch hole size of 10 μm $\times$ 10 μm and the process parameters shown in table 4, this recipe can achieve a 15 μm lateral undercut in a 3 μm gap. The selectivity was around 50:1 in this process.

6. Experimental results and discussion

6.1. Device dimensions

Figure 7 shows a photo of a fabricated logic gate. This photo was taken prior to the deposition of the last aluminum film. Since the oxide film is transparent, the isolation features on the suspended plate, the metal film under oxide and the dimple structures are all clearly visible. The V_{cc+} and V_{cc-} are applied to the anchor and then transferred through micro flexures to the suspended plate. Two input signals are given to the input terminals A and B. The dimple structures are underneath the suspended plate at two ends. Two output terminals are shown at the two ends of the device, and they will be linked together through electrical interconnects later on.

Figure 8 shows the detailed dimensions of the fabricated device before release. The amorphous silicon film (sacrificial layer) is 3.97 μm and the height of the dimple is 2.12 μm; this leads to 1.85 μm between the dimple and substrate. After release and measurements of ten devices, the suspended plates all bend down slightly. Figure 9(a) shows the deflection profile

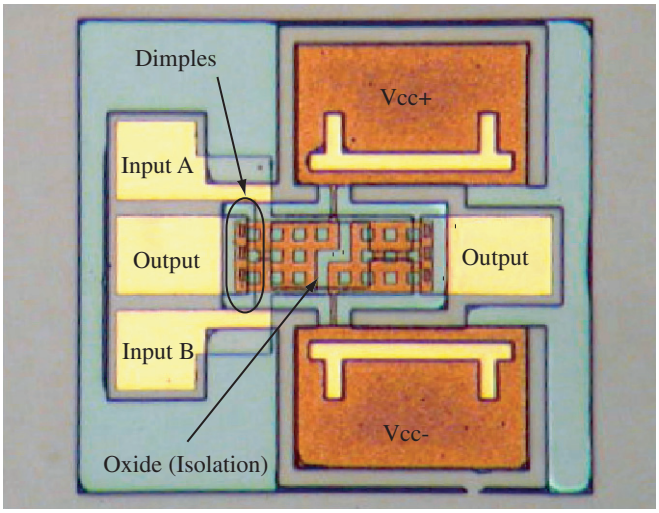


Figure 7. A photo of the fabricated MEMS logic gate. The photo was taken prior to the deposition of the last aluminum film.

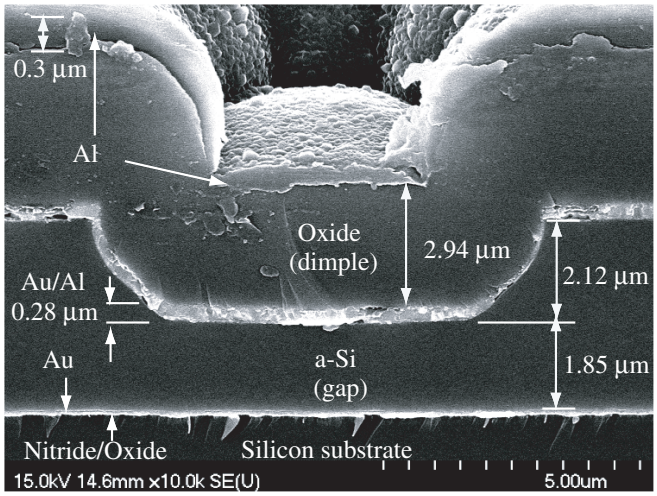


Figure 8. A SEM photo of the dimple structure before the device is released.

of one of the devices. The suspended plate bends down 0.86 μm, which creates a 1 μm gap. This corresponds to 8×10^{-3} rad of plate tilting angle and complies with the constraint of the upper limit. Besides, the measured 0.86 μm plate deflection is very close to the predicted 0.81 μm from our FEM simulations (figure 5). For comparison purposes, figure 9(*b*) shows the plate deflection without the additional aluminum film. The plate bending distance is approximately 2 μm, which is roughly the same as the gap between the substrate and the dimples. This indicates that the suspended plate touches the output terminals without applying any actuation voltage, and thus destroys the functionality of the device.

6.2. Frequency response

To investigate the dynamics of the proposed logic gate design, we measured the frequency response of a fabricated device using a laser doppler vibrometer (LDV) and a network analyzer. Figure 10 shows that the resonant frequency was measured at approximately 39 kHz, which was predicted to be 39.25 kHz using the fabricated dimensions and FEM analysis. Deducing from this experimental data, the damping ratio (ζ) of this device was calculated to be 0.11.

6.3. Logic function

Figure 11 shows the input and output signals of a fabricated device when the shuttle electrodes are biased at the voltage of +25 V and −25 V; two input signals are either +25 V or −25 V. Note that, in the plot, the oscilloscope readings of three signals (two inputs and one output) are placed at different vertical locations for ease of reading. The switching frequency of input signals is 100 Hz. In case (a), two input signals switch between (0, 0) and (1, 1) back and forth. The output switches between 1 and 0, correspondingly. An examination of these four cases (a)–(d) reveals that the proposed design can perform NOR gate functions. A similar experiment was performed when the bias voltages on the suspended plate were reversed. The experimental results in figure 12 show that the proposed design can perform NAND gate functions. Therefore, the proposed design can perform both NOR gate or NAND gate functions depending on the electrical interconnects.

6.4. Power consumption

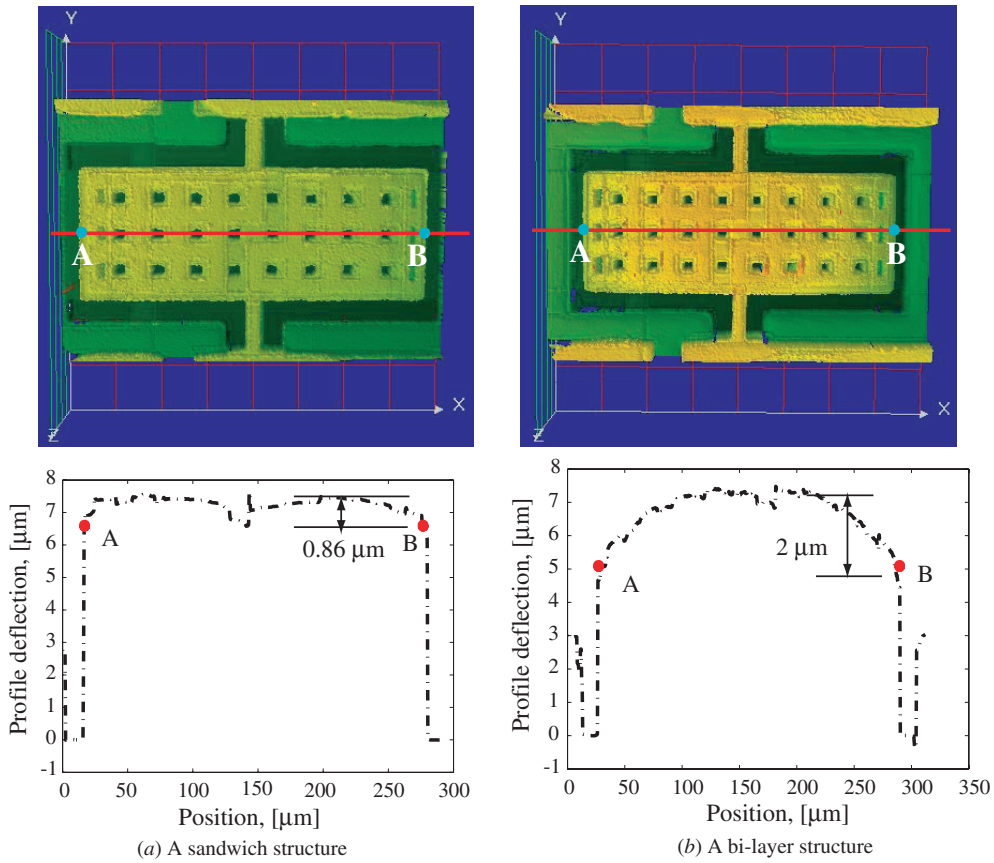
To calibrate the power consumption of this logic device, an external resistor was connected to the device in series, and the voltage across the resistor was measured during a turn-on stage. Figure 13(*a*) shows the equivalent circuit network of this setup; figure 13(*b*) shows the time response of the measured signal. The power consumption of this logic device with this setup is calculated as follows:

$$\begin{aligned} J_{sw} &= \int_0^{t_s} V_{sw}(t) I_{sw}(t)\,\mathrm{d}t \\ &= \int_0^{t_s} (V_s - V_r)\frac{V_r}{R_{\mathrm{ext}}}\,\mathrm{d}t, \end{aligned} \tag{6}$$

where t_s is the rising time, R_{ext} is the external resistance and V_r is the voltage drop across R_{ext}. Using the V_r measurements shown in figure 13(*b*), the power consumption J_{sw} is calculated to be 1.482 nJ.

This energy consumption mainly consists of three terms: energy stored in the torsional flexures (J_{elastic}), energy dissipation due to the resistance of electrical interconnects (J_{resistor}) and energy dissipation due to damping forces (J_{damping}). These energy terms can be estimated by the following equations, respectively:

$$\begin{aligned} J_{\mathrm{elastic}} &= \frac{K_t \theta_{\max}^2}{2}, \\ J_{\mathrm{resistor}} &= \int_0^{t_s} I_{sw}(t) R_{\mathrm{int}}\,\mathrm{d}t, \\ J_{\mathrm{damping}} &= \int_0^{t_s} \zeta \dot{\theta}(t)\theta(t)\,\mathrm{d}t, \end{aligned} \tag{7}$$



(*a*) A sandwich structure (*b*) A bi-layer structure

Figure 9. Deflection profiles after the devices are released. (*a*) A sandwich structure bends down 0.86 μm. (*b*) A bi-layer structure bends down 2 μm.

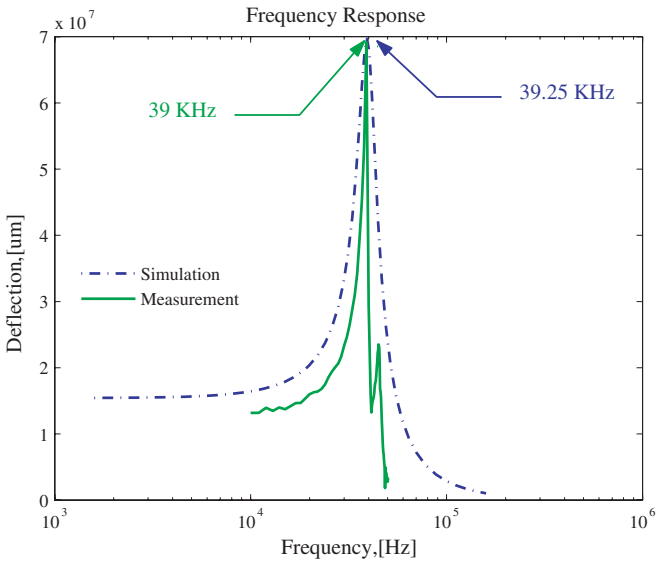


Figure 10. Frequency response of the MEMS logic gate. The first resonant mode was measured at 39 kHz, while it is predicted at 39.25 kHz by simulations.

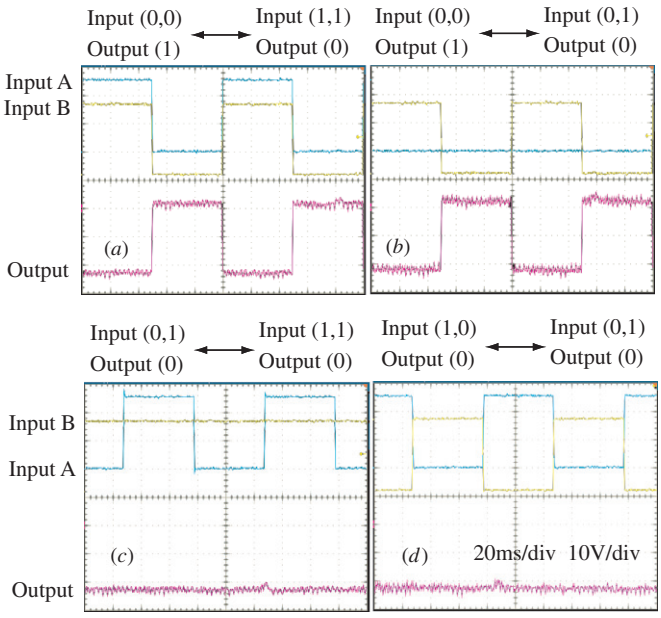


Figure 11. NOR gate functions of the proposed device. (*a*) Input: (0, 0) ↔ (1, 1); output: 1 ↔ 0. (*b*) Input: (0, 0) ↔ (0, 1); output: 1 ↔ 0. (*c*) Input: (0, 1) ↔ (1,1); output: 0 ↔ 0. (*d*) Input: (1,0) ↔ (0, 1); output: 0 ↔ 0.

where K_t is the stiffness of the torsional flexures, θ is the plate tilting angle, θ_{max} is the maximum rotation angle, which is 8×10^{-3} rad in this case, and R_{int} is the resistance of electrical interconnects. This resistance is estimated to be 95.4 Ω using the measured sheet resistance 9.53 (Ω/square) of the deposited

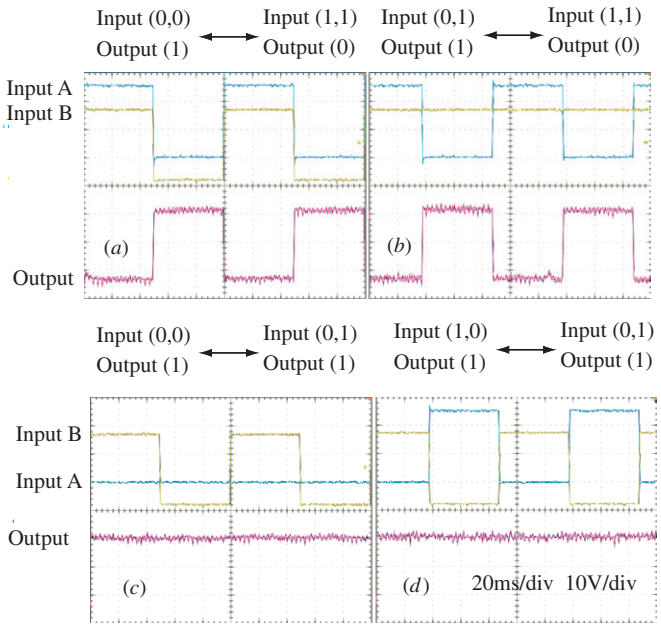


Figure 12. NAND gate functions of the proposed device. (*a*) Input: (0, 0) ↔ (1,1); output: 1 ↔ 0. (*b*) Input: (0, 1) ↔ (1,1); output: 1 ↔ 0. (*c*) Input: (0, 0) ↔ (0, 1); output: 1 ↔ 1. (*d*) Input: (1,0) ↔ (0, 1); output: 1 ↔ 1.

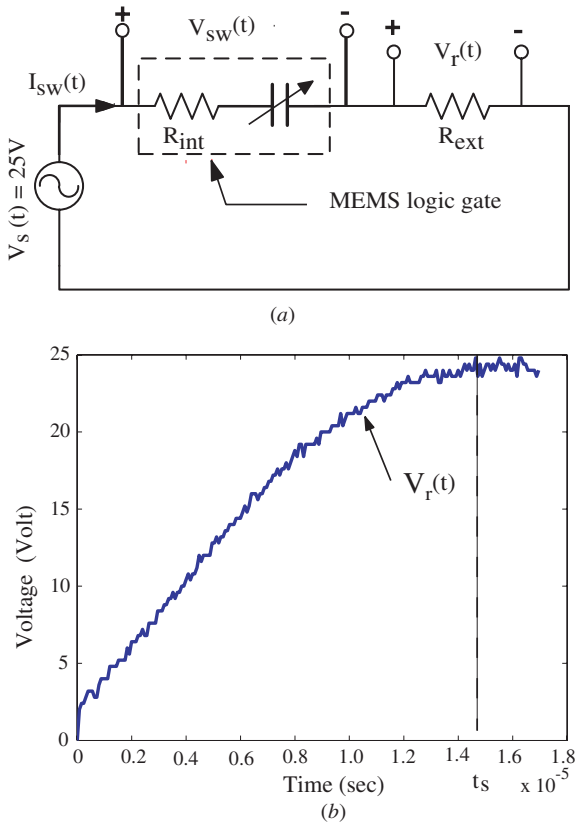


Figure 13. (*a*) A setup for calibrating the power consumption of the device. (*b*) The transient response of $V_r(t)$ during a turn-on stage. The rising time was measured approximately at 14.8 μs.

metal film. In this case, using the equation given above, J_{elastic} is 31.64 pJ, J_{resist} is 0.85 pJ and J_{damping} is 1.1 nJ. Therefore, it is clear that, in the turn-on stage, most of the energy is not stored in the torsional spring, but dissipated by the damping force.

6.5. Lifetime

We have conducted several tests on the fabricated logic gates, which do not require physical contacts between top electrodes and bottom electrodes. The devices do not show any significant performance degradation. However, when conducting a reliability test involving physical contacts, the device suffered from the 'stiction problem'. The device stuck to one state and stopped switching, and the restoring forces from torsion bars failed to pull the suspended plate back to its nominal position even when the applied voltages were removed. We test three or four devices and they all had the same problem. And, the best one lasted about 24 000 switching cycles. To investigate this contact problem, several SEM/AFM photos of the top/bottom electrodes were taken before and after the test. Figure 14 shows the surface roughness of both the dimple structure (top electrode) and contact pads (bottom electrode). For the dimple, it was 12.57 nm before the test and 5.73 nm after the test; for the contact pads, it was 5.16 nm before the test and 4.13 nm after the test. These numbers are similar to that reported in other literature [15]. SEM photos show no obvious surface deformation for the contact pads, but material removal for the dimple structure (figure 15). The material removal caused the stiction problem that has been reported in other literature [16]. We suspect that the high voltage (±25 V) on the switch accelerates the electromigration and thus the material removal. More study is needed to investigate this stiction problem in detail.

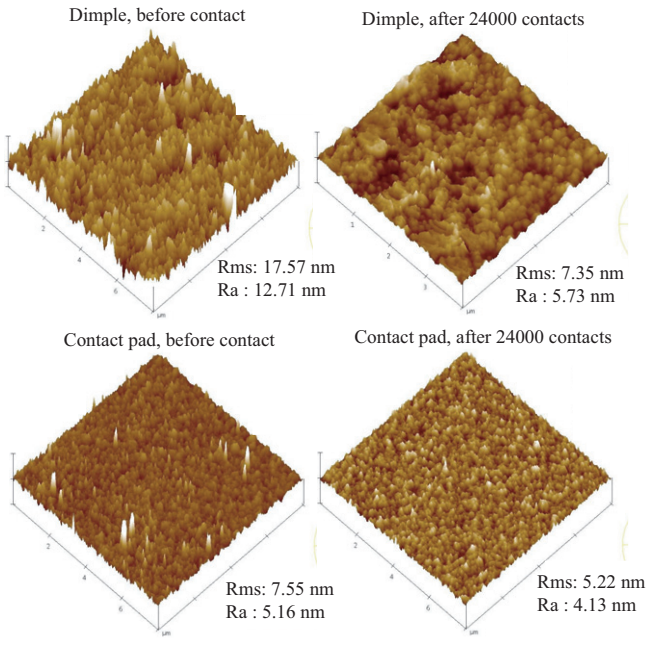


Figure 14. Surface roughness of the dimple structure and contact pads before and after the reliability test. RMS is the standard deviation; Ra is the mean value.

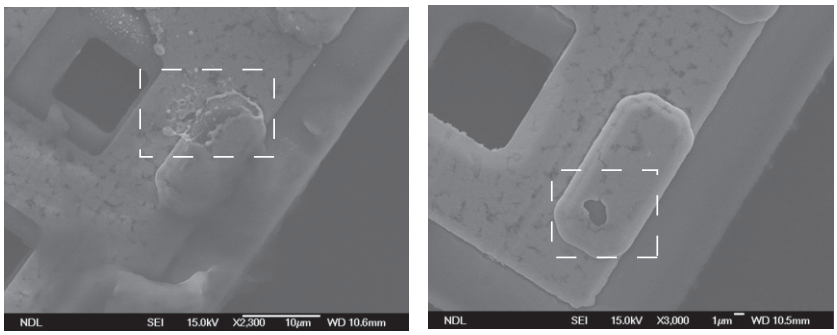


Figure 15. Material removal appeared on the dimple structure after the stiction problem.

Table 5. Performance of the MEMS logic gate.

Performance of the MEMS logic gate	
Turn-on resistance	≈100 Ω
Turn-off resistance	out of range
Mechanical lifetime	$>10^6$ cycles
Electrical lifetime	2.4×10^4 cycles

Table 5 lists other performance values of the proposed logic gate design.

7. Conclusion

This paper presents the design, fabrication processes and performance calibrations of a novel MEMS logic gate. The logic function of this MEMS device comes from several features on an electrostatically actuated tilting plate, including different dimensions of actuation pads, pull-in voltages, dimple structures and two voltage levels on a suspended plate.

A non-warping suspended structure that can carry two voltage levels is crucial to the functionality of this design. This structure can be realized by depositing a redundant aluminum film (0.25 μm) onto a suspended structure composed of oxide film (2.94 μm) and aluminum/gold (0.3 μm) film. Stress is mitigated by both engineering the film stress from its process conditions and a novel *in situ* film stress calibration method, which uses three test specimens with two boundary conditions to calibrate the residual stress of a sandwich structure. The resulting structure bending was 0.86 μm, which is very close to our prediction of 0.81 μm.

The fabricated MEMS logic gate was a suspended structure with a dimension of 250 μm by 100 μm, and had a 3.97 μm gap. This device can operate at 25/−25 volts and 100 Hz, and uses the same mechanical structure but different electrical interconnects to implement either NOR gate functions or NAND gate functions. We also experimentally calibrated several important properties of this device, including power consumption (1.4 nJ), on-resistance (≈100 Ω), off-resistance (out of range), lifetime (2.4×10^4) and resonant frequency (40 kHz).

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References

[1] Hirata A, Machida K, Kyuragi H and Maeda M 2000 A electrostatic micromechanical switch for logic operation in multichip modules on Si *Sensors Actuators A* **80** 119–25
[2] Rebeiz G M and Muldavin J B 2001 RF MEMS switches and switch circuits *IEEE Microw. Mag.* **2** 59–71
[3] Peroulis D, Pacheco S P, Sarabandi K and Katehi L P B 2003 Electromechanical considerations in developing low-voltage RF MEMS switches *IEEE Trans. Microw. Theory Tech.* **51** 259–70
[4] Millman J and Grabel A 1998 *Microelectronics* (New York: McGraw-Hill)
[5] Lee S W, Johnstone R W and Parameswaran A M 2005 MEMS mechanical logic units: design and fabrication with micragem and polymumps *Proc. Canadian Conf. on Electrical and Computer Engineering (Saskatoon, Canada, 1–4 May 2005)* pp 1513–6
[6] Tsai C-Y, Kuo W-T, Lin C-B and Chen T-L 2008 Design and fabrication of MEMS logic gates *J. Micromech. Microeng.* **18** 045001
[7] Hill M, O'Mahony C, Duane R and Mathewson A 2003 Performance and reliability of post-CMOS metal/oxide MEMS for RF application *J. Micromech. Microeng.* **13** S131–8
[8] Chu C-H, Shih W-P, Chung S-Y, Tsai H-C, Shing T-K and Chang P-Z 2007 A low actuation voltage electrostatic actuator for RF MEMS switch applications *J. Micromech. Microeng.* **17** 1649–56
[9] Pulskamp J S, Wickenden A, Polcawich R, Piekarski B, Dubey M and Smith G 2003 Mitigation of residual film stress deformation in multilayer microelectromechanical systems cantilever devices *J. Vac. Sci. Technol.* B **21** 2482–6
[10] Min Y-H and Kim Y-K 2000 In situ measurement of residual stress in micromachined thin films using a specimen with composite-layered cantilevers *J. Micromech. Microeng.* **10** 314–21
[11] Fang W and Wickert J A 1996 Determining mean and gradient residual stresses in thin films using micromachined cantilevers *J. Micromech. Microeng.* **6** 301–9

[12] Fang W and Wickert J A 1995 Comments on measuring thin-film stresses using bi-layer micromachined beams *J. Micromech. Microeng.* **5** 276–81
[13] Craig R R Jr 2000 *Mechanics of Materials* 2nd edn (New York: Wiley)
[14] Charavel R, Olbrechts B and Raskin J-P 2003 Stress release of PECVD oxide by RTA *Smart Sensors, Actuators, and MEMS (Maspalonas, Gran Canaria, Spain)* pp 596–606
[15] Jensen B D, Chow L L-W, Huang K, Saitou K, Volakis J L and Kurabayashi K 2005 Effect of nanoscale heating on electrical transport in RF MEMS switch contacts *J. Microelectromech. Syst.* **14** 935–46
[16] Chow L L W, Volakis J L, Saitou K and Kurabayashi K 2007 Lifetime extension of RF MEMS direct contact switches in hot switching operations by ball grid array dimple design *IEEE Electron Device Lett.* **28** 479–81