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Study of ultra-shallow p$^+$n junctions formed by excimer laser annealing

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ABSTRACT

Excellent ultra-shallow p$^+$n junctions have been formed by thermally treating the BF_2^+-implanted Si samples by excimer laser annealing (ELA) at 300–400 mJ cm^{-2} with post low-temperature long-time furnace annealing (FA) at 600 °C. A junction with a leakage current density lower than 20 nA cm^{-2} and a sheet resistance smaller than 200 Ω □$^{-1}$ can be well achieved. No considerable dopant diffusion is observed by using this low-thermal-budget annealing process. However, by simply using the ELA treatment at 300–400 mJ cm^{-2}, the resultant junction shows a leakage current density as high as 10^4 nA cm^{-2} and a peripheral leakage current density of 10^3 nA cm^{-1}. The large junction leakage is primarily due to the leakage current generated within the junction region near the local-oxidation-of-silicon (LOCOS) edge, and which is substantially caused by the ELA treatment. The large peripheral junction leakage current density can be significantly reduced to be about 0.2 nA cm^{-1} after a post low-temperature FA treatment at 600 °C. As a result, the scheme that employs ELA treatment with post low-temperature FA treatment would be efficient for forming excellent ultra-shallow p$^+$n junctions at low thermal budget.

1. Introduction

With the progress of extreme-large-scale-integration (ELSI) technology, the metal-oxide-semiconductor-field-effect-transistor (MOSFET) channel length has been scaled down to deep submicron dimensions. Therefore, a reduction in source/drain junction depth is required in order to minimize short channel effects [1]. In conventional furnace annealing (FA), annealing temperatures higher than 900 °C should be utilized to eliminate the implant-induced defects in the Si substrate, thereby obtaining good junction characteristics. Hence, shallow p$^+$n junctions with a depth shallower than 0.1 μm are difficult to realize, due to the rapid diffusion of boron dopant in the Si substrate during high-temperature annealing [2–3].

Accordingly, schemes that use a low thermal budget should be adopted for forming shallow junctions while achieving good electrical characteristics. Rapid thermal annealing (RTA) was reported to be effective in removing the defects and activating the dopant [4–5]. However, RTA temperatures higher than 900 °C are still required, and the anomalous boron diffusion is nevertheless induced. By using ultra-low-energy implantation with rapid thermal processing, good shallow junctions may be achieved [6]. Nevertheless, schemes that use low thermal budget should be developed to facilitate forming even better shallow junctions [7]. Accordingly, formation of good shallow junctions, by using annealing processes with a low thermal budget, is important for future progressive IC technology.

The laser annealing, a technique that can be used to activate implanted dopant, enables the formation of junction with controlled dopant redistribution and low sheet resistivity [8–17]. During the laser annealing, a shallow region at the silicon surface is rapidly heated up beyond the melting point of silicon and cools down rapidly after the laser irradiation [11–14]. However, the effective annealing time of the excimer laser annealing (ELA) process, a few hundred nanoseconds, may be too short to allow complete recovery of the crystallinity in the ion-implanted region [14]. In addition, for laser annealing, the thermal gradients during localized laser irradiation may substantially cause thermal-stress-induced defects [14–15].

In this study, formation of ultra-shallow p$^+$n junctions by using excimer laser annealing has been investigated. Various implantation conditions and annealing schemes have been examined to characterize their effects on the resultant junctions. The annealing scheme that employs excimer laser annealing with post low-temperature FA treatment is found to be quite available for fabricating excellent ultra-shallow p$^+$n junctions.

2. Experimental procedure

Phosphorus-doped n-type Si wafers, (1 0 0)-oriented, 4–7 Ω-cm, were used. A typical LOCOS isolation process was used for forming the active regions of diodes. Fig. 1(a) illustrates the schematic device structure while the formation of LOCOS isolation. Various diode sizes of 100 μm × 100 μm, 200 μm × 200 μm, 300 μm × 300 μm, and 1000 μm × 1000 μm were prepared for obtaining the area junction leakage and the peripheral junction leakage. After the patterning, a screen

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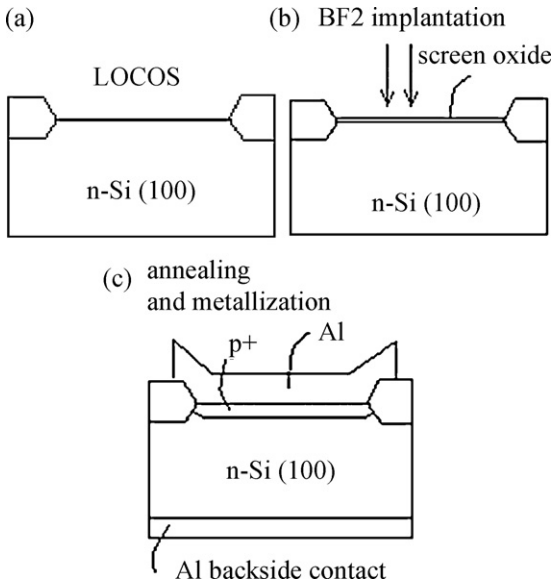

Fig. 1. (a) The schematic device structure while the formation of LOCOS isolation. (b) The schematic device structure while the BF_2^+ ion implantation. (c) The schematic device structure while the formation of metal contact pad.

oxide layer of about 10 nm thicknesses was thermally grown prior to implantation. The samples were then BF_2^+-implanted at 3 keV to doses of 1×10^{14}, 1×10^{15}, and 5×10^{15} cm^{-2}, respectively. Fig. 1(b) illustrates the schematic device structure while the BF_2^+ ion implantation. The above implantation doses were chosen for examining the practical usage of the p^+-S/D extension region and the p^+-S/D region. After the implantation, the samples were thermally treated by using different annealing schemes.**

The thermal processing includes (1) medium-temperature FA at 800 °C for 30 min, (2) ELA treatment at 300–400 mJ cm^{-2}, (3) low-temperature FA at 600 °C for 1–3 h followed by ELA treatment, and (4) ELA treatment followed by low-temperature FA at 600 °C for 1–3 h, in an N_2 ambient. For the ELA treatment, a KrF single-pulse excimer laser system of wavelength of 248 nm was used, operating at a pulse duration of 30 ns and a repetition frequency of 20 Hz. The ELA treatment was performed in a vacuum chamber at a pressure below 1×10^{-3} Torr at room temperature. And, the pulse energy density of 300, 350, and 400 mJ cm^{-2} was utilized respectively. The ELA melt depth was estimated to be about 30 nm, by using time-resolved electrical conductance measurement [18–19]. After the thermal treatment, the screen oxide layer was removed, and aluminum metallization and patterning were utilized to form the metal contact pad. Fig. 1(c) illustrates the schematic device structure while the formation of metal contact pad.

The electrical characteristics of the p^+n junctions were determined by using a HP 4145B semiconductor parameter analyzer. At least five diodes for each sample were taken to determine the average values. The sheet resistance of a junction was conducted using a four-point-probe apparatus. The leakage current density of the junction was defined at the reverse bias of 2 V and at 25 °C.

3. Results and discussion

Fig. 2 shows the dependence of sheet resistance on implantation dose for the samples treated by FA at 800 °C for 30 min, ELA treatment at 300 mJ cm^{-2}, and ELA treatment at 400 mJ cm^{-2}, respectively. By the FA at 800 °C, a sheet resistance as high as 1000 $\Omega\,\square^{-1}$ is obtained. However, the ELA treatment can result in a much smaller sheet resistance than the FA process, which manifests the high dopant activation efficiency by the ELA processing. A sheet resistance smaller than 200 $\Omega\,\square^{-1}$ is well achieved for the implantation condition of BF_2^+ (3 keV, 5×10^{15} cm^{-2}). In addition, Fig. 3 shows the SIMS (secondary ion mass spectroscopy) boron depth profile for the as-implanted specimen, the sample treated by FA at 800 °C for 30 min, and the sample treated by ELA at 400 mJ cm^{-2}, respectively, with the implantation of BF_2^+ (3 keV, 1×10^{15} cm^{-2}). No considerable dopant diffusion is found while employing the ELA treatment at 400 mJ cm^{-2}, which ensures a ultra-shallow junction by this ELA treatment.

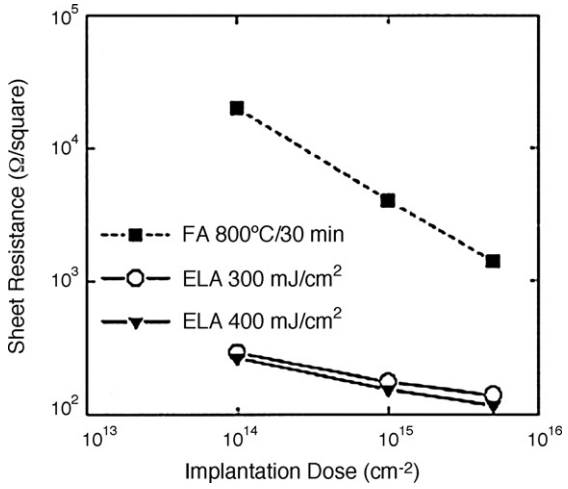

Fig. 2. Dependence of sheet resistance on implantation dose for the samples treated by FA at 800 °C for 30 mm, ELA at 300 mJ cm^{-2}, and ELA at 400 mJ cm^{-2}, respectively.

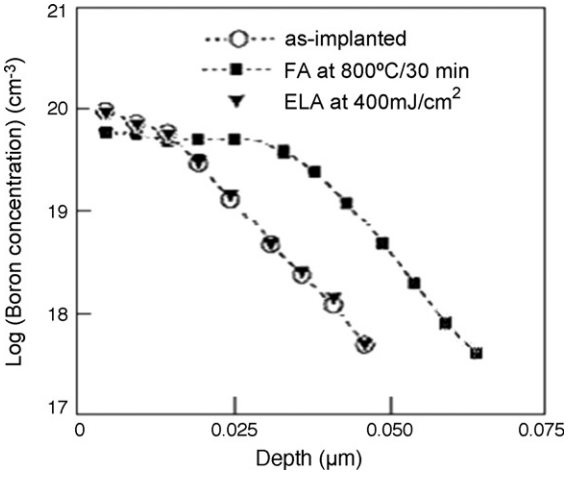

Fig. 3. The SIMS boron depth profiles for the as-implanted sample, the sample treated by FA at 800 °C for 30 min, and the sample treated by ELA at 400 mJ cm^{-2}, respectively, with the implantation of BF_2^+ (3 keV, 1×10^{15} cm^{-2}).

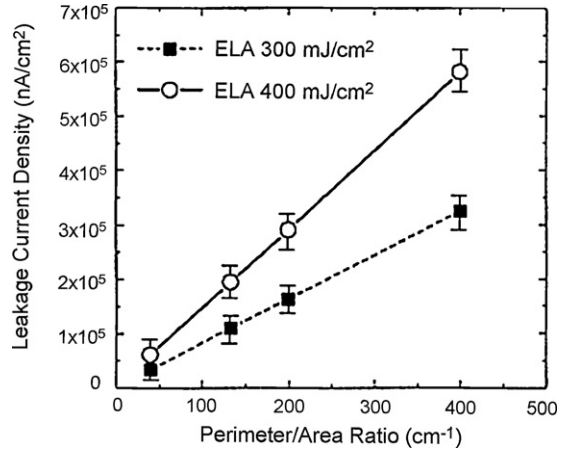

Fig. 4. The junction leakage current density as a function of perimeter/area (P/A) ratio for the samples annealed by the ELA treatment, with the implantation of BF_2^+ (3 keV, 5×10^{15} cm^{-2}).

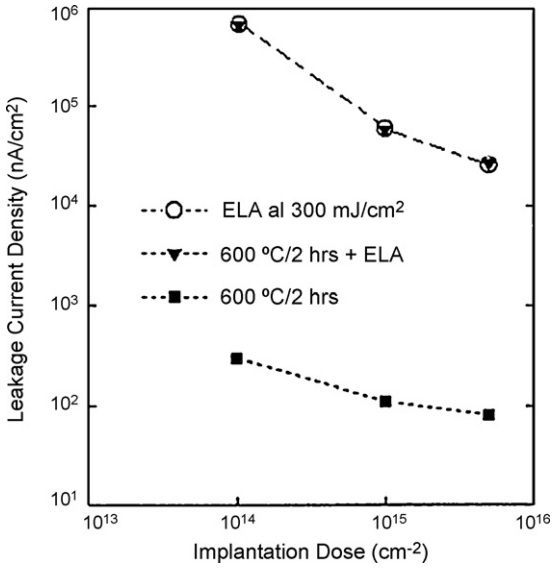

Fig. 5. Dependence of junction leakage current density on the implantation dose for the samples treated by ELA at 300 mJ cm^{-2}, by FA at 600 °C for 2 h, and by ELA treatment with pre-annealed at 600 °C for 2 h, respectively, with a diode area of 1000 μm × 1000 μm.

Moreover, Fig. 4 shows the dependence of junction leakage on perimeter/area (*P*/*A*) ratio for the samples annealed by ELA at 300 and 400 mJ cm^{-2}, respectively, with the implantation of BF_2^+ (3 keV, 5 × 10^{15} cm^{-2}). The slope of the curve implies the peripheral junction leakage, and the intercept with *Y*-axis is the area junction leakage. By using this ELA treatment at 300–400 mJ cm^{-2}, junctions with a leakage current density larger than 10^4 nA cm^{-2} are produced. And, a peripheral junction leakage current density as large as 10^3 nA cm^{-1} is caused. In addition, from Fig. 4, the resultant area junction leakage current density of the ELA-treated samples is not so large. As a result, the large junction leakage is primarily due to the leakage current generated within the junction region near the LOCOS edge.

Furthermore, prior to the ELA treatment, even though a low-temperature pre-annealing at 600 °C for 2 h is additionally done to improve the recrystallization of ion-implanted Si substrate, the resultant junctions are still poor. The low annealing temperature of 600 °C is just employed for avoiding considerable dopant diffusion. Fig. 5 shows the junction leakage current density as a function of implantation dose for the sample annealed by FA at 600 °C for 2 h, the samples treated by ELA at 300 mJ cm^{-2}, and the sample treated by pre-annealing at 600 °C for 2 h with post ELA treatment, respectively, with a diode area of 1000 μm × 1000 μm. For the sample treated by pre-FA at 600 °C for 2 h with post ELA treatment, a leakage current density larger than 10^4 nA cm^{-2} is still caused. However, the sample treated only by FA at 600 °C for 2 h can yield much better junctions than other annealing schemes mentioned in Fig. 5. Hence, the junctions formed by FA at 600 °C are degraded by the subsequent ELA treatment. As a result, in terms of the ELA-treated specimens and the samples pre-annealed at 600 °C with post ELA treatment, the poor junctions are substantially caused by the ELA treatment. Owing to the different thermal expansion coefficient of SiO_2 and silicon substrate, for the ELA rapid thermal processing, a large junction leakage may be caused within the junction region near the LOCOS edge.

Accordingly, post long-time FA at 600 °C may be available for reducing the ELA-induced junction leakage near the LOCOS edge, without causing considerable dopant diffusion. Fig. 6 shows the dependence of junction leakage current density on post low-temperature annealing time for the samples annealed by ELA at

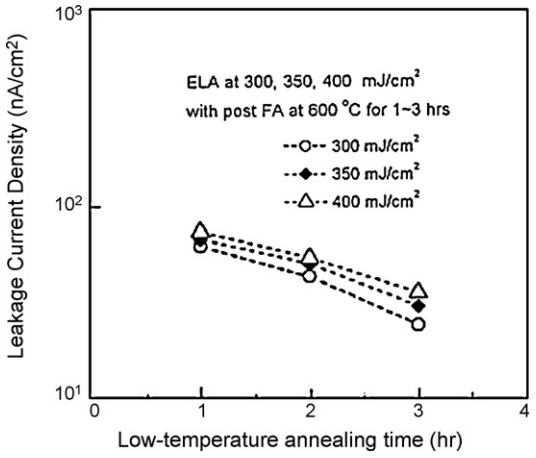

Fig. 6. Dependence of junction leakage current density on post low-temperature annealing time for the samples annealed by the ELA treatment with post FA at 600 °C, respectively, with a diode area of 1000 μm × 1000 μm and the implantation of BF_2^+ (3 keV, 5 × 10^{15} cm^{-2}).

300, 350, and 400 mJ cm^{-2}, respectively, with post FA at 600 °C, for a diode area of 1000 μm × 1000 μm. For this annealing scheme that uses ELA treatment at 300 mJ cm^{-2} followed by post FA at 600 °C for 3 h, ultra-shallow p^+n junctions with a leakage current density smaller than 20 nA cm^{-2} can be achieved. An even longer annealing time may be more helpful to the improvement of junction characteristics. As a result, the post low-temperature FA at 600 °C can significantly improve the junctions formed by ELA treatment.

Moreover, Fig. 7 also shows the dependence of junction leakage on perimeter/area (*P*/*A*) ratio for the samples treated by ELA at 300 mJ cm^{-2} with post FA at 600 °C for 1, 2, and 3 h, respectively, for the implantation of BF_2^+ (3 keV, 5 × l0^{15} cm^{-2}). From Figs. 4 and 7, when a post FA at 600 °C is performed after the ELA treatment, the junction leakage can be largely reduced. Hence, the post low-temperature FA treatment can indeed alleviate the large junction leakage generated within the junction region near the LOCOS edge.

Moreover, the peripheral junction leakage is obviously reduced with increasing the post low-temperature annealing time. With further increasing the post low-temperature annealing time to 3 h, a peripheral junction leakage current density of about 0.2 nA cm^{-1} can be obtained. Hence, the resultant junctions of the ELA-treated samples are significantly improved by the post low-temperature FA annealing. As a result, the scheme that employs ELA treatment with post low-temperature FA treatment would be efficient

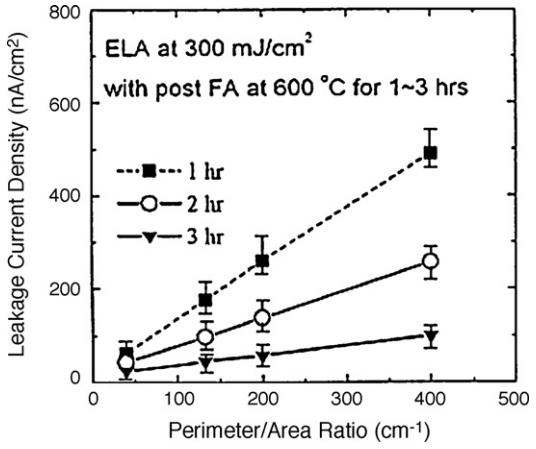

Fig. 7. The junction leakage current density as a function of *P*/*A* ratio for the samples annealed by ELA at 300 mJ cm^{-2} with post low-temperature FA at 600 °C for 1–3 h, with the implantation of BF_2^+ (3 keV, 5 × 10^{15} cm^{-2}).

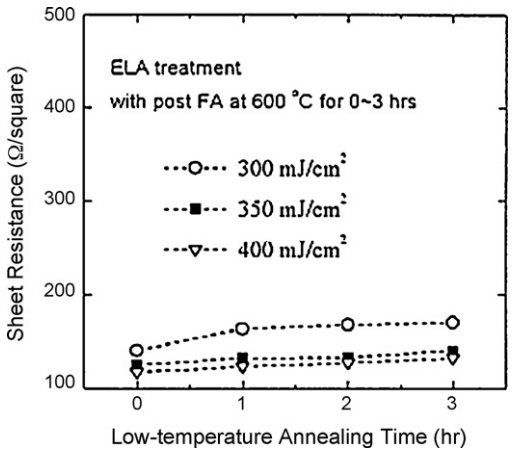

Fig. 8. The sheet resistance as a function of post low-temperature annealing time for the samples annealed by the pre-ELA treatment at 300, 350, and 400 mJ cm^{-2}, respectively, with post low-temperature FA at 600 °C, for the implantation of BF_2^+ (3 keV, 5×10^{15} cm^{-2}).

for forming excellent ultra-shallow p$^+$n junctions at low thermal budget.

Although the low-temperature FA at 600 °C is additionally performed after the ELA treatment, the resultant sheet resistance is just slightly degraded with increasing the post low-temperature annealing time. Fig. 8 shows the dependence of sheet resistance on post low-temperature annealing time for the samples annealed by the ELA treatment with post low-temperature FA treatment. As a result, even though employing post low-temperature treatment, the deactivation of the preliminarily ELA-activated boron dopant is not so serious. A sheet resistance smaller than 200 Ω □$^{-1}$ is still well available.

4. Conclusions

Formation of ultra-shallow p$^+$n junctions by using ELA treatment have been studied. No considerable dopant diffusion is caused by using these annealing processes with low thermal budget. By simply using ELA treatment at 300–400 mJ cm^{-2}, a low sheet resistance smaller than 200 Ω □$^{-1}$ can be obtained, but the resultant junction leakage current density is as high as 10^4 nA cm^{-2}. The large junction leakage is primarily due to the leakage current generated within the junction region near the LOCOS edge, which is found to be substantially induced by the ELA treatment. A post thermal treatment may be available for effectively improving the ELA-induced junction leakage. As a result, the peripheral junction leakage current density can be largely reduced from 10^3 nA cm^{-1} to about 0.2 nA cm^{-1} after receiving a post low-temperature FA at 600 °C for 3 h. And, the peripheral leakage is significantly reduced with increasing the post low-temperature annealing time. Moreover, though employing the post low-temperature long-time FA treatment, the degradation of sheet resistance is not considerable. As a result, by this promising scheme that uses the ELA treatment with post low-temperature FA treatment at 600 °C, excellent ultra-shallow p$^+$n junctions with a leakage current density lower than 20 nA cm^{-2} and a sheet resistance smaller than 200 Ω □$^{-1}$ can be well achieved.

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