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High-gain complementary inverter with InGaZnO/pentacene hybrid ambipolar thin film transistors

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Ambipolar thin film transistors (TFTs) with InGaZnO/pentacene heterostructure channels are demonstrated for a high-voltage-gain complementary metal oxide semiconductor (CMOS) inverter. The ambipolar TFT exhibits a electron mobility of 23.8 $cm^2/V\,s$ and hole mobility of 0.15 $cm^2/V\,s$ for the InGaZnO and pentacene, respectively. The thermal annealing process was also studied to adjust electron concentration reducing operating voltage of the CMOS inverter. The voltage gain achieves as high as 60 obtained in the first and third quadrants of the voltage transfer characteristic. The high performance and simple manufacture of the heterostructure CMOS inverter show promise as critical components in various electrical applications. © *2010 American Institute of Physics*. [doi:10.1063/1.3483616]

System-on-panel (SoP) concept has been proposed to integrate various functional electronic devices on a single liquid crystal display (LCD) panel for achieving high-performance, low power consumption, low cost, and more compact display products. Complementary metal oxide semiconductor (CMOS) inverter composed of both *p*-type and *n*-type thin film transistors (TFTs) plays an important role in the SoP, serving as a basic circuit building block. The CMOS inverter progress in previous literatures can be classified as two main types, including the unipolar[1–3] and the ambipolar types.[4–7] Different from the unipolar inverter, the ambipolar TFT inverter with vertical configuration of *p*-channel and *n*-channel heterostructures has received much attention in recent years, and possesses the superiorities of reduced complexity of device fabrication and good electrical behavior operated in both the first and third quadrants of transfer characteristics.[8,9] Pentacene is one of the promising candidates among *p*-channel polymer semiconductors, due to commercial availability and high hole mobility.[5] Nevertheless, the carrier mobility is always extremely low for organic *n*-type polymer field-effect transistors (FETs) even under a high voltage bias.[10,11] The ambipolar TFTs which exhibit comparable *n*-type and *p*-type mobilities will be highly desirable to demonstrate the high-performance inverters for TFT-LCD peripheral circuits. To overcome the deficiency of high-mobility *n*-channel organic polymer FETs, a concept of organic/inorganic hybrid ambipolar inverters has been proposed by Dodabalapur *et al.*[7,12] Amorphous InGaZnO (a-IGZO), as an air-stable and high-mobility *n*-type inorganic material for this demand, has great potential for ambipolar inverter applications.[13] In this study, we demonstrate an ambipolar inverter consisted of heterostructure TFT with both *n*-type a-IGZO and *p*-type pentacene channel layers, instead of the unipolar inverter with a separate *n*-channel TFT and *p*-channel TFT devices.[13]

The ambipolar inverter was composed of two same inverted-staggered TFT devices with pentacene/a-IGZO hybrid semiconductor channels. First, a n^+ heavily doped silicon substrate served as a common gate electrode was thermally grown a 100-nm-thick thermal oxide in a thermal furnace at 650 °C. The first channel layer of the heterostructure was 40-nm-thick a-IGZO film, which was deposited by a dc sputtering system and patterned through a shadow mask. The dc sputtering system has great compatibility with the existing facilities in the semiconductor industry. The target for the a-IGZO film deposition was an IGZO pellet with a component ratio where In:Ga:Zn:O was approximately 1:1:1:4. The sputtering process was carried out at room temperature under a sole argon (Ar) gas ambient pressure of 3×10^{-3} Torr with gas flow rate of 10 SCCM (SCCM denotes cubic centimeter per minute at STP). Sequentially, these samples were thermal annealed to adjust electron concentra-

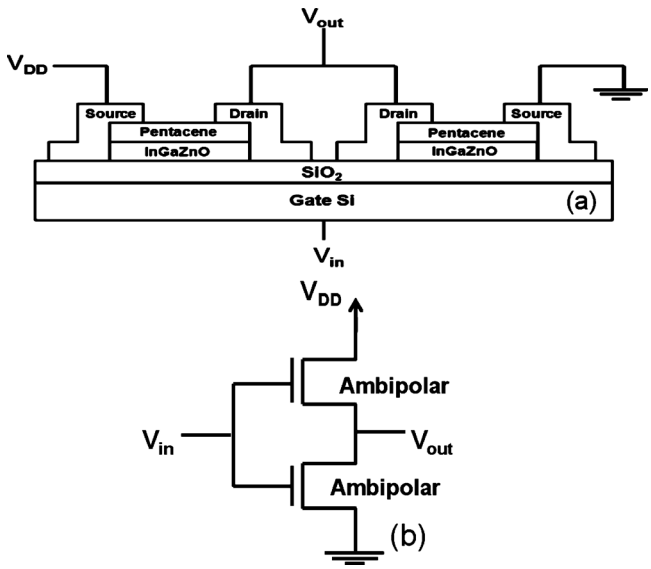

FIG. 1. (a) The schematic of a single hybrid ambipolar inverter consisting of two ambipolar TFTs with a-IGZO/pentacene heterostructure. (b) The equal inverter circuit comprising two identical ambipolar TFTs.

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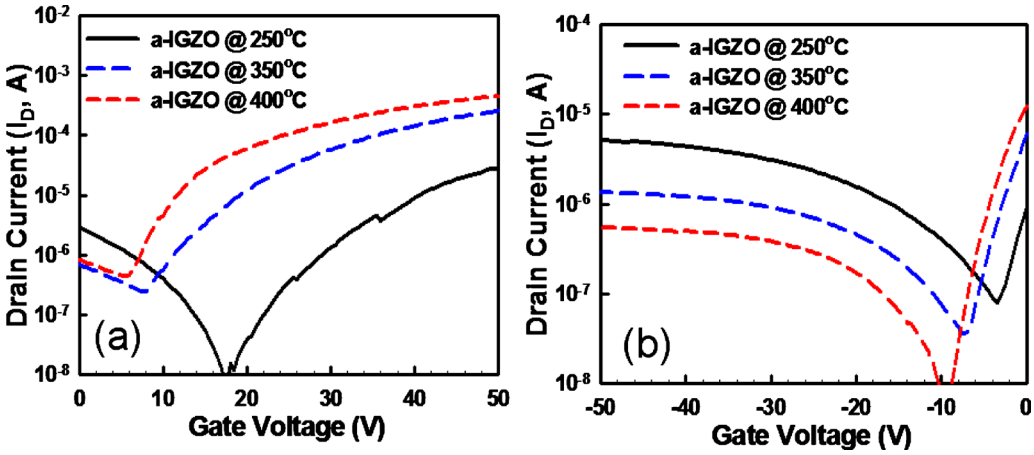

FIG. 2. (Color online) (a) The *n*-channel transfer characteristics (I_D-V_G) of ambipolar TFTs with a-IGZO/pentacene hybrid heterostructure measured at a drain voltage (V_D) of 20 V, where the a-IGZO films were thermally annealed at 250 °C, 350 °C, and 400 °C, respectively, and referred to as a-IGZO @ 250 °C, a-IGZO @ 350 °C, and a-IGZO @ 400 °C. (b) The *p*-channel transfer characteristics (I_D-V_G) of ambipolar TFTs with a-IGZO/pentacene hybrid heterostructure measured at V_D=20 V, where the a-IGZO films were thermally annealed at 250 °C, 350 °C, and 400 °C, respectively, and referred to as a-IGZO @ 250 °C, a-IGZO @ 350 °C, and a-IGZO @ 400 °C.

tion of a-IGZO film in nitrogen ambience at 250 °C, 350 °C, and 400 °C for 1 h, respectively. Then, a 40-nm-thick pentacene film serving as the second channel layer of the heterostructure was deposited on the a-IGZO layer by using thermal evaporation deposition technique. The *p*-type active region was also defined by using the same shallow mask to the a-IGZO film. It was followed that a 50-nm-thick gold (Au) layer was thermally evaporated to form source/drain electrodes of TFT devices. The schematic cross-section view of the ambipolar TFT inverter is sketched in Fig. 1(a), and the equivalent CMOS-like inverter circuit is also shown in Fig. 1(b). While studying CMOS inverter characteristics, gate electrode is common for both heterostructure TFTs and serves as the input voltage (V_{in}). To analysis the function of the ambipolar inverter in the first quadrant, the input voltage and supply voltage are positively biased. As for the inverter function in the third quadrant, the V_{in} and V_{DD} are negatively biased.

Thermal annealing was initially implemented to study the ambipolar TFT inverter, whose performance was reported to be strongly related to the balance of electron and hole transport in the ambipolar TFTs.[3,8] In this work, we performed thermal annealing processes to adjust the conduction electron concentration in the a-IGZO channel. The transfer characteristics of the ambipolar TFT with thermal annealed a-IGZO/pentacene heterostructures, referred to as a-IGZO @ 250 °C, a-IGZO @ 350 °C, and a-IGZO @ 400 °C, respectively, are showing both *n*-type and *p*-type behavior, as depicted in Figs. 2(a) and 2(b). For the *n*-channel characteristics as shown in Fig. 2(a), the induced electrons were accumulated at the interface between SiO_x and a-IGZO layer when the gate was positively biased. The electron mobility was 6.87 $cm^2/V\,s$, 11.2 $cm^2/V\,s$, and 23.8 $cm^2/V\,s$, respectively, for the annealing temperature at 250 °C, 350 °C, and 400 °C. It is clearly observed that the transfer characteristic of ambipolar TFTs shifted left, and the electron mobility and on-current were raised with increasing the annealing temperature. It can be attributed to higher annealing temperatures resulting in higher electron carrier concentration in the a-IGZO, due to the structural relaxation of a-IGZO film.[14] However, the increase in electron concentration also partially compensate the hole accumulation while the gate electrode was negatively biased, causing the decent of hole conduction current for the *p*-channel characteristics of the ambipolar

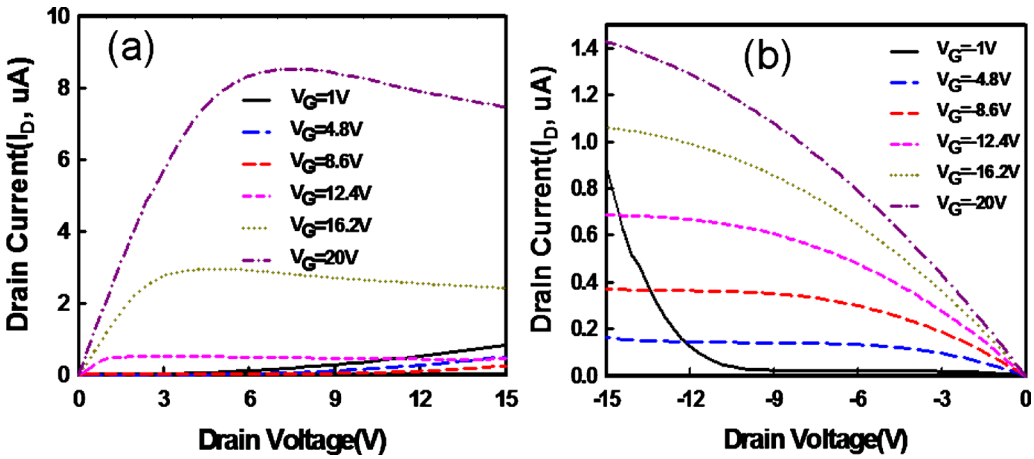

FIG. 3. (Color online) (a) The *n*-channel (electron accumulation mode) transfer characteristics (I_D-V_G) of ambipolar TFTs with a-IGZO/pentacene hybrid heterostructure with the a-IGZO thermally annealed at the highest temperature (400 °C) in this study. (b) The *p*-channel (hole accumulation mode) transfer characteristics (I_D-V_G) of ambipolar TFTs with a-IGZO/pentacene hybrid heterostructure with the a-IGZO thermally annealed at 400 °C.

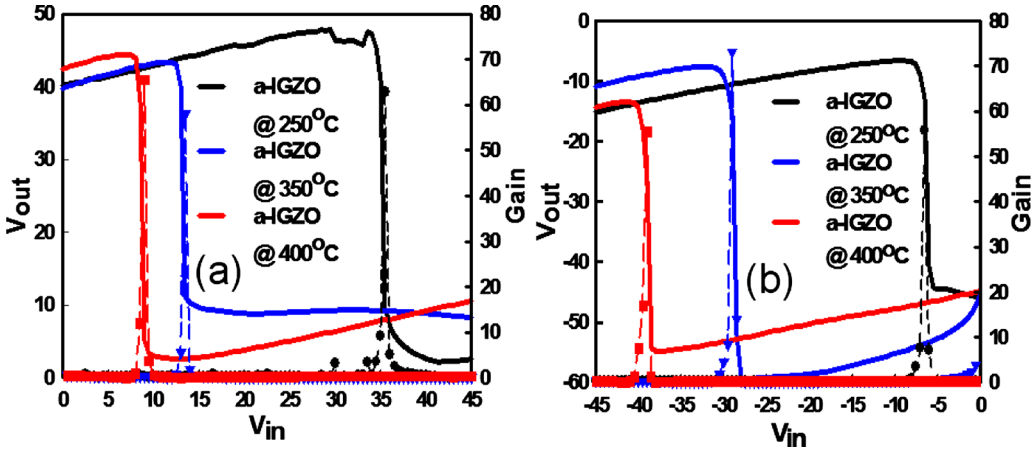

FIG. 4. (Color online) Voltage transfer curve and their corresponding gains of the ambipolar inverter with a-IGZO@250 °C, a-IGZO@350 °C, and a-IGZO@400 °C, operated in the (a) first quadrant and (b) third quadrant. The corresponding voltage gains of the ambipolar inverter operated in both the first and third quadrants are all close to 60.

TFT, as shown in Fig. 2(b). Figures 3(a) and 3(b) show the output characteristics (I_D-V_D) of the hetereostructure TFT with the a-IGZO film annealed at 400 °C. Both *n*-channel and *p*-channel behavior of the ambipolar TFT can be clearly exhibited even thought high electron concentration was formed in the a-IGZO film by an annealing temperature as high as 400 °C. Also, the high conduction current of ambipolar TFT still can be obtained in the first quadrant.

In order to characterize the hybrid ambipolar inverter, two ambipolar TFTs were interconnected to form a single inverter as shown in Fig. 1(a). The common gate electrode of the ambipolar inverter acts as the input node (V_{in}). For the inverter operation in the first quadrant, the supply voltage (V_{DD}) and V_{in} were biased positively. The magnitude of V_{DD} was set to 60 V. The voltage gains were defined by $\partial V_{out}/\partial V_G$, and the operating voltages were defined at V_G related to the highest voltage gain. Experimental measurement results of output voltage (V_{out}) versus V_{in} were plotted in Fig. 4(a). The operating voltages of the ambipolar inverter with 250 °C, 350 °C, and 400 °C annealed a-IGZO films were 35.5 V, 13.5 V, and 9 V, respectively, and the corresponding voltage gains of each hybrid inverters were 62, 58, and 65 in order. It was obviously observed that the operating voltage decreases while the ambipolar inverter consisted of the a-IGZO film thermally annealed at higher temperatures. The reduction in operating voltage in the first quadrant can be attributed to the increase in *n*-channel carrier concentration in the heterostructure TFTs. For the operation in the third quadrant, the V_{DD} was set to −60 V and the V_{in} was negatively biased, as shown in Fig. 4(b). The operating voltages of ambipolar inverter were −6.5 V, −29 V, and −39 V, respectively, for the ambipolar inverter with 250 °C, 350 °C, and 400 °C annealed a-IGZO films, and the voltage gains all were about 60. The evolution trend on the curves of V_{in} versus V_{out} with increasing annealing temperatures is as similar as the one shown in I_D-V_G cures of the heterostructure TFTs, which also can be attributed to the reduction in hole by the increased background electron concentration. Since the voltage gains in the third quadrant were independent of the annealing temperature of a-IGZO film, the hybrid ambipolar inverter can operate in both the first and third quadrants, and exhibit high voltage gains.

In summary, the proposed ambipolar TFT using a-IGZO/pentacene bilayer films has exhibited both *n*- and *p*-channel conduction behavior with a electron mobility of 23.8 and hole mobility of 0.15 $cm^2/V\,s$, respectively. Furthermore, two ambipolar TFTs also were interconnected to study the electrical characteristics of the inverter circuit. Thermal annealing processes at a series of temperatures were implemented to effectively improve a-IGZO film quality and adjust the carrier concentration of the a-IGZO film. Thus, the operating voltage of the inverter as low as 9 V with the voltage gain of about 60 in both the first and the third quadrant regions have been achieved in this work. The hybrid TFT-based inverter demonstrated great potential for the high-voltage-gain complementary circuit applications.

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