3–10 GHz ultra-wideband low-noise amplifier with new matching technique

C.-P. Liang, C.-W. Huang, Y.-K. Lin and S.-J. Chung

A low-power and low-noise amplifier with a new input- matching technique using 0.18 μm CMOS technology for ultra-wideband applications is presented. A proposed broadband input match can be acquired easily by selecting an appropriate width of the transistor, which will effectively avoid the usage of the low-Q on-chip inductors in the input network. Moreover, demonstrated is the feasibility of the inter-stage resonator to accomplish bandwidth enhancement without additional power consumption. The IC prototype achieves good performances such as a power gain of 16.2 dB, a better than 10 dB input return loss, and 2.3 dB minimum noise figure while consuming a DC core power of only 6.8 mW.

Introduction: Ultra-wideband (UWB) systems operate over a wide range of frequencies from 3.1 to 10.6 GHz, and the realisation of the UWB receiver suffers serious challenges, especially for the low-noise amplifier (LNA). It must provide a fine wideband 50 Ω input matching with flat gain over the entire bandwidth, low noise, good linearity, and low power consumption. In general, the distributed configuration [1] and *LC* input network [2, 3] are attractive for their ultra-wide bandwidth; however, major drawbacks are the larger chip area and worse noise figure owing to use of low-Q on-chip inductors in the input network. To overcome the above-mentioned drawbacks, in this Letter we propose a new inductorless input-matching technique, which is based on a source-degenerated structure to achieve superior noise performance. On the other hand, the common-source stage with *LC* tank load can be adopted to enhance the bandwidth of the amplifier by appropriately tuning the resonator frequency of the *LC* tank load; however, it is unavoidable to increase DC power consumption, which may make this circuit unsatisfactory for low-power application. In this Letter, we utilise the inter-stage resonator to improve power gain bandwidth without using the common-source stage. As a consequence, DC power reduction and bandwidth enhancement will be attained simultaneously.

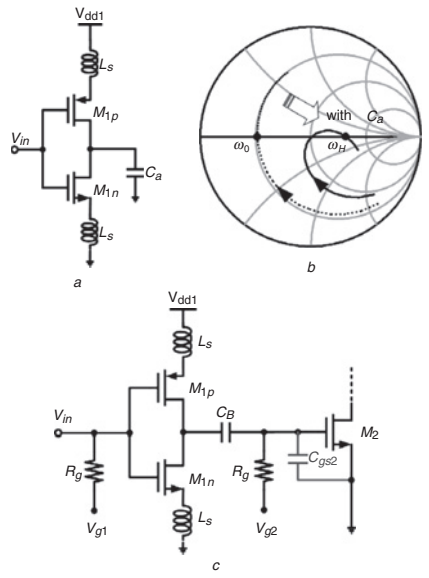

Fig. 1 *Principle of proposed input matching circuit*

a Current-reused configuration with additional capacitor C_a
b Frequency behaviour of input impedance with and without capacitor C_a
c Proposed broadband input match circuit with suitable size of transistor M_2

Circuit design: The proposed input matching circuit, as shown in Fig. 1*a*, utilises the current-reused configuration with an additional capacitor C_a to achieve the design of low-power characteristic and wideband match. Fig. 1*b* depicts the frequency behaviour of the input impedance on the Smith chart. It is obvious that the transistor components M_{1n} and M_{1p} give rise to a parasitic effect such as a Miller parasitic capacitor; therefore, an extra parallel resonant frequency ω_H in Fig. 1*b* can be generated by introducing only an additional capacitor C_a. Owing to the presence of the resonant frequency Ω_H, a loop surrounding the 50 Ω matching point is formed on the Smith chart. As we will see, a broadband input match in the intended frequency range can be acquired by selecting an appropriate value of the capacitor C_a. In this study, we are inclined to employ the parasitic capacitor C_{gs2} of the amplifier stage M_2, as shown in Fig. 1*c*, to substitute for the capacitor C_a. Fig. 2*a* shows the relation between input return loss and frequency for different widths of transistor M_2. It can be observed that the input-matching performance will be ameliorated when the width of transistor M_2 increases; however, an overlarge width will bring about deterioration in the noise figure, as demonstrated in Fig. 2*b*. This is because an overlarge capacitor C_a will diminish the power gain of the current-reused amplifiers M_{1n} and M_{1p} to indirectly worsen the noise property of the proposed UWB LNA. As a consequence, a trade-off should be carefully considered so as to make an optimum design.

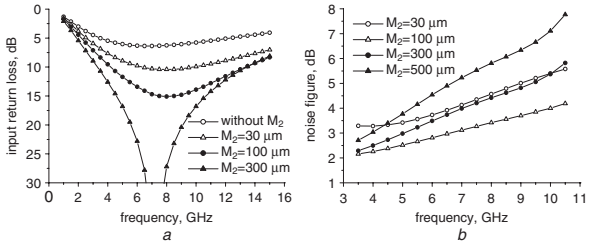

Fig. 2 *Simulated input return loss and noise figure for different widths of transistor M_2*

a Input return loss
b Noise figure

The 3–10 GHz UWB LNA fabricated by 0.18 μm TSMC CMOS process is shown in Fig. 3. It is known that maximum power transfer will occur by means of conjugate impedance matching. The inter-stage resonator (C_2, L_1) in Fig. 3 accomplishes bandwidth extension owing to the conjugate impedance matching. Fig. 4 shows the simulated impedances of Z_1 (solid line) and Z_2 (dashed line) (see Fig. 3*a*) from 4 to 12 GHz. The best conjugate impedance matching is designed near 9.6 GHz by using the inter-stage resonator to improve the bandwidth without additional power consumption. In addition, a larger substrate resistor R_B is adopted in the RF MOS device to obstruct undesired noise power from the substrate port, and the buffer transistor M_3 with a 50 Ω resistive load R_o in the proposed UWB LNA is employed to achieve output matching for testing purposes.

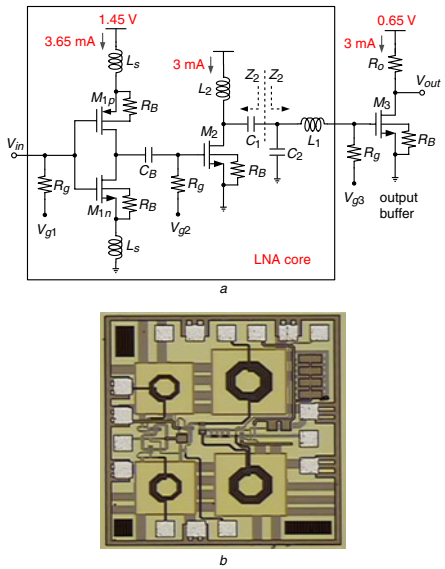

Fig. 3 *Complete schematic and die microphotograph of proposed UWB LNA*

a Complete schematic
b Die microphotograph

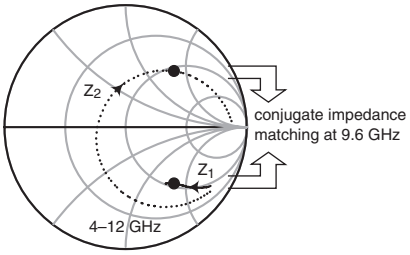

Fig. 4 *Input reflection coefficients on Smith chart for impedances Z_1 (solid line) and Z_2 (dashed line) shown in Fig. 3a*

Results: The UWB LNA chip is measured by on-wafer probing and the total DC core power dissipation is 6.8 mW. A die microphotograph of the fabricated LNA is shown in Fig. 3*b*, with a die area including pads of 0.81 × 0.81 mm^2. The S-parameters of the designed LNA are measured using an Agilent E8361A PNA network analyser. The noise figure (NF) is measured using an Agilent N8975A noise figure analyser with Agilent 346C noise source. Simulated and measured results of power gain and input return loss are depicted in Fig. 5. The small signal peak gain is 16.2 dB with 3 dB bandwidth of 7 GHz from 3 to 10 GHz and input return loss is better than 10 dB in the operation bandwidth. The simulated and measured noise figure at the same bias condition is also depicted in Fig. 5. It is seen that the minimum value of NF is equal to 2.3 dB at 3.5 GHz. The proposed LNA performance is compared with recently published CMOS LNAs and summarised in Table 1 [4–8].

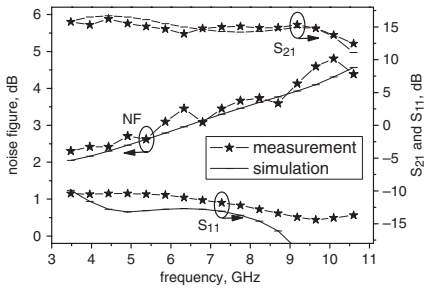

Fig. 5 *Measured S-parameters and noise figure of proposed UWB LNA*

Table 1: UWB LNA performance summary

Ref.	Tech.! (μm)	BW (GHz)	G_{max} (dB)	NF_{min} (dB)	P_{diss} (mW)	Area (mm^2)	*FOM/Area
[1]	0.13	0–12.1	18.7	3	27.6	0.88	4.29
[2]	0.18	3–4.8	13.9	4.7	14.6	0.95	0.33
[3]	0.13	2.2–9	11.3	3.9	30	0.68	0.87
[4]	0.18	2–12	11.8	3.1	22.7	0.45	3.66
[5]	0.13	0.1–10	17	5.3	60	0.64	0.76
[6]	0.13	3–10.35	12.5	3.3	7.2	0.77	4.92
[7] +	0.13	4.7–11.7	12.4	2.9	13.5	–	–
[8]	0.18	0–16	10	3.6	21	1.19	1.57
TW	0.18	3–10	16.2	2.3	6.8	0.66	14.4

+ simulation results ! CMOS

* $FOM = \frac{BW[GHz]\ G_{max}[lin]}{(NF_{min}[lin]-1)\ P_{diss}[mW]\ Area[mm^2]}$

Conclusion: The UWB LNA with a new input-matching concept has been fabricated by using 0.18 μm CMOS process. A superior noise performance with easily be achieved by the usage of the proposed inductorless input-matching technique. The inter-stage resonator is employed for low power application to accomplish gain bandwidth extension without extra DC power dissipation.

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One or more of the Figures in this Letter are available in colour online.

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