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LETTER

A −68.5 dB IM3 Low-Voltage CMOS Transconductor with Wide Tuning Range

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SUMMARY A CMOS transconductor for multi-mode application is presented. The transconductor includes a voltage-to-current converter and a current multiplier. Voltage-to-current conversion employs linear region MOS transistors, and the conversion features high linearity over a wide input swing range. The current multiplier, which operates in the weak inversion region, provides a wide transconductance tuning range without degrading the linearity. The transconductor was designed and fabricated in the TSMC 0.18-μm CMOS process. The results show the transconductance tuning ratio of 23 and the IM3 performance of −68.5 dB.

key words: *transconductor, IM3, CMFF, tuning*

1. Introduction

A circuit that converts the voltage applied to the input terminals into current at output nodes is generally referred as a voltage-to-current converter or a transconductor. The transconductor is a basic building block in analog VLSI applications, including continuous-time Gm-C filters, voltage controlled oscillators and continuous-time delta-sigma modulators [1], [2]. The transconductance would be an important parameter to the resonant frequency of these applications. Also, the linearity of the voltage-to-current should be maintained owing to the open loop design in the applications.

The Recent trend in system-on-a-chip solutions is to include multiple applications in a high-integration system. Therefore, cost efficiency of VLSI implementations has been greatly enhanced with the emergence of multi-mode technology. To meet different specifications in multi-mode technology, new basic analog building blocks should be designed. Therefore, the transconductor requires a wide tuning range for multi-mode technology, and the linearity should be well maintained.

2. Proposed Transconductor Circuit and Performance

The transconductor using triode region transistors have been reported in the past decade [3]–[5]. The transconductance is proportional to the $K_{lin}V_{DS}$, where K_{lin} is the device parameter of input transistors and V_{DS} is the drain-to-source voltage. However, these circuits behave limited tuning range and require extra common-mode feed-forward (CMFF) circuit.

Figure 1 shows the proposed transconductor circuit. The voltage-to-current conversion is composed of transistors M1 to M6, M17 and M18. The conversion is designed based on the flipped voltage follower (FVF) [6], which is composed of transistors M5 and M6. The main voltage-to-current conversion is provided by transistors M1 and M2 in the linear region. The gate voltage of transistor M5 is used to provide a bias voltage for transistors M3 and M4, and ensure the linear region operation of transistors M1 and M2. Thus, the drain voltage of transistors M1 and M2 would be kept to a constant value. In the circuit, the input transistors operate in the linear region, rather than the saturation region proposed in [6]. Besides, the source of transistors M1 and M2 is fixed to a constant value owing to the FVF feedback loop. From analysis, it is shown that the low impedance can be obtained at the source of transistor M6. The structure suppresses the variation at the source of transistors M1 and M2, and thus the circuit would operate under class AB topology. To obtain the voltage-to-current characteristic of our proposed circuit, the input differential voltages at the gate of transistors M1 and M2 can be written as $V_{i+} = V_{cm} + (v_d/2)$ and $V_{i-} = V_{cm} - (v_d/2)$, where V_{cm} is the input common-mode voltage and v_d is the input differential-mode voltage. The currents which flow through transistors M1, M2, and M6 are expressed by

$$I_{D1} = K_1\left[\left(V_{cm}+\frac{v_d}{2}-V_{th}-V_X\right)(V_{D1}-V_X)-\frac{1}{2}(V_{D1}-V_X)^2\right] \quad (1)$$

$$I_{D2} = K_2\left[\left(V_{cm}-\frac{v_d}{2}-V_{th}-V_X\right)(V_{D2}-V_X)-\frac{1}{2}(V_{D2}-V_X)^2\right] \quad (2)$$

$$I_b = \frac{1}{2}\left[K_6(V_{cm}-V_X-V_{th})^2\right] \quad (3)$$

where V_{D1} and V_{D2} are the drain voltages of transistors M1 and M2, respectively, and V_x is the source voltage of transistor M6. The aspect ratios of transistors M1, M2, and M6 are set to the same value. In addition, the aspect ratios of M3 and M4 are twice the aspect ratios of M1 and M2. Note that $V_{D1} = V_{GS5} - V_{GS3}$ and $V_{D2} = V_{GS5} - V_{GS4}$. We assume V_{GS5} would be very close to V_{GS6} since transistors M1 and M2 work in the linear region and a small drain current is produced. Moreover, a slightly larger aspect ratio of transistor M5 can be designed to support this assumption. V_{GS3} and V_{GS4} could be obtained by using the square law equation of saturated transistors. Therefore,

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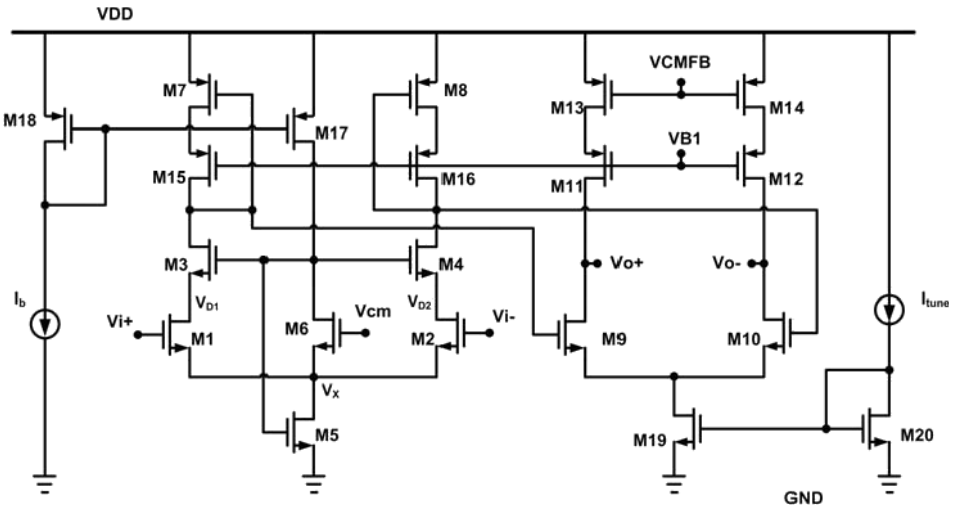

Fig. 1 The implementation of the proposed transconductor circuit.

$V_{D1} = V_{GS6} - V_{GS3} = (2I_b/K)^{1/2} - (I_{D1}/K)^{1/2}$ and $V_{D2} = V_{GS6} - V_{GS4} = (2I_b/K)^{1/2} - (I_{D2}/K)^{1/2}$. Also, from (3), $V_{cm} - V_X - V_{th} = (2I_b/K)^{1/2}$ and $V_X = V_{cm} - V_{th} - (2I_b/K)^{1/2}$. By inserting these results into (1), with only one variable I_{D1} left in the equation, I_{D1} can be solved and obtained. Similarly, I_{D2} can be solved from (2) as well. The currents I_{D1} and I_{D2} would be a function of the input differential voltage. To analyze the linearity of the output current $i_{out} = I_{D1} - I_{D2}$ against the input voltage under the differential structure, a Taylor series expansion has been used, where the relationship could be summarized by

$$i_{out} = a_{1,out}v_d + a_{2,out}v_d^2 + a_{3,out}v_d^3 + a_{4,out}v_d^4 + L \tag{4}$$

$$a_{1,out} = G_m = \frac{1}{2}K\left(\alpha - \frac{\beta^2 - 3\beta\alpha + \alpha^2}{\sqrt{\alpha^2 + 2\beta\alpha - \beta^2}}\right) \tag{5}$$

$$a_{3,out} = -\frac{3(\beta - 2\alpha)^3\,\alpha}{2(\beta - \alpha)(\beta^2 - 2\alpha\beta - \alpha^2)^3} \tag{6}$$

where $K1 = K2 = K6 = K$, $\alpha = \sqrt{\dfrac{2I_b}{K}}$ and $\beta = V_{cm} - V_{th}$

In (4), the output current can be seen to be a nonlinear function of the input differential voltage. Since the even-order harmonic terms could be cancelled out by the differential structure, the third-order harmonic distortion would become the dominant component. We can find that to minimize the third-order distortion term, the following equation should be satisfied.

$$\sqrt{\frac{2I_b}{K_6}} = \frac{V_{cm} - V_{th}}{2} \tag{7}$$

If the above condition is held, only the fifth or higher order distortion terms are left in (4) and these nonlinear terms have very low contribution to the proposed circuit. The input common-mode voltage is detected by using extra resistors, and the resistors are designed without degrading the input signal performance. In addition, this circuit would not need extra common-mode feedfoward (CMFF) circuit. This is because the input common-mode voltage is directly sensed at the gate terminal of transistor M6. If the input common-mode voltage is changed, the variation would appear at the source node of transistor M6, that is, the source nodes of transistors M1 and M2. Therefore, the common-mode current would not be changed since the gate and source voltage of transistors M1 and M2 vary in the same direction simultaneously.

Low distortion voltage-to-current conversion is obtained under the defined bias conditions, and furthermore, a transconductance tuning ability can be added with a high linearity current multiplier circuit, which is composed of transistors M7 to M10 in Fig. 1. The transistors would operate in the weak inversion region while proper sizing is required. For a MOSFET operating in the weak inversion region with V_{DS} larger than a few times the thermal voltage U_T, its current exhibits an exponential dependence on V_{GS} and can be expressed as

$$I_D = I_{D0}\frac{W}{L}\exp\left(\frac{V_{GS}}{nU_T}\right) \tag{8}$$

where W and L are the width and the length of the transistor, respectively, I_{D0} is the reverse saturation current, n is the subthreshold slope factor, and U_T is the thermal voltage. From the above equation, we can find that

$$V_{SG7} = nU_T \ln\left(\frac{I_{D7}}{I_{D0}}\frac{L_7}{W_7}\right) \tag{9}$$

$$V_{SG8} = nU_T \ln\left(\frac{I_{D8}}{I_{D0}}\frac{L_8}{W_8}\right) \tag{10}$$

The device sizes of transistors M7 and M8 are set to be the same. We can obtain from the linear voltage-to-current conversion circuit, $I_{D7} = I_1 + i_i$ and $I_{D8} = I_1 - i_i$. Therefore,

$$\Delta V = V_{SG7} - V_{SG8} = V_{GS9} - V_{GS10} = nU_T \ln\left(\frac{I_1 + i_i}{I_1 - i_i}\right) \tag{11}$$

The subthreshold slope factor n is equal to (C_{ox} +

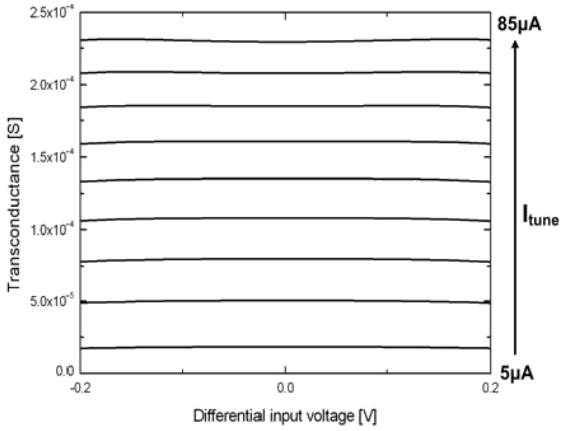

Fig. 2 The simulated G_m range of the proposed transconductor.

$C_{depl})/C_{ox}$ [7], where C_{ox} and C_{depl} are the gate and depletion capacitance per unit area, respectively. We can find that the factor C_{ox} is almost equal for NMOS and PMOS devices from the process device model. Besides, C_{depl} would be changed according to the size of MOSFET, and we can design a specified ratio of NMOS and PMOS to obtain the same capacitance. The current output from the differential pair of transistors M9 and M10 can be expressed by

$$I_{D9} = \frac{2I_2}{1 + e^{\frac{\Delta V}{nU_T}}} = \frac{2I_2}{1 + \left(\frac{I_1 + i_i}{I_1 - i_i}\right)} = I_2 - \frac{I_2}{I_1} i_i \tag{12}$$

$$I_{D10} = \frac{2I_2}{1 + e^{\frac{-\Delta V}{nU_T}}} = \frac{2I_2}{1 + \left(\frac{I_1 - i_i}{I_1 + i_i}\right)} = I_2 + \frac{I_2}{I_1} i_i \tag{13}$$

Finally, the output current i_o is given by

$$i_o = I_{D10} - I_2 = I_2 - I_{D9} = \frac{I_2}{I_1} i_i \tag{14}$$

With the weak inversion characteristic, the input voltage should be logarithmically determined at first and through the exponential function, the output current would have a linear relationship. In other words, the output current is equal to a scaled version of the input current where the scaling factor is determined by the ratio of two bias currents. In our proposed circuit, the output current can be tuned by tuning the bias current I_2 at the output stage. The high linearity characteristic can also be maintained when the circuit operates from the weak inversion region to the moderate inversion region, and thus the tuning range could be further extended. The transconductor was designed in the TSMC 0.18-μm Deep N-Well CMOS process, with a 1-V supply. The power consumption is less than 0.24 mW. Figure 2 shows the large signal simulation of the transconductance with respect to the function of applied differential input voltage. With the scalable tuning current, the tuning range of 10 μS to 230 μS can be obtained. The chip photograph is shown in Fig. 3 with the active area less than 0.03 mm^2. The third-order inter-modulation (IM3) distortion measured with two sinusoidal tones of 400 mV_{pp} amplitude at the transconductance of 100 μS is shown in Fig. 4. The IM3 is shown to be less than −68.5 dB at a frequency of 2 MHz. When we increase the transconductoance value to 230 μS, the IM3 is kept at −68.3 dB. The IM3 becomes −70 dB at the transconductance of 10 μS. The IIP3 can be obtained by using the IM3 results in different input signal swings. In this design, the IIP3 is 28 dBm. However, due to the limited supply voltage of 1 V, the P1 dB is 6.5 dBm.

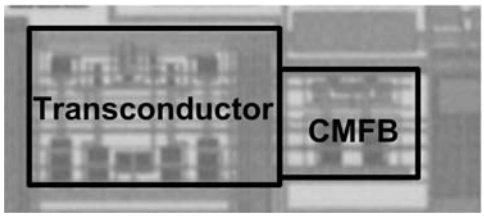

Fig. 3 Die photograph.

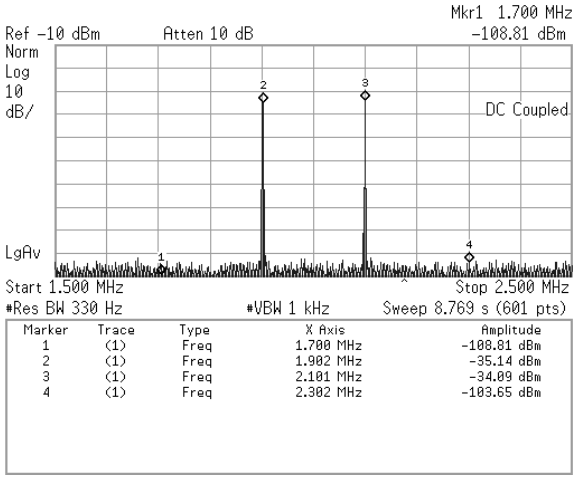

Fig. 4 The measured IM3 of the proposed transconductor.

The circuit works under the differential fashion, and thus the noise performance is highly dependent on the aspect ratio of input transistors M1 and M2. In this circuit, a large aspect ratio of input transistors is designed and the measured input-referred noise of the transconductor is 9 nV/$\sqrt{\text{Hz}}$ at 1 MHz.

3. Paragraphs and Itemizations

A CMOS implementation of a wide tuning range transconductor is presented. Linear region MOS transistors are used to perform the voltage-to-current conversion and the third-order harmonic distortion term can be minimized by providing suitable bias conditions. The current multiplier makes use of weak inversion region MOS transistors to achieve high linearity. The theoretical analysis of the high performance operation and the results are provided to demonstrate the validity of the transconductor.

Acknowledgments

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