Parallel-RC Feedback Low-Noise Amplifier for UWB Applications

Kuang-Chi He, Ming-Tsung Li, Chen-Ming Li, and Jenn-Hwan Tarng, *Senior Member, IEEE*

***Abstract*—A two-stage 3.1- to 10.6-GHz ultrawideband CMOS low-noise amplifier (LNA) is presented. In our design, a parallel resistance–capacitance shunt feedback with a source inductance is proposed to obtain broadband input matching and to reduce the noise level effectively; furthermore, a parallel inductance–capacitance network at drain is drawn to further suppress the noise, and a very low noise level is achieved. The proposed LNA is implemented by the Taiwan Semiconductor Manufacturing Company 0.18-μm CMOS technology. Measured results show that the noise figure is 2.5–4.7 dB from 3.1 to 10.6 GHz, which may be the best result among previous reports in the 0.18-μm CMOS 3.1- to 10.6-GHz ultrawideband LNA. The power gain is 10.9–13.9 dB from 3.1 to 10.6 GHz. The input return loss is below -9.4 dB from 3.1 to 15 GHz. It consumes 14.4 mW from a 1.4-V supply voltage and occupies an area of only 0.46 mm^2.**

***Index Terms*—Broadband, complimentary metal–oxide–semiconductor (CMOS) low-noise amplifier (LNA), feedback, ultrawideband (UWB).**

I. Introduction

In RECENT YEARS, ultrawideband (UWB) systems have attracted more interest due to their capability of transmitting data with a high data rate and low power consumption. For the IEEE 802.15.3a standard, the allocated band of UWB is between the 3.1- and 10.6-GHz frequency range [1]. The wideband low-noise amplifier (LNA) for a wireless front-end RF receiver is a critical block, which needs to fulfill several requirements, such as broadband input matching, sufficient power gain, low-noise figure (NF), etc.

Several major types of UWB CMOS LNAs have been reported in literature [1]–[9]. The distributed amplifier (DA) provides good wideband input matching and flat gain; however, it consumes more power and chip area. The resistive shunt feedback is a well-known wideband technique, which provides wideband input matching but increases NF due to the local feedback [1]. The inductive degeneration can only provide narrow-band input matching, but it can achieve better noise performance; therefore, it needs other technology to extend the bandwidth [3]. Another technology is to use a multistage input filter for broadband input matching [4]. However, the input filter insertion loss degrades the LNA's NF, and a large chip area is unavoidable. According to the points discussed above, the parallel resistance–capacitance shunt feedback with a source inductance is proposed to obtain the broadband input matching and to reduce the noise level effectively. The parallel LC network at drain is drawn to further suppress the high-frequency noise, and a low noise level is achieved. Moreover, the input stage in cascade with cascode topology can provide broadband power gain (3.1–10.6 GHz) with both relatively low power consumption and a small chip area.

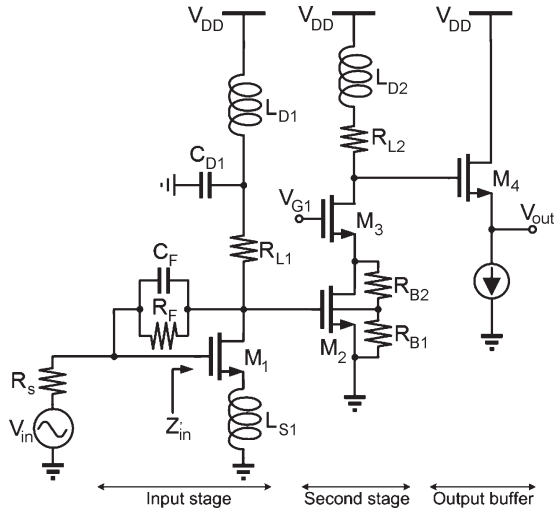

Fig. 1. Proposed UWB LNA.

II. Circuit Design and Analysis

The proposed wide-band LNA is depicted in Fig. 1. It consists of an input stage, a cascode second stage, and an output buffer. The output buffer is a simple source follower that is added for measurement purposes only.

A. Input Stage

The input stage provides the broadband power and noise matching. The input impedance $Z'_{\rm in}$ looking into the gate of transistor M_1 (as seen in Fig. 1) is

$$Z'_{\rm in} = g_{m1}\frac{L_{S1}}{C_{gs1}} + sL_{S1} + \frac{1}{sC_{gs1}} \tag{1}$$

where g_{m1} and C_{gs1} are the transconductance and the gate-to-source capacitance of the transistor M_1, respectively. From

Manuscript received August 2, 2009; revised December 10, 2009; accepted February 11, 2010. Date of publication June 28, 2010; date of current version August 13, 2010. This work was supported in part by the National Science Council, R.O.C., under Contract NSC97-2219-E-009-012. This paper was recommended by Associate Editor A. I. Karsilayan.

The authors are with the Department of Communication Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan (e-mail: hkc.cm96g@nctu.edu.tw).

Digital Object Identifier 10.1109/TCSII.2010.2050943

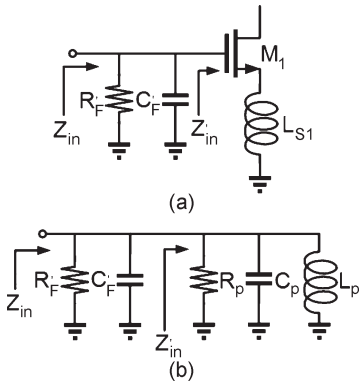

Fig. 2. (a) Miller equivalent circuit. (b) Series converted to parallel of the equivalent circuit.

Fig. 1, using Miller's theorem to convert the input stage to that shown in Fig. 2(a), we obtain $R'_F = R_F/(1 + A_v)$ and $C'_F = C_F(1 + A_v)$, where A_v is the voltage gain from gate to drain and is equal to

$$A_v = \frac{(sC_{gs1}Z'_{in} - g_{m1}Z_F)\,Z_L}{sC_{gs1}Z'_{in}(Z_F + Z_L)}. \tag{2}$$

Equation (1) presents a series-RLC network. For simplicity, the series combination of R, L, and C can be converted to the equivalent parallel circuit shown in Fig. 2(b),[1] where R_p, L_p, and C_p can be derived as

$$R_p = \frac{R^2 + (\omega L - 1/\omega C)^2}{R} \tag{3}$$

$$L_p = \frac{R^2 + (\omega L - 1/\omega C)^2}{\omega^2 L} \tag{4}$$

$$C_p = \frac{1}{\omega^2 C\,(R^2 + (\omega L - 1/\omega C)^2)}. \tag{5}$$

Thus, the input impedance Z_{in} is approximated as

$$Z_{\text{in}} = (R'_F \| R_p) \| \left(sL_p \| \frac{1}{s\,(C'_F + C_p)} \right). \tag{6}$$

Referring to (6), we can make the following observations. First, the form of (6) clearly shows that the input impedance is purely resistive at resonance. Thus, a proper choice of g_{m1}, L_{S1}, R_F, and C_F yields a 50-Ω part. In (6), C'_F makes inductive reactance of Z_{in} closer to capacitive reactance. In other words, C'_F makes the imaginary part of Z_{in} closer to zero (see Fig. 3). Thus, Z_{in} is dominated by $R'_F \parallel R_p$ during several gigahertz. As a result, the optimal choice of g_{m1}, L_{S1}, R_F, and C_F ensures broadband input matching condition. Second, the resistive component at the input is the parallel combination of R'_F and R_p, and the local feedback noise is inversely proportional to R_F; hence, we can select the larger feedback resistor R_F in order to suppress noise. The simulation

[1]The quality factor Q of the IC component is quite low, that is, the impedance curve of the IC component is not so sharp; therefore, we can expect that the conversion range is wide.

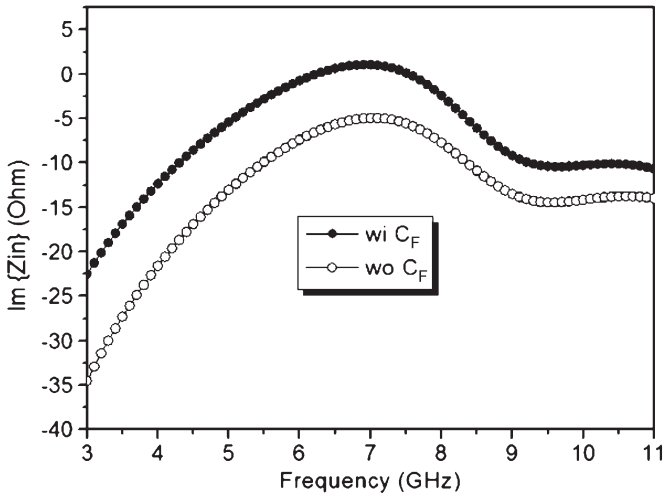

Fig. 3. Simulation effect of C_F on input impedance.

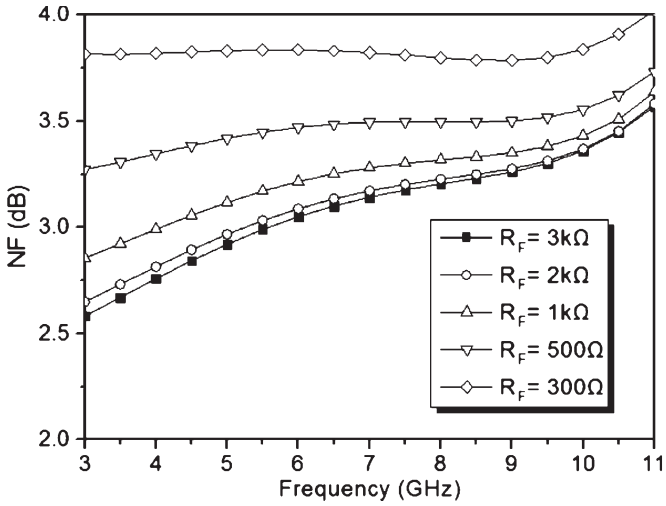

Fig. 4. Simulation effect of the RF on the NF.

effect of R_F on the NF is shown in Fig. 4. Third, different from the conventional inductive degeneration [3], the design in this study only uses a small inductor L_{S1} for input matching, so the core area can be reduced. From the above observations, the proposed input stage can provide wideband input matching and better noise performance with a relatively small area. Moreover, a general noise figure of a common-source amplifier is linearly proportional to the frequency in 3–10 GHz. The noise factor of input stage F_{in} is equal to

$$F_{\text{in}} = \frac{V^2_{n,o1}}{A^2_v}\frac{1}{4kTR_S} \tag{7}$$

where $V_{n,o1}$ represents the total noise power at the output of the input stage, which includes the thermal noise of R_S, R_F, R_{L1}, and M_1. The output noise power contributed by R_F and M_1 is inversely proportional to f. As the frequency goes higher, A_v becomes low, and the output noise power contributed by R_F and M_1 is abated; therefore, R_{L1} plays a critical role in increasing F_{in} due to low A_v at a high frequency. Thus, we suppress the high-frequency noise of R_{L1} to maintain a low

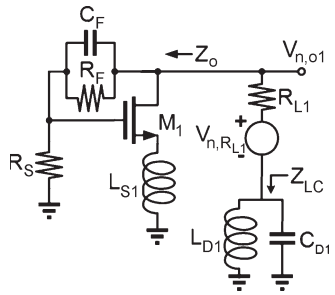

Fig. 5. Equivalent circuit for suppressing the thermal noise of R_{L1}.

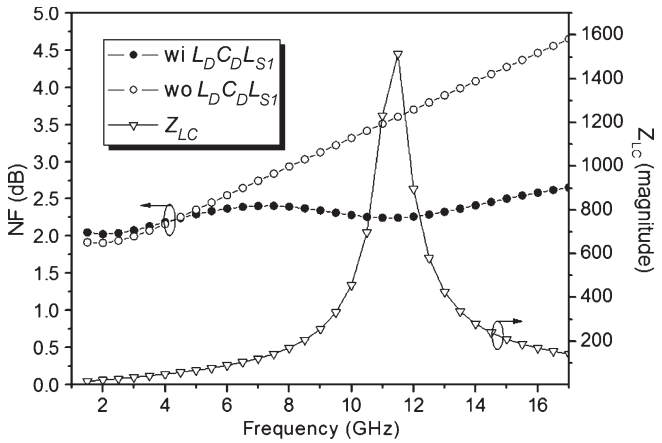

Fig. 6. Simulation effect of L_D, C_D, and L_{S1} on the NF of the input stage.

NF. As depicted in Fig. 5, we assume that the impedance seen looking into the drain of M_1 is equal to Z_o, the impedance of parallel-LC circuit is Z_{LC}, and the output noise power contributed by R_{L1} can be derived as

$$V_{n,o1}^2 = 4kTR_{L1} \times \frac{Z_o^2}{(Z_o + R_{L1} + Z_{LC})^2}. \tag{8}$$

From (8), $V_{n,o1}$ is inversely proportional to Z_{LC}, so the output noise voltage can be effectively reduced at resonance. As shown in Fig. 6, L_{D1}, C_{D1}, and L_{S1} can reduce high-frequency noise (7–15 GHz) effectively.

B. Second Stage

The second stage is a cascode common-source stage, which provides high-frequency gain and better isolation. The transistor M_3 is used for the improvement of M_2's Miller effect, better isolation, and higher gain. The series peaking inductor L_{D2} can resonate with the total parasitic capacitances C_{D3} at the drain of M_3, and a resistor R_{L2} is added to reduce the Q factor of L_{D2} for flat gain. As shown in Fig. 1, we use a voltage divider that consists of resistors R_{B1} and R_{B2} to realize the forward body bias (FBB) technique for reducing the threshold voltage of the transistor [10]. A general FBB needs an extra dc bias. In other words, we can save an extra dc pad by using a voltage divider, so the complexity of the layout is lessened, and the FBB can further obtain the same g_{m2} with a low supply voltage so that the power consumption can be reduced. Fig. 7 shows the

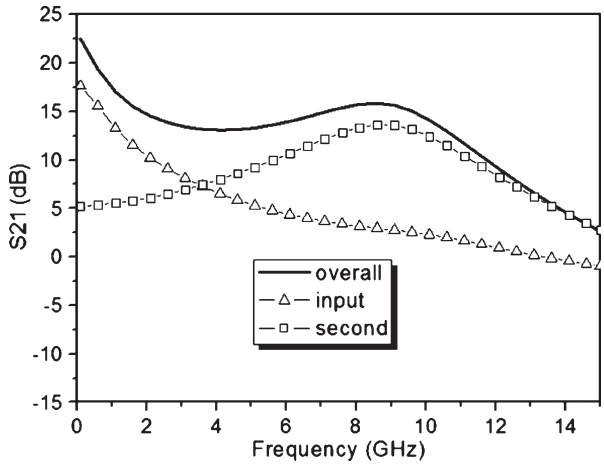

Fig. 7. Simulation frequency response of the input stage, the second stage, and the overall stage.

simulation frequency response of the input stage, the second stage, and the overall stage. The input stage and the second stage provide low-frequency power gain and high-frequency power gain, respectively. The combination of both frequency responses results a broadband power gain. The parameters of the UWB LNA design are listed in Table I.

III. Experimental Results

The proposed UWB LNA has been fabricated by the Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-μm CMOS process. The chip microphotograph is shown in Fig. 8. The chip area is 0.697 $\times$ 0.657 mm, including testing pads. The measurement is carried out on a wafer for RF characterization.

Fig. 9 shows the power gain and the input return loss of the UWB LNA. The measured power gain is 12.4 dB ($\pm$ 1.5-dB variation) from 3.1 to 10.6 GHz. The measured high-frequency gain is less than the simulated one by about 1.4 dB. It may be due to process variation and inaccuracy of inductor and transistor models. The measured input return loss is -9.4 to -32.5 dB from 3.1 to 15 GHz. Fig. 10 shows the output return loss and the reverse isolation of the UWB LNA. The measured output return loss is below -8.5 dB, and the measured reverse isolation is below -45 dB across the entire band.

The measured and simulated NFs are illustrated in Fig. 11. The measured NF is 2.5–4.7 dB from 3.1 to 10.6 GHz. The measured NF is larger than the computed one due to degraded power gain. The measured and simulated group delays are illustrated in Fig. 12. The average delay is 75 ps with maximum and minimum values of 125 and 25 ps, respectively. Fig. 13 shows IIP3 measured by applying a two-tone test with 1-MHz spacing. The measured IIP3 is -8.5 dBm at 8 GHz. Fig. 14 shows the measured IIP3 versus frequency. The measured IIP3 is higher than -8.5 dBm from 4 to 10 GHz. In general, the figure of merit (FoM) is applied to evaluate performance of LNAs and is defined as [11]

$$\text{FoM } (\text{mW}^{-1}) = \frac{S_{21}[1] \times BW \text{ (GHz)}}{(NF-1)[1] \times P_{\text{dc}} \text{ (mW)} \times f_t \text{ (GHz)}}.$$

TABLE I
CIRCUIT PARAMETERS OF THE UWB LNA

Devices	M_1* (μm)	M_2* (μm)	M_3* (μm)	M_4* (μm)	R_F (kΩ)	C_F (fF)	L_{S1} (pH)	R_{L1} (Ω)	C_{D1} (fF)	L_{D1} (nH)	R_{B1} (kΩ)	R_{B2} (kΩ)	R_{L2} (Ω)	L_{D2} (nH)
Design values	383	160	160	96	3	43	416	163	70	1.67	8	4.85	36	1.04

* The length of transistors are 0.18μm.

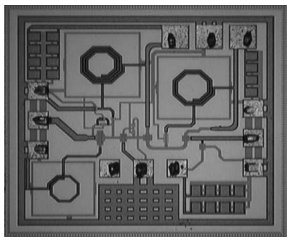

Fig. 8. Chip microphotograph of the UWB LNA.

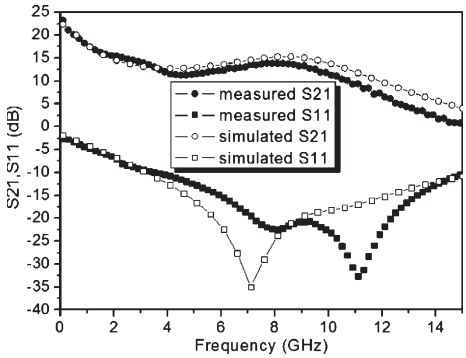

Fig. 9. Power gain and input return loss of the UWB LNA.

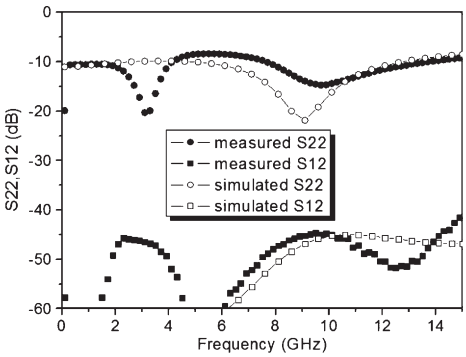

Fig. 10. Output return loss and reverse isolation of the UWB LNA.

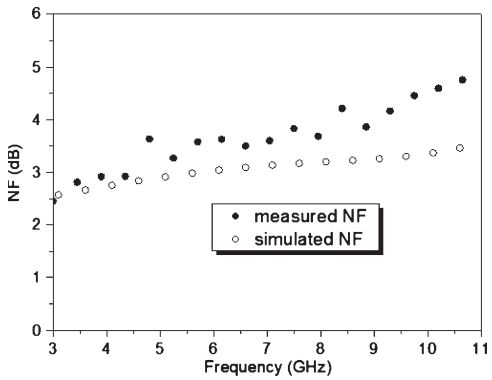

Fig. 11. Measured and simulated noise figures of the UWB LNA.

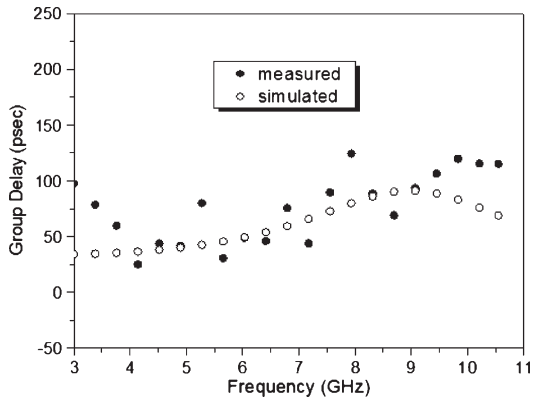

Fig. 12. Measured and simulated group delay of the UWB LNA.

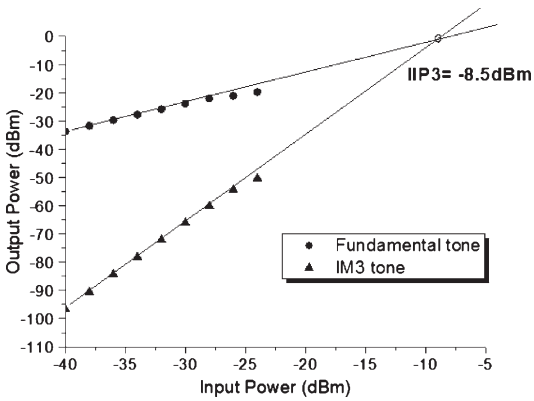

Fig. 13. Measured IIP3 at 8 GHz.

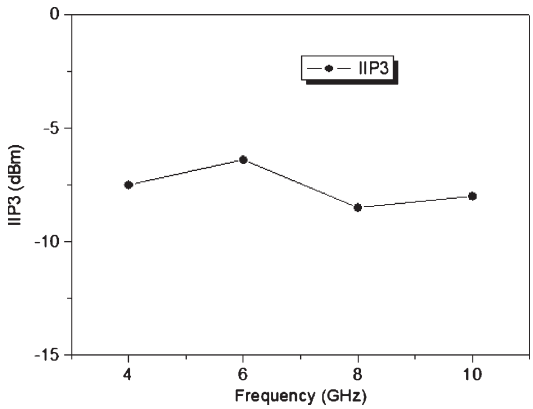

Fig. 14. Measured IIP3 versus frequency.

The measured performance of the proposed LNA is compared with others, which is summarized in Table II. It is found that our circuit achieves an excellent noise figure and the best ratio of FoM to chip area.

TABLE II
MEASURED PERFORMANCE SUMMARY AND COMPARISON

Ref.	CMOS Technology	3-dB BW (GHz)	G_{max} (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Area (mm^2)	FoM (W^{-1})	FoM/Area (W^{-1}/mm^2)
This work	0.18μm	3.1-10.6	13.9	2.5-4.7	-8.5	14.4	0.46	57.1	124.1
[1]	0.18μm	1.2-11.9	9.7	4.5-5.1	-6.2	20	0.59	15.5	26.2
[2]	0.18μm	0.4-10	12.4	4.4-6.5	-6	12	0.42	32.8	78.1
[4]STD	0.18μm	2.3-9.2	9.3	4-8	-6.7	9	1.1	25.5	23.1
[5]$^{\Delta}$	0.18μm	3.1-10.6	17.5	3.1-5.7	-	33.2^{+}	0.5	28.2	56.4
[6]	0.18μm	2.8-7.2	19.1	3-3.8	-1	32^{+}	1.63	21.5	13.2
[7]	0.18μm	0.04-7	8.6	4.2-6.2	$+3$	9	1.16	22.1	19.1
[8]	0.18μm	2.9-11	16	3.8-4.8	-	9.5	0.98	66.3	67.66
[9]	0.13μm	3.1-10.6	16.5	2.07-2.93	-8.5	9	0.87	101.3	121.6

$^{\Delta}$ Simulation only.
$^{+}$ The power consumption including buffer, ours is 21mW.

IV. CONCLUSION

A UWB LNA has been proposed and implemented by the TSMC 0.18-μm CMOS technology. By using the proposed input stage, the local feedback noise can be reduced to achieve a very low NF and broadband input matching. The measured NF is 2.5–4.7 dB, and the power gain is 10.9–13.9 dB from 3.1 to 10.6 GHz. The measured input return loss is below -9.4 dB from 3.1 to 15 GHz. The IIP3 is -8.5 dBm at 8 GHz. It consumes 14.4 mW from a 1.4-V supply and occupies a chip area of only 0.46 mm^2. The proposed UWB LNA compared with other UWB techniques has excellent noise performance, a small size, and a higher FoM.

ACKNOWLEDGMENT

The authors would like to thank the National Chip Implementation Center, Taiwan, for chip fabrication and measurement support.

REFERENCES

[1] C. F. Liao and S. I. Liu, "A broadband noise-canceling CMOS LNA for 3.1–10.6-GHz UWB receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 329–339, Feb. 2007.

[2] K. H. Chen, J. H. Lu, B. J. Chen, and S. I. Liu, "An ultra-wide-band 0.4-10-GHz LNA in 0.18- μm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 3, pp. 217–221, Mar. 2007.

[3] C. W. Kim, M. S. Kang, P. T. Anh, H. T. Kim, and S. G. Lee, "An ultra-wideband CMOS low noise amplifier for 3–5-GHz UWB system," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 544–547, Feb. 2005.

[4] A. Bevilacqua and A. M. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1–10.6-GHz wireless receivers," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2259–2267, Dec. 2004.

[5] Y. Lu, K. S. Yeo, A. Cabuk, J. G. Ma, M. A. Do, and Z. H. Lu, "A novel CMOS low-noise amplifier design for 3.1-to 10.6-GHz ultra-wide-band wireless receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 8, pp. 1683–1692, Aug. 2006.

[6] Y. J. E. Chen and Y. I. Huang, "Development of integrated broad-band CMOS low-noise amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 10, pp. 2120–2127, Oct. 2007.

[7] F. Zhang and P. Kinget, "Low power programmable-gain CMOS distributed LNA," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1333–1343, Jun. 2006.

[8] Y. Shim, C. W. Kim, J. Lee, and S. G. Lee, "Design of full band UWB common-gate LNA," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 10, pp. 721–723, Oct. 2007.

[9] M. T. Reiha and J. R. Long, "A 1.2 V reactive-feedback 3.1–0.6 GHz low-noise amplifier in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1023–1033, May 2007.

[10] H. H. Hsieh and L. H. Lu, "A high-performance CMOS voltage-controlled oscillator for ultra-low-voltage operations," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 3, pp. 467–473, Mar. 2007.

[11] D. Barras, F. Ellinger, H. Jackel, and W. Hirt, "A low supply voltage SiGe LNA for ultra-wideband frontends," *IEEE Microw. Wireless Compon. Lett.*, vol. 14, no. 10, pp. 69–71, Oct. 2004.