Characteristics of SONOS-Type Flash Memory With *In Situ* Embedded Silicon Nanocrystals

Tsung-Yu Chiang, Yi-Hong Wu, William Cheng-Yu Ma, Po-Yi Kuo, Kuan-Ti Wang, Chia-Chun Liao, Chi-Ruei Yeh, Wen-Luh Yang, and Tien-Sheng Chao, *Senior Member, IEEE*

***Abstract*—In this paper, silicon–oxide–nitride–oxide–semiconductor (SONOS) devices with embedded silicon nanocrystals (Si-NCs) in silicon nitride using *in situ* method with multilevel and 2-b/cell operation have been successfully demonstrated. The proposed *in situ* Si-NC deposition method exhibits the advantages of low cost, simplicity, and compatibility with modern IC processes. SONOS memories with embedded Si-NCs exhibit a significantly improved performance with a large memory window ($>$ 5.5 V), low operating voltage (P/E voltage: $V_g = 6$ V, $V_d = 7$ V and $V_g = -7$ V, $V_d = 10$ V, respectively), greater tolerable gate and drain disturbance (V_t shift $<$ 0.2 V), negligible second-bit effect, high P/E speed (after programming time $= 10$ μs with a 2-V shift of V_t under $V_g = V_d = 6$ V operation), good retention time ($> 10^8$ s for 13% charge loss), and excellent endurance performance (after 10^4 P/E cycles with a memory window of 3 V).**

***Index Terms*—*In situ*, memory window, nonvolatile memory, retention time, silicon nanocrystal (Si-NC).**

I. Introduction

THE SCALING down of conventional floating-gate memory devices has met limitations beyond 60-nm node technology [1]. Tunneling oxide thickness below 7 nm must confront a number of challenges, including large stress-induced leakage current (SILC), serious short-channel effect, and critical floating-gate coupling effect [2]–[4]. The most serious issue among these challenges is the increase of the tunneling oxide leakage current induced by program/erase cycling stress, resulting in data retention degradation when the tunneling oxide is scaled below 7 nm [3].

Recently, metal–oxide–semiconductor (MOS) memory devices with embedded silicon nanocrystals (Si-NCs) and polysilicon–oxide–nitride–oxide–semiconductor (SONOS) nonvolatile memory devices have attracted attention because of their potential for solving the issues involved in scaling down conventional floating-gate memory devices [5]–[8]. In MOS memories with embedded Si-NCs and SONOS memories, charge stored in the trapping layer offers advantages over floating-gate memories, including high density, elimination of drain-induced turn-on effect, 2-b operation, no floating-gate coupling effect, and excellent immunity to SILC [9]–[12]. When the tunneling oxide thickness is scaled down below 7 nm, SONOS memories show much better retention than floating-gate memories. This is attributed to the discrete and deep-level storage states of SONOS memory devices.

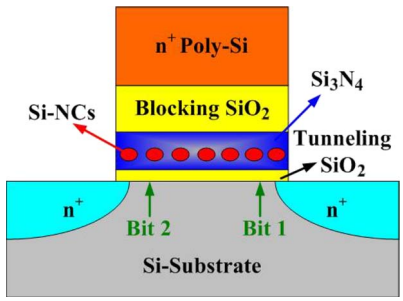

Fig. 1. Schematic representation of a Flash memory cell structure with the nitride film embedded Si-NCs using the *in situ* method.

However, SONOS memories still face many issues, including lateral stored charge migration, the second-bit effect, and erase saturation [13]–[16]. Therefore, a MOS memory device with embedded Si-NCs has been proposed to solve lateral stored charge migration and second-bit effect [17], [18]. Unfortunately, it is difficult to grow high-density suitably distributed uniformly sized Si-NCs on silicon oxide. It has been reported that the density of Si-NCs on silicon nitride is higher than on oxide [19], [20], because silicon nitride exhibits lower activation energy and higher nucleation growth rate than oxides. This means that nucleation occurs more easily on silicon nitride surfaces than on silicon oxide surfaces.

The performance of SONOS can be improved further if embedded Si-NCs are used. The Si-NCs can be formed in Si-rich SiN_x layers using different chemical vapor deposition (CVD) techniques or by a low-energy Si ion implantation technique [21], [22]. Finding a simple scheme to produce embedded Si-NCs in silicon nitride has thus become increasingly important for the development of SONOS-type memories.

Recently, we have investigated SONOS-type memory devices with *ex situ* embedded Si-NCs in nitride, showing improved performance in terms of larger memory window, lower operation voltage, and longer retention time [23]. However, this growth method of Si-NCs is not an *in situ* method. Later, we successfully developed an *in situ* method to fabricate SONOS devices with embedded Si-NCs in silicon nitride [24]. In this

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T.-Y. Chiang, Y.-H. Wu, P.-Y. Kuo, K.-T. Wang, C.-C. Liao, C.-R. Yeh, and T.-S. Chao are with the Department of Electrophysics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: tschao@mail.nctu.edu.tw).

W. C.-Y. Ma is with the Institute of Electronics, National Chiao Tung University, Hsinchu 30010, Taiwan.

W.-L. Yang is with the Department of Electronic Engineering, Feng Chia University, Taichung 40724, Taiwan.

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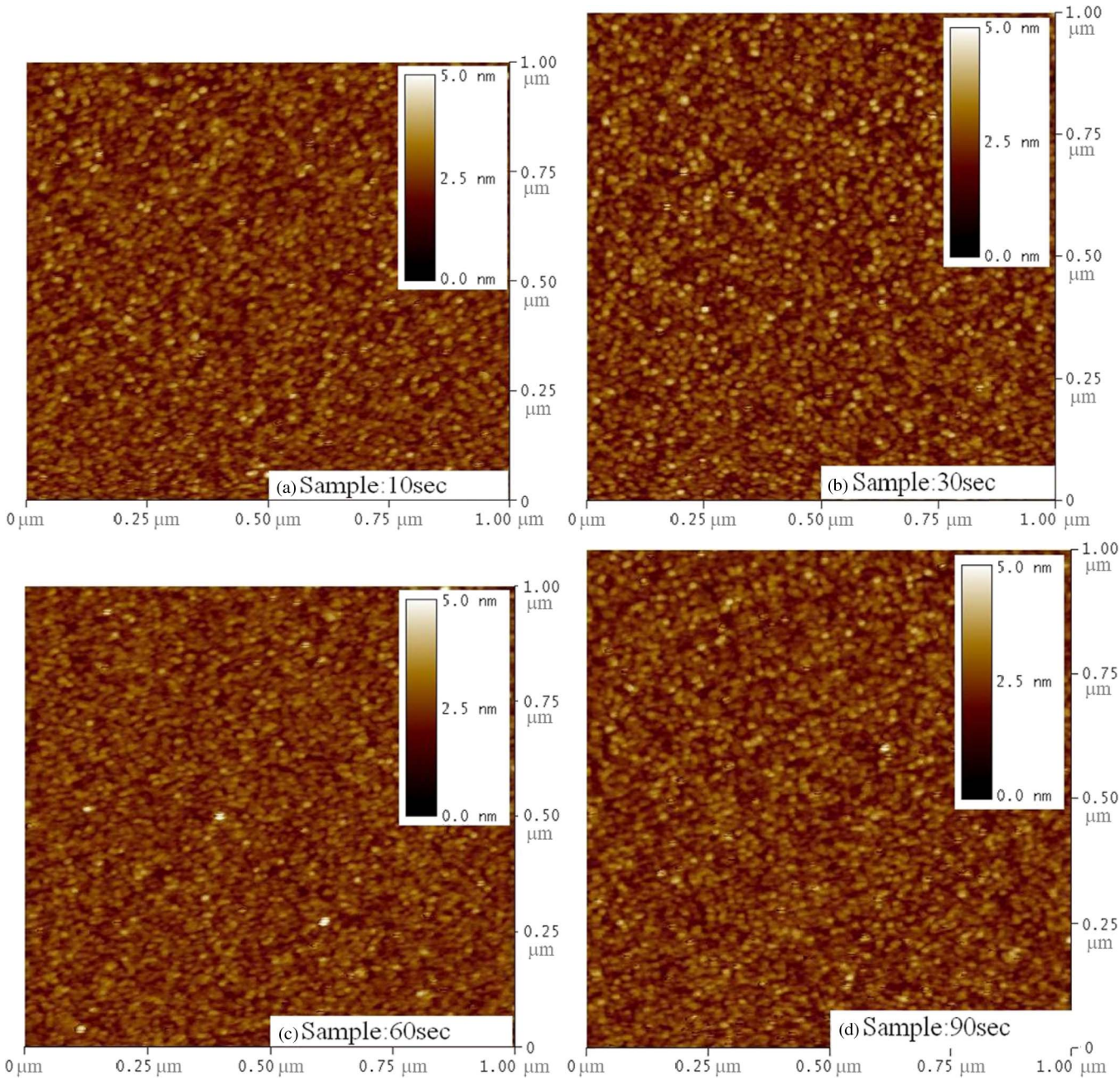

Fig. 2. $1 \times 1\ \mu m^2$ AFM image of Si-NCs formed on the nitride film with the four deposition conditions. The highest density of the Si-NC is $9 \times 10^{11}\ cm^{-2}$.

paper, a SONOS-type Flash memory with *in situ* embedded Si-NCs in silicon nitride is fully investigated in detail, including dot size and density analyzed by AFM and transmission electron microscopy (TEM). The performance and reliability of devices formed with different Si-NC deposition times (10, 30, 60, and 90 s), including data retention, multilevel and 2-b operation, P/E cycling test, and drain and gate disturbance, were investigated.

II. Experimental Procedure

Fig. 1 shows the schematic diagram of the *in situ* embedded Si-NCs in a silicon nitride film. Devices were fabricated on p-type (100) 150-mm 8–12-$\Omega \cdot$ cm silicon substrates. After the LOCOS isolation process, a 2.5-nm-thick tunneling oxide was thermally grown in N_2O on the silicon substrate. The formation of *in situ* embedded Si-NCs in the silicon nitride film includes three steps, including bottom nitride, Si-NCs, and top nitride. In the first step, i.e., the forming of the bottom silicon nitride, a 3-nm-thick silicon nitride film was deposited in a low-pressure CVD system using NH_3 (130 sccm) and $SiCl_2H_2$ (30 sccm) at 780 °C. The second step was the *in situ* forming of the Si-NCs. It is noted that wafers were still in the same tube at the same temperature. The only change in the recipe was turning off the NH_3 gas and reducing the flow rate of the $SiCl_2H_2$ to 10 sccm. In this step, the Si-NCs were then *in situ* deposited on the wafers. The deposition times used were 10, 30, 60, and 90 s, respectively. As previously mentioned, the density of

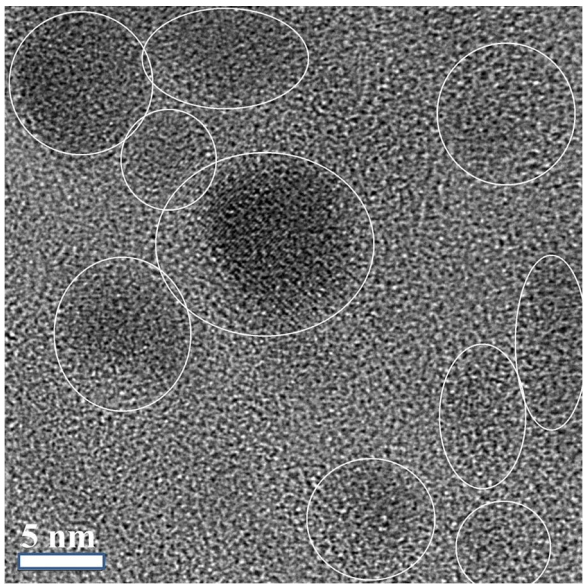

Fig. 3. Top view of an HR-TEM image of 30-s deposition time embedded the nitride film with *in situ* Si-NC.

Si-NCs deposited on the nitride is higher than that on oxide. Hence, this method enjoys the advantage of high density of Si-NCs. The final step in the process is the formation of the top nitride, with a thickness of 4 nm, on the Si-NCs deposited in the same tube by turning on the NH_3 gas again.

Using this approach, the wafers do not need to change tubes during the process of embedding the Si-NCs in the silicon nitride layer. These Si-NCs can be easily *in situ* embedded into the silicon nitride without additional instruments or treatments. All three steps were executed in the same tube and at the same temperature by the alternating on/off switching of NH_3 gas. A blocking oxide (20 nm) was deposited on the nitride using a high-density plasma CVD system. An n^+-poly-Si (200 nm) was deposited as the control gate. Subsequently, gate patterning, source/drain implantation, contact patterning, and the remaining standard CMOS processes were completed to fabricate the SONOS-type memory with *in situ* embedded Si-NCs in the silicon nitride layer.

III. Results and Discussion

Fig. 2 shows the 1×1 μm^2 AFM images of Si-NCs formed on the nitride film with the four deposition conditions. The highest density of the Si-NC is 9×10^{11} cm^{-2}. The root-mean-square roughness values of the SONOS with Si-NC deposition for 10, 30, 60, and 90 s are 0.499, 0.548, 0.453, and 0.517 nm, respectively. These Si-NCs are well separated, with an average 2-D distance > 5 nm on the silicon nitride, which ensures electrical isolation between any two Si-NCs. Fig. 3 shows the top view of a high-resolution TEM (HR-TEM) image for Si-NCs. The mean size of Si-NCs and the aerial density turned out to be 7–12 nm and $7-9 \times 10^{11}$ cm^{-2}, respectively. The trends of the size and the density of Si-NCs across various deposition times are shown in Fig. 4. A longer deposition time results in a larger Si-NC size. However, the longest deposition time (90 s) of Si-NCs does not show the highest density.

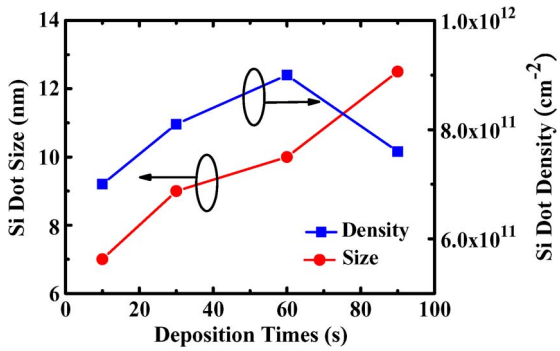

Fig. 4. Si-NC size and density depend on the deposition time.

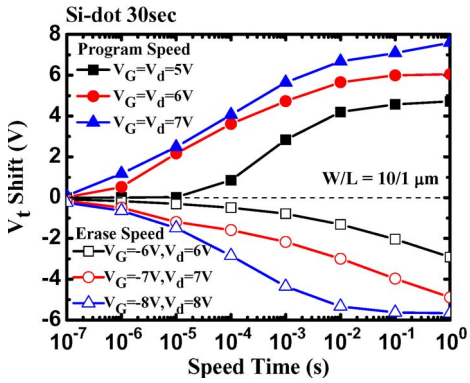

Fig. 5. Program and erase speed characteristics for 30-s deposition time at different operating voltages.

Instead, the 60-s deposition time shows the highest density among these samples. This may be attributed to the merging of NCs during a longer deposition time. After comprehensive material and morphological analysis of the Si-NCs, a series of electrical characterizations was then carried out to discover the optimum conditions for programming and erasing SONOS with *in situ* embedded Si-NCs.

Fig. 5 shows the programming speed of a SONOS-type memory with *in situ* Si-NCs for a deposition time of 30 s under different operating bias conditions. The memory window is defined as the change of the V_t of the sample between the programmed and erased states. The threshold voltage (V_t) is defined as the applied gate voltage when the drain current is 100 nA during operation mode. The device is programmed by using channel hot-electron injection and erased by using band-to-band hot-hole injection. When V_d and V_g were both set at 6 V, a considerably high programming speed $(t = 10\ \mu s)$ with a 2-V shift of V_t was found. A higher voltage of V_d and V_g tends to result in faster programming speed and larger programming window. It should be noted that the saturation phenomenon of programming window did not occur when the voltage bias was set at $V_g = V_d = 7$ V. Fig. 6 shows the curves of programming $(V_g = V_d = 6\ \text{V})$ and erasing speed $(V_g = -8\ \text{V}, V_d = 8\ \text{V})$ across the different deposition times of Si-NCs. A deposition time of 30 s results in faster programming and erasing speeds than the other times due to the maximum trapping cross area, a product of dot size and dot density. This implies that higher dot size and density will increase the number of trapping states, which can be located in Si-NCs or at the interface of the

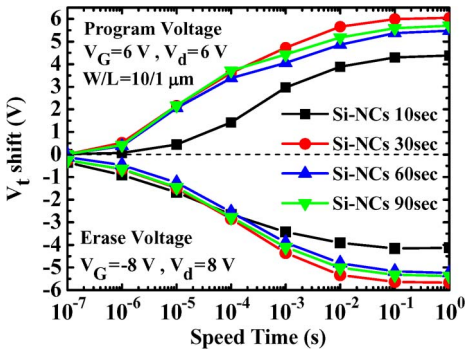

Fig. 6. Program and erase speed curves of the same operating voltage across different Si-NC deposition times.

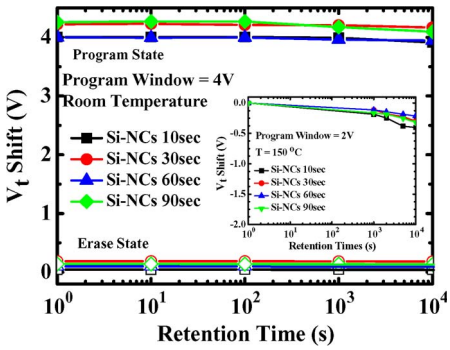

Fig. 7. Data retention characteristics of a Si-NC Flash memory device across different deposition times at a programming window of 4 V at room temperature (inset shows a programming window of 2 V at 150 °C).

silicon nitride and the Si-NCs. Among all devices, those with a deposition time of 10 s show the minimum memory window having the smallest and lowest density Si-NCs. This implies that a 10-s deposition time is not enough for the formation of higher density Si-NCs.

Fig. 7 shows the data retention performance measured at room temperature. The charge loss can barely be observed up to 10^4 s. At room temperature, the charge loss was below 13%, as extrapolated to 10^8 s. The retention characteristics of devices baked at 150 °C are measured and shown in the inset of Fig. 7. They exhibit only a 10% charge loss for 10^4 s. Compared to conventional SONOS, SONOS memories with embedded Si-NCs appear to have better data retention due to the additional trapping sites created at the Si-NCs or at the interface of the Si-NCs and the nitride. Fig. 8 shows the data retention behavior of the SONOS memory devices with embedded Si-NCs and multilevel operation at room temperature and high temperature (at 85 °C). There is negligible charge loss for multilevel operation for SONOS memory devices with embedded Si-NCs.

The band-to-band tunneling is the main cause of drain disturbance, resulting in charge injection into the trapping nitride layer [25], [26]. The electrons can be migrated by vertical hopping in the silicon nitride layer. The electrons can move to the bottom silicon nitride from the top silicon nitride to increase the total quantity of trapped electrons, resulting in a larger memory window. The result means that the deposition time of 30 s has a lot of effective trapped states. Therefore, the deposition time of 30 s has a larger gate and drain disturbance. However, the drain disturbance and gate disturbance of SONOS

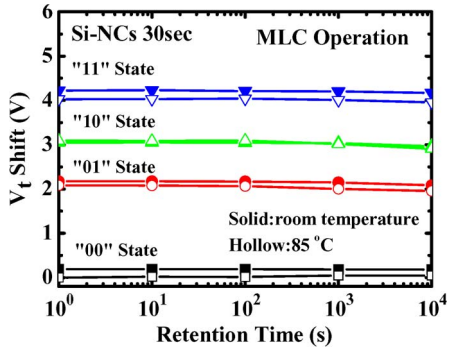

Fig. 8. Multilevel operation data retention of Si-NC memories for the deposition time of 30 s at room temperature and high temperature (at 85 °C).

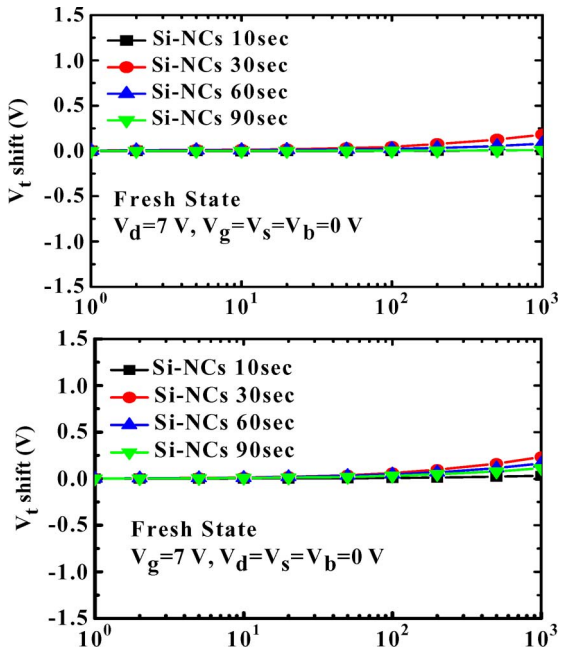

Fig. 9. Drain disturbance and gate disturbance characteristics of various Si-NC embedded nitride layer memory samples.

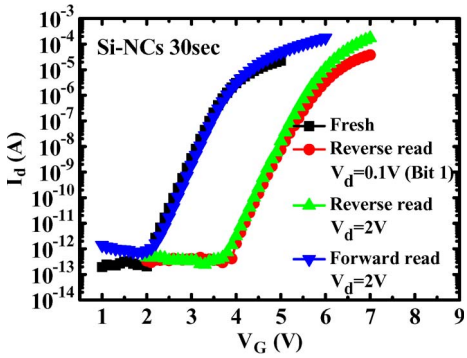

Fig. 10. I_d–V_g curves of the 2-b Si-NC embedded nitride film memory in one cell; forward read and reverse read for programmed bit 1.

memories with embedded Si-NCs for different deposition times are not affected at all, as shown in Fig. 9. The V_t shifts of the drain disturbance and gate disturbance were less than 0.2 V for devices with different deposition times after 10^3 s under stress. As a result, the drain disturbance and gate disturbance can be ignored for devices with embedded Si-NCs.

TABLE I
OPERATING PRINCIPLES AND BIAS CONDITIONS USED DURING THE OPERATION OF THE SONOS MEMORY WITH EMBEDDED Si-NCs

		Program (V)	Erase (V)	Read (V)
Bit-1	V_G	6	-7	4.5
	V_D	7	10	0
	V_S	0	0	>2

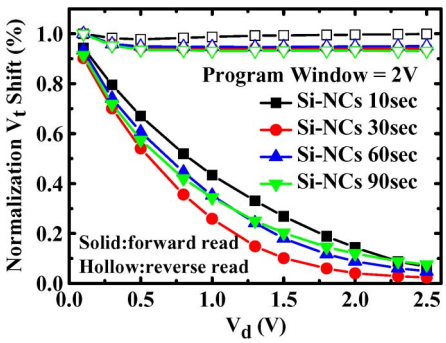

Fig. 11. Two-bit effect characteristics of various Flash memory samples using *in situ* Si-NCs.

Fig. 10 shows the feasibility of performing a 2-b operation for the SONOS memory with embedded Si-NCs for a deposition time of 30 s through a forward read and reverse read scheme in a single cell. The read operation was achieved using a reverse read scheme. From the I_d–V_g curves, it is evident that the forward and reverse reads can be employed to detect the information stored in programmed bit 1 (drain side). The memory window difference between the forward and reverse V_t's was found to be 2 V, indicating that 2-b operation in a single cell is possible. Table I summarizes the operation bias conditions for the 2-b operation of SONOS memory with embedded Si-NCs. Forward read and reverse read after programming at the drain-side storage result in a memory window of 2 V, as shown in Fig. 11. A well-behaved 2-b operation was found for the SONOS with a 30-s deposition time, most likely because a deposition time of 30 s generates the optimum size and aerial density of Si-NCs. These results confirmed again that MOS memory devices with embedded Si-NCs can solve the lateral stored charge migration and second-bit effect [17], [18] in long-channel devices, but this improvement on charge migration needs more investigations in short-channel devices. Fig. 12 shows the endurance characteristics of the SONOS memories with embedded Si-NCs. The programming and erasing conditions were $V_g = 6$ V and $V_d = 7$ V for 30 μs and $V_g = -7$ V and $V_d = 10$ V for 20 ms, respectively. A large memory window, i.e., 3 V, was obtained for a deposition time of 30 s after 10^4 P/E cycles. The deposition time of 10 s is not shown in Fig. 12 because the V_t cannot shift under this operation voltage. The upward V_t shift is due to interface trap generation and electron trapping in the tunneling oxide during P/E cycle operation [27], [28]. After 10^4 P/E cycles, the charge loss curves of the SONOS memories with embedded Si-NCs are measured at room temperature and are shown in Fig. 13. A large memory window of 2.7 V and a small charge loss

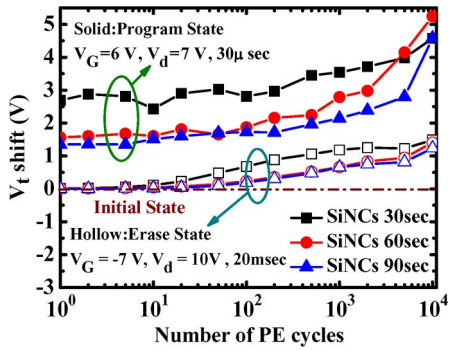

Fig. 12. Endurance characteristics of Si-NC embedded nitride layer memories across different samples up to 10^4 P/E cycles.

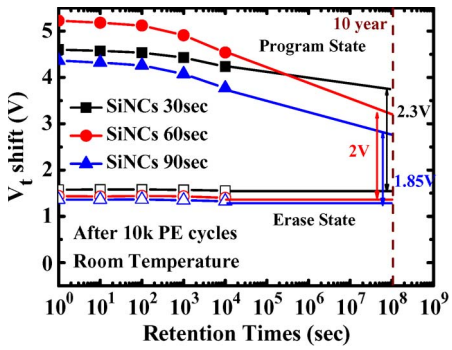

Fig. 13. Data retention after 10^4 P/E cycles in different samples of embedded Si-NCs in nitride layer memories.

of 12% are found as the time of stress is increased to 10^4 s at room temperature. The memory window was still 2.3 V, as extrapolated to 10^8 s. Before P/E cycles, the I_{cp} currents of the device with embedded Si-NC deposition for 30, 60, and 90 s are 7.43×10^{-9}, 7.59×10^{-9}, and 1.1×10^{-9} nA, respectively. After 10^4 P/E cycles, the I_{cp} currents of the device with embedded Si-NC deposition for 30, 60, and 90 s are 1.2×10^{-8}, 1.26×10^{-8}, and 1.59×10^{-8}, respectively. The device with a deposition time of 30 s has the lower I_{cp} current, which means lower interface state after 10^4 P/E cycles. This result means that the deposition time of 30 s has lower charge loss due to better interface states. The charge loss appears to result from detrapping from shallow traps at the interface or/and electron traps in the tunneling oxide. Some memory devices with high-k material such as Si-NCs, Si_3N_4, La_2O_3, CeO_2, and Y_2O_3 [29]–[33] are compared in Table II. Among these devices, SONOS memories with embedded Si-NCs exhibit large memory windows at a lower operating voltage.

SONOS memories also have a higher program/erase speed and excellent data retention at high temperatures and after P/E cycles compared to the devices with high-k materials. This is due to the newly created trapping sites in the Si-NCs or at the interface of the silicon nitride and the Si-NCs.

IV. CONCLUSION

SONOS-type Flash memory devices with *in situ* embedded Si-NCs in nitride have been successfully demonstrated. Multilevel and 2-b/cell operations of this device are easily obtained with a fast program/erase speed. It is found that the optimum

TABLE II
COMPARISON OF MEMORY DEVICE ELECTRICAL CHARACTERISTICS AMONG EMBEDDED Si-NCs IN NITRIDE LAYER MEMORY DEVICES (THIS WORK) AND OTHER SONOS-TYPE MEMORY DEVICES WITH DIFFERENT HIGH-k TRAPPING LAYERS

	Memory window	P/E voltage (V) and times(s) ΔV_t=2V	Charge loss after 10^4 sec @150°C	After PE cycles @ Charge loss after 10^4 sec
This work	**6V**	**V_G=V_d=6V , 10μsec V_G=-8V, V_d=8V , 100μsec**	**10%**	**12%**
SiO_2/Si /SiO_2 [29]	1.4V	V_G=13V,V_d=13V , 1μsec @only ΔV_t=1.4V	14% Only 25°C	No data
SiO_2/Si_3N_4 /SiO_2 [30]	4.2V	V_G=8V,V_d=8V , 100μsec V_G=-5V, V_d=8V , 10μsec	26% Only 25°C	40%
SiO_2/La_2O_3 /SiO_2 [31]	3.5V	V_G=V_d=8V , 1msec V_G=-4V, V_d=9V , 1msec	20% Only 125°C	No data
SiO_2/CeO_2 /SiO_2 [32]	6V	V_G=9V , V_d=10V , 10μsec V_G=-5V, V_d=10V , 10μsec	24% Only 85°C	No data
SiO_2/Y_2O_3 /SiO_2 [33]	4.3V	V_G=6V,V_d=8V , 1msec V_G=-3V, V_d=8V , 100μsec	No data	12%

time of deposition of Si-NCs is 30 s based on the program/erase speed and endurance performance. This device has been shown to have excellent electrical performance in terms of larger memory windows, fast program/erase speed, ignored second-bit effect, almost negligible drain and gate disturbance, long data retention times, and good endurance up to 10^4 cycles with a memory window of 3 V. This *in situ* scheme to incorporate Si-NCs in nitride appears to be very promising for SONOS Flash memory applications.

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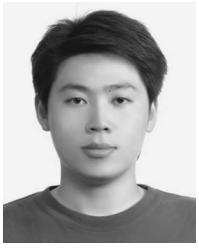
Tsung-Yu Chiang was born in Yunlin, Taiwan, in 1984. He received the B.S. degree in physics from National Chung Cheng University, Chiayi, Taiwan, in 2006. He is currently working toward the Ph.D. degree in the Department of Electrophysics, National Chiao Tung University, Hsinchu, Taiwan.

His research interest includes the studies of semiconductor device physics, including low-temperature polycrystalline-silicon thin-film transistors, metal-gate/high-k technology, strain techniques, and nonvolatile Flash memories.



Yi-Hong Wu was born in Chiayi, Taiwan, in 1984. He received the B.S. and M.S. degrees in electronics engineering from Feng Chia University, Taichung, Taiwan, in 2006 and 2008, respectively. He is currently working toward the Ph.D. degree in the Department of Electrophysics, National Chiao Tung University, Hsinchu, Taiwan.

His research interest includes the studies of semiconductor device physics, including low-temperature polycrystalline-silicon thin-film transistors and nonvolatile Flash memories.

William Cheng-Yu Ma was born in Taipei, Taiwan, in 1980. He received the B.S. degree in electrophysics and the M.S. and Ph.D. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2002, 2004, and 2008, respectively.

He is currently with the Institute of Electronics, National Chiao Tung University, working for the research and design of 32-nm node CMOS technology. His research interests are in the fabrication and characterization of low-temperature polycrystalline-silicon thin-film transistors, silicon-on-insulator devices, metal-gate/high-k technology, and RF metal–insulator–metal capacitors.

Po-Yi Kuo was born in Pingtung, Taiwan, in 1978. He received the Ph.D. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2007.

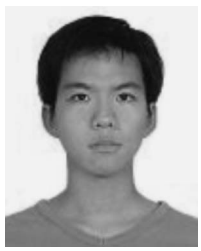
Since October 2008, he has been with the Department of Electrophysics, National Chiao Tung University, as a Postdoctoral Researcher. His current research topics are gate-all-around nanowire transistors, vertical channel thin-film transistors, Si/Ge heterojunction devices, floating-body-effect random-access memories, and tunneling field-effect thin-film transistors.

Kuan-Ti Wang was born in Kaohsiung, Taiwan, in 1983. He received the B.S. degree in electronics engineering from Chang Gung University, Taoyuan, Taiwan, in 2006. He is currently working toward the Ph.D. degree in the Department of Electrophysics, National Chiao Tung University, Hsinchu, Taiwan.

His research interests include dynamic threshold MOSFETs, metal-gate/high-k technology, and nonvolatile Flash memories.

Chia-Chun Liao was born in Taoyuan, Taiwan, in 1980. He received the B.S. degree in electrophysics from National Chiao Tung University, Hsinchu, Taiwan, in 2007, where he is currently working toward the Ph.D. degree in the Department of Electrophysics.

His research interests include strain techniques, PEALD for metal-gate/high-k applications, and nonvolatile Flash memories.



Chi-Ruei Yeh was born in Taipei, Taiwan, in 1985. He received the M.S. degree in electrophysics from National Chiao Tung University, Hsinchu, Taiwan, in 2009.

He is currently with the Department of Electrophysics, National Chiao Tung University. His research interests include low-temperature polycrystalline-silicon thin-film transistors and metal-gate/high-k technology.

Wen-Luh Yang was born in Taichung, Taiwan, on May 5, 1961. He received the B.S. degree and the M.S. and Ph.D. degrees in electronics from National Chiao Tung University, Hsinchu, Taiwan, in 1983, 1987, and 1992, respectively.

In 1993, he joined the faculty of Feng Chia University, Taichung, as an Associate Professor with the Department of Electrical Engineering. From 2000 to 2004, he was a Professor and the Chairman of the Department of Electronic Engineering. From 2004 to 2006, he was the Associate Dean of the College of Information and Electrical Engineering, the Chairman of the Honor Program of Information and Electrical Engineering, the Director of the Master Program of the Extended Education, and the Chief Executive Officer of the Master Program of Industrial R&D. He is currently a Professor with the Department of Electronic Engineering. He is an Independent Director of the Solid State System Company, Ltd. (Flash Disk Innovators), and is an Advisory Counselor of the Anova Technology Company, Ltd. He is interested in Flash (SONOS), metal silicides, Cu and low-k-dielectric multilevel interconnections, and bio-electronics.

Tien-Sheng Chao (SM'01) was born in Penghu, Taiwan, in 1963. He received the Ph.D. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1992.

In July 1992, he joined the National Nano Device Laboratories (NDL) as an Associate Researcher, where he became a Researcher in 1996. He was engaged in developing thin dielectric preparations, cleaning processes, and CMOS device fabrication. In 2001, he joined the Department of Electrophysics, National Chiao Tung University, where he has been a Professor since 2002. He acted as the Vice Director of NDL from January 2002 to July 2004. He has published more than 160 papers in his field.