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Effect of Nitrogen Plasma Treatment on Electrical Characteristics for Pd Nanocrystals in Nonvolatile Memory

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Pd nanocrystals (NCs) are successfully embedded in a TaN/SiO_2/HfAlO/Si structure. The initial memory window increases at a higher rate with increasing fabrication temperature of Pd NCs compared with the linear variation of Pd NC density, which is related to the thermally induced neutral traps in the HfAlO film around Pd NCs. After manufacturing a TaN/SiO_2/Pd NCs/HfAlO/Si/Al structure, the subsequent N_2 plasma treatment is conducted at 300 °C for 3 min. The number of leakage current paths in the SiO_2 blocking layer adjacent to TaN is clearly reduced, but that of leakage current paths in SiO_2/HfAlO around Pd NCs is slightly increased owing to the thermal stress. The thermally induced neutral traps in the HfAlO film around the Pd NCs can be passivated by nitrogen atoms, which leads to the improvement of the final memory window for the Pd NC samples fabricated at 600–700 °C. However, the intrinsic traps in the HfAlO film play an important role in memory characteristic and the final memory window is reduced by thermal densification for the Pd NC samples fabricated at 500 °C. © 2010 The Japan Society of Applied Physics

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1. Introduction

To improve the performance of nanocrystals embedded in a nonvolatile memory (NVM), the use of metal nanocrystal (NC) structures was suggested to prolong the data retention time.[1–5] Apparent improvement in the programming speed and data retention in a nanocrystal nonvolatile memory was also observed when a high-*k* material was used instead of the conventional SiO_2.[6–9] Therefore, a combined structure of a metal nanocrystal and a high-*k* tunneling layer is expected to show better data retention characteristics. For metal-nanocrystal-embedded SiO_2, some annealing processes can induce defects or traps in the SiO_2 film around metal nanocrystals. The induced deficiency in the surrounding SiO_2 results in stored charges leaking out of the nanocrystals through trap-assisted tunneling.[10–12] Therefore, the quality of the surrounding dielectric including the blocking oxide and tunneling oxide is an important issue in metal nanocrystal memories. As is well known, a high-*k* material easily crystallizes at a high annealing temperature for the integration of metal NCs with a high-*k* material, thereby inducing leakage current paths.[13] HfAlO is a promising candidate material for use in metal nanocrystal memories owing to its higher crystallization temperature than the HfO_2 film.[14] In addition, although they are widely used in Pd metal electrodes and are a promising metal NC candidate owing to their high work function of 5.1 eV, only a few Pd nanocrystals have been used for NVM.[15] As mentioned above, for the defects induced by the fabrication process, previous research studies have mainly focused on NVMs with a SiO_2 tunneling layer. In a previous study, the induction of defects during Mo nanocrystal formation in a tunneling oxide and the reduction in the density of defects were achieved by NH_3 plasma treatment.[12] In this study, the effect of N_2 plasma treatment on electrical characteristics will be investigated for Pd nanocrystal nonvolatile memories with fabricated by different processes. Moreover, process-induced defects including the leakage current paths in dielectrics and intrinsic traps/thermally induced neutral traps in a HfAlO tunneling layer will be considered in explaining all electrical characteristics.

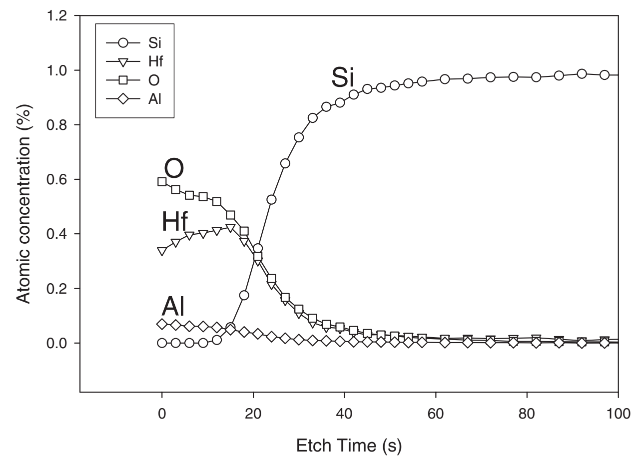

Fig. 1. Chemical compositional analysis of the as-prepared HfAlO film by AES analysis.

2. Experimental Procedure

A 5-nm-thick HfAlO film was grown on a p-type (100) substrate by the MOCVD method. The HfAlO film was deposited at 500 °C by using a combination of $Hf[OC(CH_3)_3]_2[C_5H_{11}O_2]_2$ and $Al[PCH(CH_3)_2]_3$ precursors. The chemical compositional analysis of the as-prepared sample (Hf : Al : O = 0.34 : 0.07 : 0.59–0.42 : 0.06 : 0.52) was conducted by auger electron spectrometer (AES) analysis, as shown in Fig. 1. Then, a thin Pd wetting layer (2 nm) was deposited by using an E-gun system (3×10^{-6} Torr, 40 mA and 0.02–0.03 nm/s). After Pd deposition, some samples were annealed by rapid thermal annealing at temperatures ranging from 500 to 700 °C for 30 s. Then, all annealed samples were followed by the deposition of a 25-nm-thick SiO_2 blocking oxide layer in a high density plasma CVD (HDPCVD) system. Photolithography processes were conducted, and TaN layers (50 nm) were deposited as the top electrodes by lift-off technology. Finally, Al bottom electrodes were deposited. After manufacturing a TaN/SiO_2/Pd NCs/SiO_2/Si/Al structure, partial Pd NC samples with different fabrication temperatures of Pd NCs were subjected to N_2 plasma treatment (200 mTorr, 200 W, and 200 sccm)

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with a wafer substrate at 300 °C for 3 min. To investigate the mechanism underlying the improvement in electrical characteristics, some samples were subjected to 300 °C annealing in N_2 ambient for 3 min. The capacitance–voltage (C–V) measurements were performed using a precision LCR meter (HP 4284A). In addition, leakage current and charge retention measurements were performed using a HP4156A LCR meter. The charge retention measurement was performed using the C–t method.[16] After programming/erasing at ±8 V for 10 s, the capacitance was measured at a fixed voltage $[(V_{FB1} + V_{FB2})/2]$ with varying retention time. From the variation of capacitance with retention time, the relative flat-band voltage can be deduced. Therefore, the variation of flat-band voltage in the program state and erase state can be plotted against retention time. To estimate the total number of stored electrons in the capacitor, C–V curves were also immediately measured by a voltage sweep with sufficiently fine steps after programming/erasing at ±8 V for 10 s, respectively. Hereafter, this method is called the "sweeping method". The Pd nanocrystal shape and density were determined by transmission electron microscopy (TEM) analysis. To determine whether or not the nitrogen atoms diffuse into dielectrics, the determination of atom concentration was conducted by AES.

3. Results and Discussion

After Pd deposition on HfAlO/Si using an E-gun system, Pd nanocrystals can be distinctly observed in the as-deposited film, as shown in Fig. 2(a). This observation is similar to the growth of Au on SiO_2,[5] and the density of as-deposited Pd nanocrystals on the HfAlO film is 1.87×10^{12}/cm^2. According to the TEM figure, many Pd metal islands have not yet separated well into regularly shaped nanocrystals. The relaxation of the film stress in the deposited metal layer and the surface energy minimization drive the formation of new nanocrystals during the following annealing process.[5] Therefore, the nanocrystal density and size vary linearly with increasing fabrication temperature of Pd nanocrystals, as shown in Fig. 2(b). For retention measurement, the C–t method is adopted.[16] Although the C–t method can provide a correct retention characteristic, it has difficulty in obtaining the initial memory window owing to an inevitable delay after discharging. Therefore, to obtain the total number of stored charges after charging, the sweeping method with sufficiently fine voltage steps is adopted. For the sample without plasma, typical C–V curves with the voltage swept from 8 to −8 V and then back to 8 V were obtained, as shown in Fig. 3(a). This indicates an accelerating increase of the C–V loop for the sample annealed at 700 °C. By the C–t method, after programming/erasing, the initial memory window increases at a higher rate from 500 to 600 to 700 °C (6.8 to 8 to 11.6 V), compared with the linear variation of Pd NC density, as shown in Figs. 3(b) and 2(b), respectively. For the Pd NC samples fabricated at 600–700 °C without subsequent treatment, the leakage current densities are similar to each other (see Figs. 7 and 8). Therefore, in addition to the Pd NC density and leakage current paths, the induced neutral traps in the HfAlO film also play an important role in the initial memory window of the sample at a higher fabrication temperature of Pd NCs. In other words, a higher Pd NC fabrication temperature will induce more

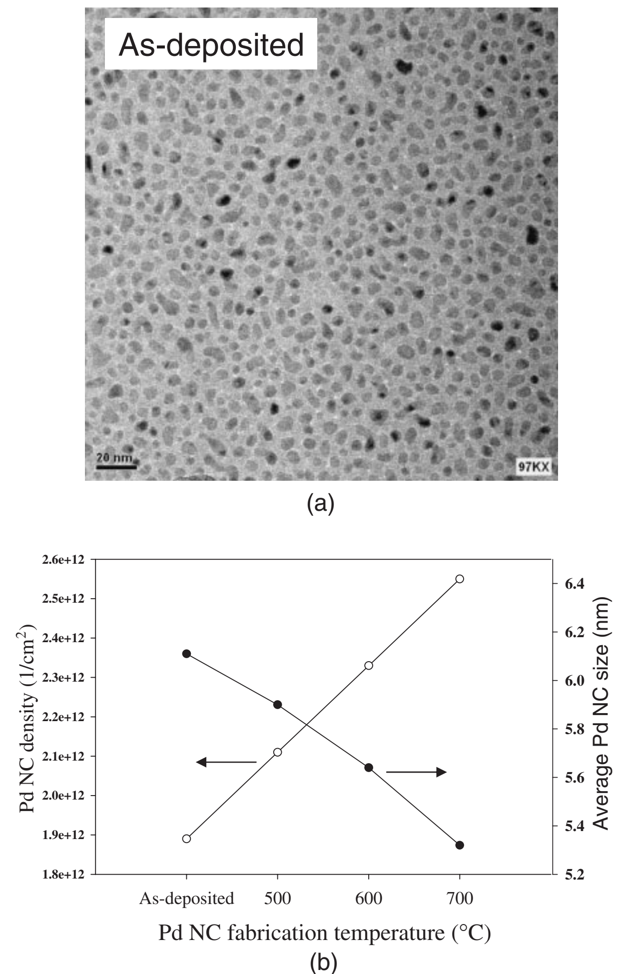

Fig. 2. (a) TEM photograph of Pd nanocrystals in as-deposited sample. (b) Density of Pd NCs as a function of Pd NC fabrication temperature.

neutral traps around Pd NCs, and this will affect the initial memory window. Al acts as a network modifier by breaking Al–O–Al bonds and producing nonbridging oxygen centers in a HfAlO film.[17] It is considered that neutral traps originate from nonbridging oxygen centers and that more thermally induced neutral traps in HfAlO around Pd NCs are obtained with increasing annealing temperature. Some researchers reported that some intrinsic traps in Hf-based oxides can be obtained after deposition and that these intrinsic traps are used in NVM application.[18,19] On the basis of previous mechanisms[10–13,18,19] and the thermally induced neutral traps mentioned above, the schematic of a defect model is shown in Fig. 4. It is considered that the intrinsic traps in the HfAlO film, the leakage current paths in the SiO_2 blocking film/HfAlO film, and the thermally induced neutral traps in the HfAlO film around Pd NCs affect the memory window and retention characteristics.

After manufacturing a TaN/SiO_2/Pd NCs/HfAlO/Si/Al structure, some samples were subjected to N_2 plasma treatment in the HDPCVD system at 300 °C for 3 min. To determine whether or not the nitrogen atoms diffuse into dielectrics, the analysis of atom concentration for the SiO_2/HfAlO/Si structure is conducted by AES analysis, and the results are plotted in Fig. 5(a). Compared with the observation in the sample without N_2 plasma treatment, more nitrogen atoms appear in the SiO_2 blocking layer and at the

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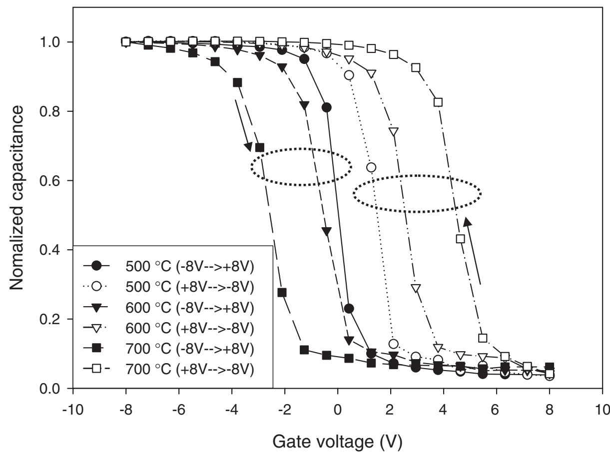


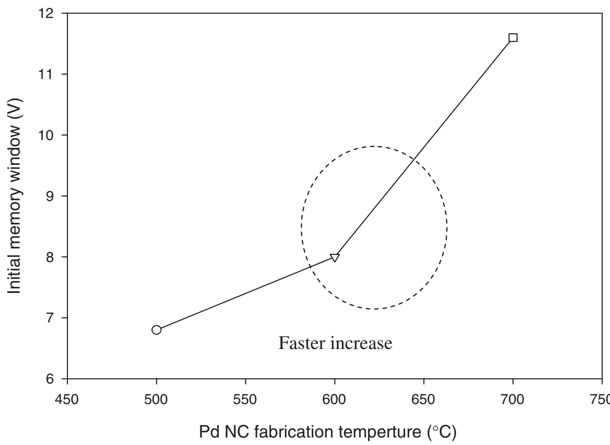
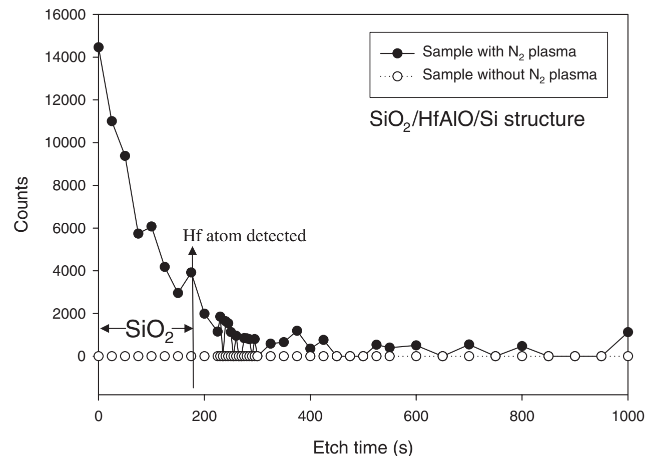


Fig. 3. (a) Typical *C*–*V* curves with the voltage swept from 8 to −8 V and then back to 8 V for the samples without subsequent treatment. (b) Initial memory window as a function of Pd NC fabrication temperature for the samples without subsequent treatment.



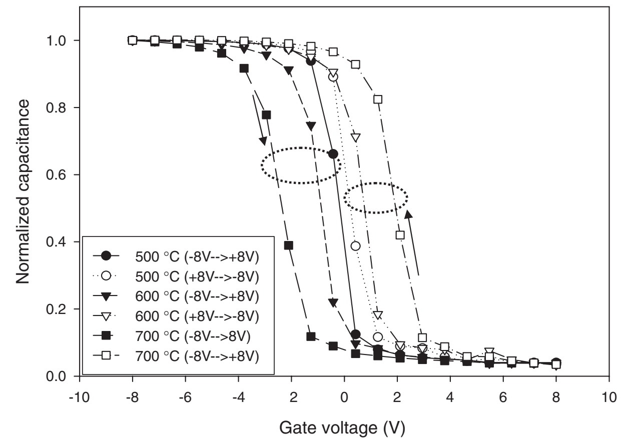


Fig. 5. (a) Profile distribution of nitrogen concentration with sputtering time determined by AES technique. (b) Typical *C*–*V* curves with the voltage swept from 8 to −8 V and then back to 8 V for the samples with N_2 plasma treatment.

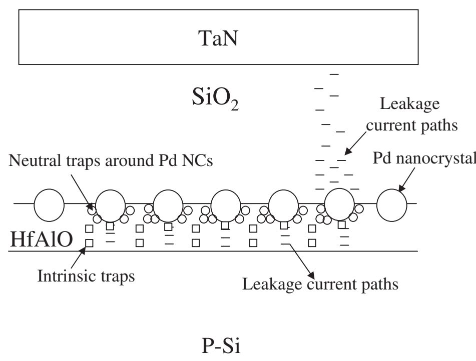


Fig. 4. Schematic of defect model for explaining the retention characteristics.

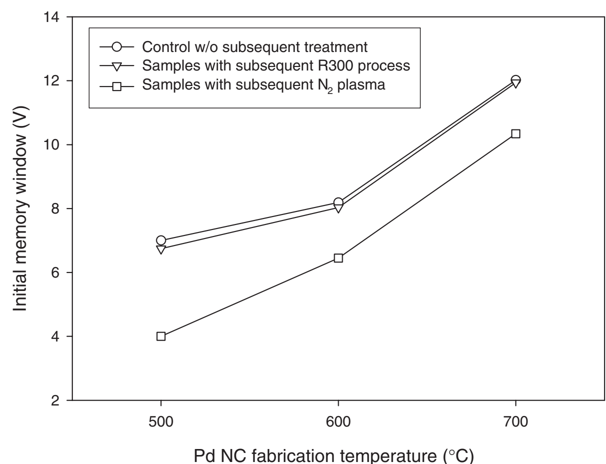


Fig. 6. Initial memory window as a function of Pd NC fabrication temperature for all samples with different subsequent processes.

SiO_2/HfAlO interface. Compared with the *C*–*V* loop in Fig. 3(a), a smaller *C*–*V* loop can be found for the sample subjected to N_2 plasma treatment, as shown in Fig. 5(b). To investigate the detailed mechanism of memory characteristic, some samples were annealed at 300 °C for 3 min in N_2 ambient after manufacturing the TaN/SiO_2/Pd NCs/HfAlO/Si/Al structure. Hereafter, this process is called the "R300" process. For different subsequent processes, the initial memory window as a function of Pd NC fabrication temperature is shown in Fig. 6. According to the defect model in Fig. 4, many defects affect the initial memory window. To determine which factor dominates the initial memory window, the leakage current densities of all the

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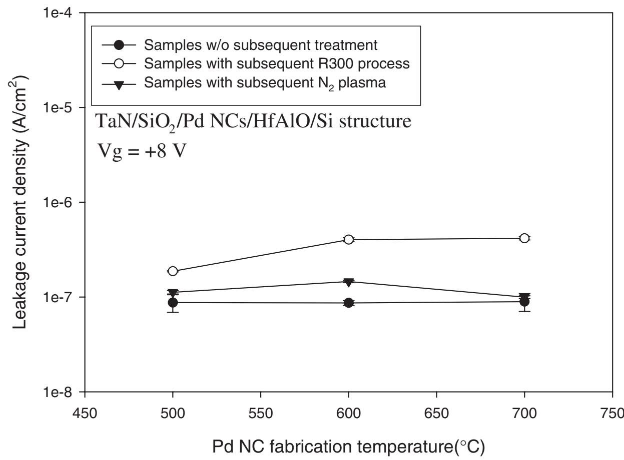

Fig. 7. Leakage current densities under +8 V gate bias for the samples with three different subsequent processes.

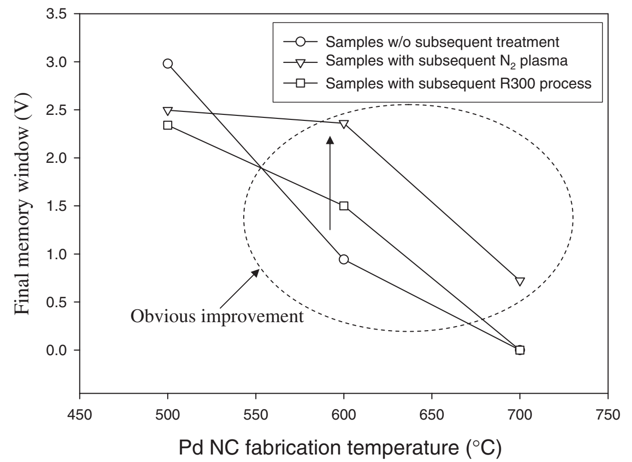

Fig. 9. Final memory windows for the samples with three different subsequent processes.

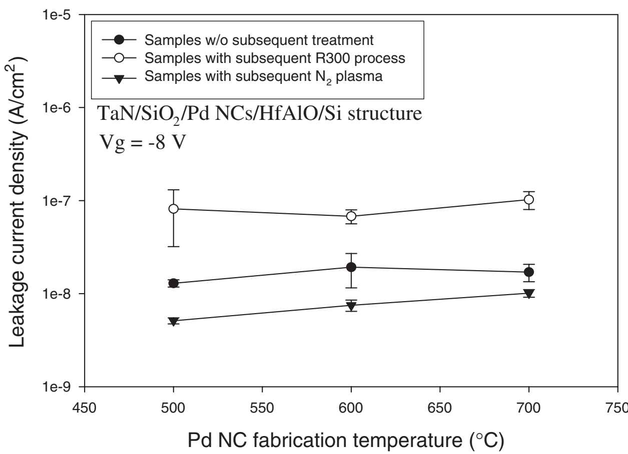

Fig. 8. Leakage current densities under −8 V gate bias for the samples with three different subsequent processes.

samples at ±8 V are measured and shown in Figs. 7 and 8, respectively. It is found that the subsequent 300 °C annealing in N_2 ambient creates additional leakage current paths in dielectrics and leads to higher leakage current densities. However, the nitrogen atoms can passivate leakage current paths in dielectrics, thereby leading to lower leakage current densities for the samples with subsequent N_2 plasma treatment. Compared with that observation in the samples without subsequent treatment, further nitrogen diffusion near the metal TaN/SiO_2 interface results in lower leakage current densities at −8 V due to gate injection, but slightly higher leakage current densities are found at +8 V due to the thermal stress in dielectrics around the Pd NCs for the samples with subsequent N_2 plasma treatment. Similarly to the samples without subsequent treatment, the other samples show small variations of leakage current densities with different Pd NC fabrication temperatures. Although the leakage currents of the samples subjected to the R300 process are always higher than those of the control samples, the initial memory windows are similar to each other at the same Pd fabrication temperature. Therefore, it is considered that the Pd NC density, the intrinsic traps in the HfAlO film, and the induced neutral traps in the HfAlO film around the Pd NCs dominantly determine the initial memory window. Owing to nitrogen diffusion, the number of thermally induced neutral traps in the HfAlO film around the Pd NCs is reduced and lower initial memory windows are observed for the samples with subsequent N_2 plasma treatment. For the 500 °C annealed sample with N_2 plasma treatment, more nitrogen atoms can diffuse into the traps beneath Pd NCs owing to the fewer thermally induced neutral traps in the HfAlO film around the Pd NCs. Therefore, a larger reduction in the number of the neutral traps beneath Pd NCs results in a clearer variation of V_{FB} during charging.

Figure 9 shows the final memory window after discharging for 1800 s as a function of different Pd NC fabrication temperature. In contrast to the initial memory window, the final memory window decreases with increasing Pd NC fabrication temperature. Previous research indicates that the trap-assisted tunneling in SiO_2 dominates charge loss due to thermal stress in the SiO_2 film.[9,10] The leakage current through Hf-based dielectrics dominated by trap-assisted tunneling has been reported.[17] In this work, the leakage current density of a TaN/25 nm SiO_2/Pd NCs/5 nm HfAlO/Si structure is much lower than that of a TaN/Pd NCs/5 nm HfAlO/Si by at least 7 orders of magnitude. It is considered that the charging and discharging mainly occur between Pd nanocrystals and the Si substrate through the HfAlO tunneling layer for all the annealed samples. The leakage current densities of the TaN/Pd NCs/HfAlO/Si structures with different Pd NC fabrication temperatures at −8 V are shown in Fig. 10. Results indicate that the leakage current densities for different Pd NC fabrication temperatures are similar to each other for the samples subjected to N_2 plasma treatment and the R300 process, but the final memory window for the samples with N_2 plasma treatment is always larger than that for the samples with the R300 process. Therefore, the Pd NC density, the intrinsic traps in the HfAlO film, and the thermally induced neutral traps in the HfAlO film around the Pd NCs dominantly determine the variation of the final memory window at different Pd NC fabrication temperatures. After N_2 plasma treatment, a clear improvement of the final memory window due to the reduction in the number of thermally induced neutral traps

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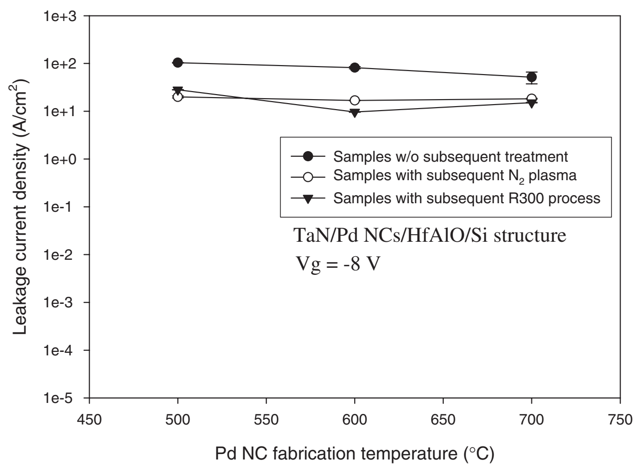

Fig. 10. Leakage current densities under −8 V gate bias for the TaN/Pd NCs/HfAlO/Si structure with three different subsequent processes.

by nitrogen passivation for the samples fabricated at 600–700 °C can be observed. During charging, most charges are captured in the thermally induced neutral traps instead of in Pd NCs for the samples fabricated at 700 °C, and the charges are easily released from these traps. For the samples with subsequent N_2 plasma treatment, a large reduction in the number of neutral traps is observed and more charges are stored in the Pd NCs. This results in the improvement of the final memory window. However, the improvement of the final memory window is limited because of the lack of nitrogen passivation for the samples with the subsequent R300 process. Compared with the samples annealed at 600–700 °C, the samples fabricated at 500 °C have fewer thermally induced neutral traps that are due to the lower thermal stress from Pd NCs. According to Fig. 10, the number of leakage current paths is reduced after the N_2 plasma process or 300 °C annealing. It is also considered that the number of intrinsic traps in the HfAlO film can be reduced by thermal densification. Moreover, the intrinsic traps in the HfAlO film dominate the variation of flat-band voltage for the samples annealed at 500 °C. Therefore, the final memory window of the sample without subsequent treatment is larger than that for the samples subjected to N_2 plasma treatment and the R300 process for the samples fabricated at 500 °C, Experimental results indicate that N_2 plasma treatment can effectively passivate the thermally induced neutral traps resulting from the thermal stress during Pd NC formation, which leads to a better retention characteristic of the samples with higher fabrication temperatures of Pd NCs (600–700 °C).

4. Conclusions

Pd nanocrystals can be successfully embedded in a TaN/SiO_2/HfAlO/Si structure. For the 600–700 °C-fabricated samples, the thermally induced neutral traps in the HfAlO film around Pd NC play an important role in determining the memory window. Moreover, N_2 plasma treatment can effectively reduce the number of thermally induced neutral traps resulting from the thermal stress during Pd NC formation and achieve a better retention characteristic. For the Pd NC samples fabricated at 500 °C, the intrinsic traps play an important role in memory characteristic and the final memory window is reduced by thermal densification.

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