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The Impact of Uni-axial Strain on Low Frequency Noise in Nanoscale p-Channel Metal–Oxide–Semiconductor Field Effect Transistors under Dynamic Body Biases

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The impact of local strain on low frequency noise (LFN) in p-channel metal–oxide–semiconductor field effect transistor (pMOSFET) is investigated under dynamic body biases. For 60 nm pMOSFET, the uni-axial compressive strain from embedded SiGe (e-SiGe) in source/drain can contribute 75% effective mobility (μ_{eff}) enhancement and the proportional improvement in current (I_{DS}) as well as transconductance (G_m). However, the strained pMOSFET suffer more than 80% higher LFN ($S_{ID}/I_D{}^2$) compared with the control pMOSFET free from strain engineering. The measured LFN can be consistently explained by mobility fluctuation model and the increase of Hooge parameter (α_H) appears as a key factor responsible for the higher LFN in strained pMOSFET. Forward body biases (FBB) is proposed as an effective method adapted to nanoscale devices for improving μ_{eff} and suppressing LFN, without resort to strain engineering.

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1. Introduction

Strain engineering has been introduced as an indispensable technology for increasing the mobility and driving current, especially useful for nanoscale devices.[1–3] The fast gate speed driven by the mobility and current indeed contributes superior f_T and f_{max}, the key performance parameters for RF/analog circuits.[4,5] Since strain engineering has the potential impact on noise, particularly the low frequency noise (LFN) or flicker noise, it attracts increasing research effort in recent years. There exist a lot of controversies in the experimental results and proposed mechanisms on this topic.[6–9] Maeda *et al.* reported flicker noise increases in p-channel metal–oxide–semiconductor field effect semiconductors (pMOSFET) under both compressive and tensile stress, namely bi-directional noise degradation.[7] Stress induced excess traps and dipoles were assumed responsible for flicker noise degradation. Guisi *et al.* also concluded that SiGe recess source/drain (S/D) regions give rise to a significant enhancement of the trap density in the SiO_2/HfO_2 gate stack.[8] However, Ueno *et al.* claimed improved $1/f$ noise in pMOSFET with embedded-SiGe (e-SiGe) for local compressive stress,[9] and controverted Maeda's results as inclusive owing to side effects other than stress. In fact, there remain many open questions deserving an extensive investigation, e.g., the abnormally large LFN revealed in pMOSFET compared to nMOSFET with stress free liner and number fluctuation model assumed for pMOSFET.

Dynamic body biases method is proposed as an alternative solution aside from strain engineering, to achieving mobility and current enhancement. In fact, dynamic body biases have been extensively adopted in modern circuit design and proven as the most promising method to facilitate low power design in nanoscale complementary metal–oxide–semiconductor (CMOS) platform, known as dynamic threshold voltage CMOS (DTMOS).[10,11]

In this paper, novel and interesting results of uni-axial compressive strain effect on LFN in pMOSFETs under dynamic body biases are presented. The pMOSFET adopting e-SiGe S/D for uni-axial compressive strain were fabricated for mobility enhancement. A comprehensive characterization was carried out to investigate the local strain effect on mobility, current, short channel integrity, and most importantly LFN. Dynamic body biases scheme consisting of forward body bias (FBB), zero body bias (ZBB), and reverse body bias (RBB) was employed to explore the influence on LFN. Mobility fluctuation model can explain the strain and dynamic body biases effect in nanoscale pMOS and Hooge parameter manifests itself a critical dependence on both effects.

2. Device Fabrication and Characterization

The strained pMOSFET with e-SiGe in S/D for uni-axial compressive strain were fabricated in 65 nm high performance CMOS process and the standard pMOS free from strain engineering act as the control devices. Four-terminal device layout was implemented with four individual pads for four electrodes (G/D/S/B) to enable a freedom of body biases. The gate width (W) was fixed at 10 μm while the gate lengths drawn on layout (L_{drawn}) varied in a wide range from 10 to 0.08 μm. An etching bias of 0.02 μm leads to physical gate length $L_g = L_{drawn} - 0.02\,\mu m$, i.e., the minimal L_g down to 0.06 μm (60 nm). Interface trap density N_{it} was extracted by using the incremental frequency charge pumping (IFCP) method.[12]

The power spectral density (PSD) of drain current noise, namely S_{ID} was measured by LFN measurement system, consisting of Agilent dynamic signal analyzer (DSA 35670) and low noise amplifier (LNA SR570). The LFN measurement generally covers a wide frequency range of 10 Hz to 100 kHz.

3. Local Strain Engineering Effect on pMOSFET Performance

3.1 Effective mobility μ_{eff} enhancement from uni-axial strain

The uni-axial compressive strain can realize around 80% boost in linear I_{DS} and maximum G_m for 60 nm pMOSFET due to the uni-axial compressive strain.[3] Note that the gate overdrive $V_{GT} = V_{GS} - V_T$ was used to replace V_{GS} as the expression in this work to eliminate the V_T offset due to strain engineering. In this way, a fair comparison of electrical performance between the strained and control pMOSFET can be approached.

Figure 1 presents the effective mobility μ_{eff} extracted from linear drain current–gate voltage (I_D–V_{GS}) character-

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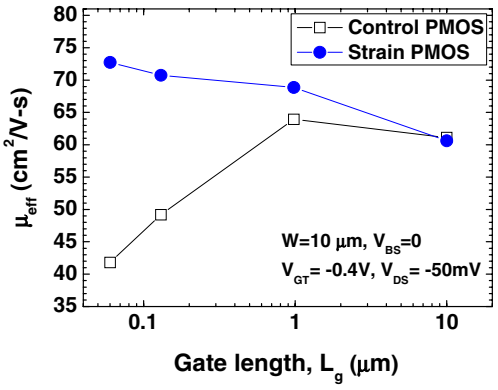

Fig. 1. (Color online) Effective mobility μ_{eff} extracted from linear I–V characteristics for strained and control pMOSFETs over various gate lengths, $L_g = 0.98-0.06\,\mu m$.

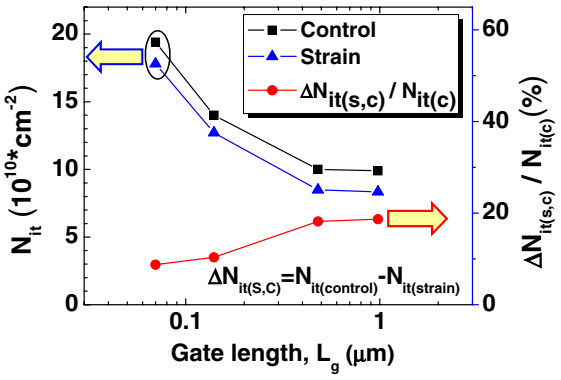

Fig. 2. (Color online) Interface trap density N_{it} vs L_g (0.07, 0.14, 0.48, and 0.98 μm), measured at $V_D = V_S = V_B = 0\,V$ and $V_G = V_{amp} = 1.4\,V$ for control and strained pMOSs.

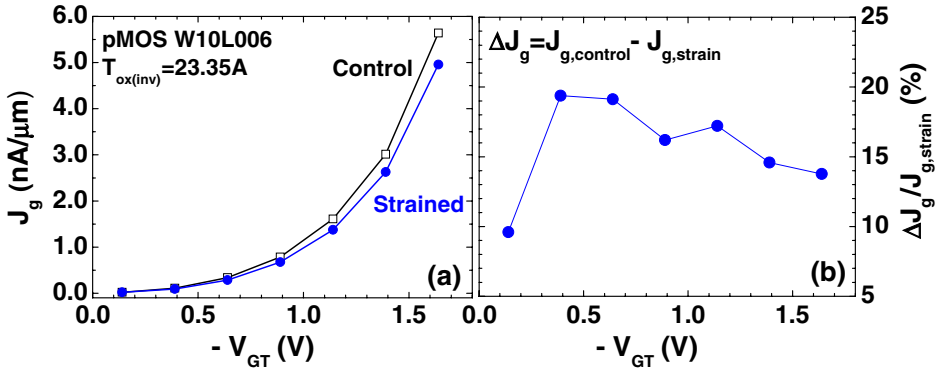

Fig. 3. (Color online) (a) Gate current density J_g vs V_{GT}. (b) Gate current density difference: $\Delta J_{g(c,s)}/J_{g,s}$ vs V_{GT}, $\Delta J_{g(c,s)} = J_{g,c} - J_{g,s}$, measured at $V_D = V_S = V_B = 0\,V$ and varying V_{GT} ($V_{GT} = V_{GS} - V_T$) in -0.4 to $-0.8\,V$, for control and strained pMOSFETs with $L_g = 60\,nm$.

istics. The dependence of μ_{eff} on gate length L_g for strained and control pMOSFET is in an opposite direction. Strained pMOSFET gets higher μ_{eff} for shorter L_g but the control one suffers a dramatic degradation in μ_{eff}. As a result, the μ_{eff} enhancement due to this local strain can attain 75% for 60 nm devices, which contributes near 80% increase of I_{DS} and G_m in linear region.[3] Furthermore, the μ_{eff} enhancement in linear region contributes around 65% higher I_{DS} and G_m in saturation region (not shown). The μ_{eff} enhancement realized in strained pMOSFET with sufficiently short L_g manifests the local compressive strain effect from e-SiGe S/D. On the other hand, the dramatic μ_{eff} degradation with L_g reduction revealed in control pMOS suggests an aggravated impurity scattering due to halo implantation located near the channel region in sufficiently short devices.

3.2 Interface traps and gate current: Uni-axial strain effect

Strain effect on interface traps is one of major concerns for the deployment of strain engineering in the state-of-the-art process. Figure 2 indicates the interface trap density N_{it} extracted by incremental frequency charge pumping (IFCP) method[12] for control and strained devices with various L_g. It is found that the control pMOSFET revealed somewhat higher N_{it}. The difference of N_{it} between the control and strained pMOSFET, namely $\Delta N_{it(s,c)}$ and normalized to that of control pMOS, denoted as $\Delta N_{it(s,c)}/N_{it(c)}$ is around 10–20% over various L_g. However, the $\Delta N_{it(s,c)}/N_{it(c)}$ decreases with decreasing channel length L_g. This result suggests that uni-axial compressive stress does not introduce additional interface traps. Meanwhile, the N_{it} in channel region increases with downscaling L_g for both control and strained pMOSFET. Gate edge damage or longitudinal shallow trench isolation (STI) stress along the direction of channel length are proposed as the potential mechanisms responsible for the increase of N_{it} in shorter devices.

The strain effect on gate leakage currents is one more critical concern for nanoscale devices under low power applications. The comparison between the strained and control pMOSFET, shown in Fig. 3 indicates that the uni-axial compressive strain can help reduce gate leakage current density J_g, attributed to larger out-of-plane effective mass.[13] For L_g at 60 nm, the strained pMOSFET can achieve 15–20% lower J_g over V_{GT} (-0.4 to $-1.8\,V$), shown in Fig. 3(b). The effective J_g reduction is a great benefit offered by the compressive strain to pMOS. Note that the J_g tends to increase with gate length scaling for both strained and control pMOS (not shown for brevity). The result suggests that the edge component of J_g is larger than that of area component and can be explained by the increasing impact from longitudinal STI stress or gate edge damage along the channel length.

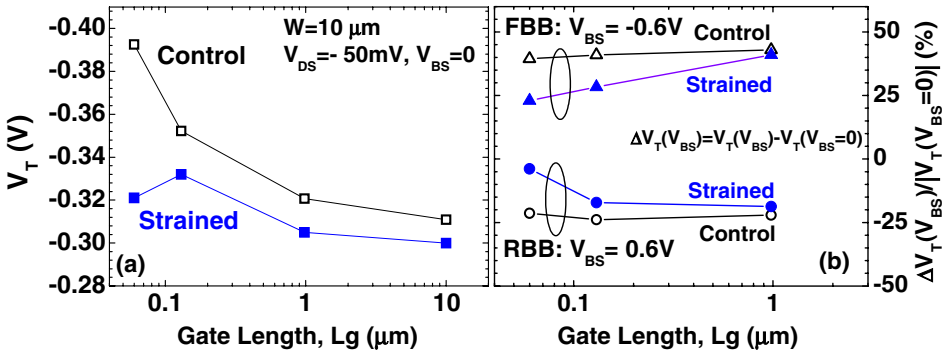

Fig. 4. (Color online) (a) Linear V_T measured at $V_{DS} = -50$ mV, $V_{BS} = 0$ for strained and control pMOSFET (b) V_T shift due to V_{BS}, normalized to $V_T(V_{BS} = 0)$: $\Delta V_T(V_{BS})/V_T(V_{BS} = 0)$, $\Delta V_T(V_{BS}) = V_T(V_{BS}) - V_T(V_{BS} = 0)$ measured under FBB ($V_{BS} = -0.6$ V) and RBB ($V_{BS} = 0.6$ V) for strained and control pMOSFET with $L_g = 0.06$, 0.13, and 0.98 μm.

3.3 Threshold voltage V_T and body bias sensitivity

Figure 4(a) presents the threshold voltage V_T versus L_g with a dramatic difference between the strained and control pMOSFET, due to the uni-axial compressive strain. The control pMOSFET show an apparent reverse short channel effect (RSCE) but the strained pMOSFET reveal a V_T roll-off for L_g scaling to 60 nm. Halo implantation introduced lateral non-uniform profile is the major cause responsible for RSCE. For strained pMOSFET, uni-axial strain induced bandgap narrowing (or valence band offset for holes) and S/D recess in e-SiGe are two potential reasons for the worse SCE and V_T roll-off.[14] Figure 4(b) indicates V_T shift due to FBB ($V_{BS} = -0.6$ V) and RBB ($V_{BS} = 0.6$ V) and normalized to that under ZBB ($V_{BS} = 0$), namely $\Delta V_T(V_{BS})/V_T(V_{BS} = 0\,\text{V})$ over various L_g. For pMOSFET, the FBB enables a positive V_T shift toward lower $|V_T|$ whereas RBB leads to a negative V_T shift toward higher $|V_T|$. Note that the strained pMOSFET have a smaller V_T shift under both FBB and RBB, particularly for 60 nm device due to SCE featured by a remarkable V_T roll off, shown in Fig. 4(a). This feature will influence dynamic body bias effect on μ_{eff} and LFN as discussed later. The degraded V_T tunability and sensitivity under dynamic body biases emerges as a potential impact.

3.4 Local strain and body biases effect on effective mobility μ_{eff}

For pMOSFETs, the E_{eff} can be calculated by eq. (1) in which V_T dependence on body biases (V_{BS}) makes a major contribution. Under the dynamic body biases, μ_{eff} of both control and strained pMOSFET decreases with increasing E_{eff} and can be fitted by a simple model in eq. (2), in which γ keeps near 0.3 for various L_g (0.06–0.98 μm). The E_{eff} dependence of μ_{eff} suggests phonon scattering as the dominant mechanism[15] under an operation at room temperature, and the mechanism is applied to both strained and control pMOSFET:

$$E_{eff} = \frac{V_{GT} + 3V_T}{9T_{OX}}, \quad (1)$$

$$\mu_{eff} = \mu_0 \left(\frac{E_{eff}}{E_0}\right)^{-\gamma}. \quad (2)$$

Figure 5 presents the normalized μ_{eff} shift $[\Delta\mu_{eff}(V_{BS})/\mu_{eff}(V_{BS} = 0)]$ under FBB and RBB, over various L_g. The FBB enables a positive μ_{eff} shift whereas RBB leads to a negative μ_{eff} shift. The magnitude of $\Delta\mu_{eff}(V_{BS})$ increases

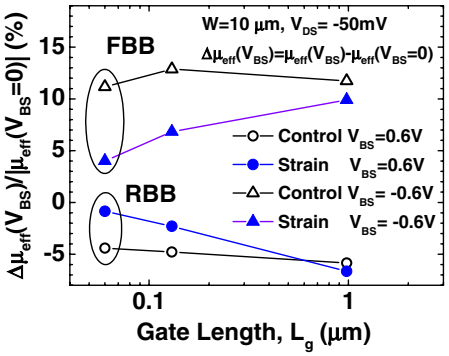

Fig. 5. (Color online) The μ_{eff} shift due to V_{BS} and normalized to $\mu_{eff}(V_{BS} = 0)$: $\Delta\mu_{eff}(V_{BS})/\mu_{eff}(V_{BS} = 0)$, $\Delta\mu_{eff}(V_{BS}) = \mu_{eff}(V_{BS}) - \mu_{eff}(V_{BS} = 0)$ measured under FBB ($V_{BS} = -0.6$ V) and RBB ($V_{BS} = 0.6$ V) for strained and control pMOSFETs with $L_g = 0.06$, 0.13, and 0.98 μm.

with decreasing L_g no matter whether it is a positive or a negative shift. The strained pMOSFET indicate a smaller value in $\Delta\mu_{eff}(V_{BS})/\mu_{eff}(V_{BS} = 0)$ under both FBB and RBB, particularly for 60 nm device. It can be understood that the smaller body bias effect on V_T in strained pMOSFET, shown in Fig. 4(a) leads to smaller E_{eff} variation and then the smaller $\Delta\mu_{eff}(V_{BS})$ according to eqs. (1) and (2).

4. Local Strain Engineering Effect on LFN in pMOSFETs

4.1 Uni-axial strain and dynamic body bias effect on S_{ID}/I_{DS}^2

The LFN measured from 60 nm pMOSFET and expressed in terms of S_{ID}/I_{DS}^2 under varying frequencies is shown in Fig. 6. Unfortunately, the strained pMOSFET suffers much higher S_{ID}/I_{DS}^2 than control pMOSFET over a wide range of frequencies in 10 Hz–100 kHz. Therefore, the impact of uni-axial strain on LFN in nanoscale pMOSFETs appears as a critical concern, particularly for analog and RF circuit design.

Figure 7(a) shows S_{ID}/I_{DS}^2 under a specified $V_{GT} = -0.4$ V for strained and control pMOSFET with various L_g. For long channel devices, e.g., $L_g = 0.98$ μm, strained and control pMOSFET demonstrate similar LFN characteristics in S_{ID}/I_{DS}^2. However, for shorter L_g going down to 0.13 μm and below, the strained pMOSFET suffer obviously higher S_{ID}/I_{DS}^2. Figure 7(b) presents S_{ID}/I_{DS}^2 multiplied with device gate width and length ($W \times L_g$). Interestingly,

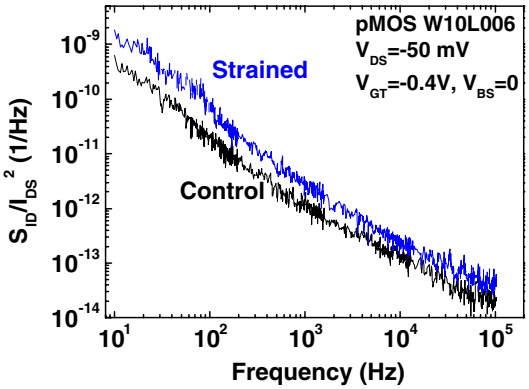

Fig. 6. (Color online) LFN measured for 60 nm pMOSFET under $V_{GT} = -0.4$ V and $V_{BS} = 0$. The LFN is represented as S_{ID}/I_{DS}^2 for a fair comparison between strained and control devices with different I_{DS}. S_{ID}/I_{DS}^2 is the normalized PSD of drain current noise.

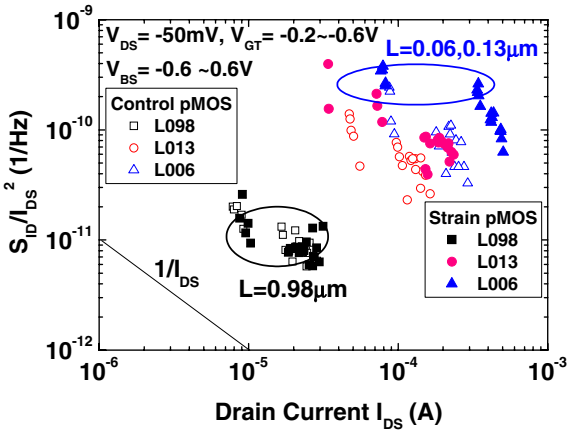

Fig. 8. (Color online) S_{ID}/I_{DS}^2 versus I_{DS}, measured under varying V_{GT} ($V_{GT} = -0.2$ to -0.6 V) and body biases ($V_{BS} = -0.6$, 0, 0.6 V) for strained and control pMOSFET with various $L_g = 0.06$, 0.13, and 0.98 μm.

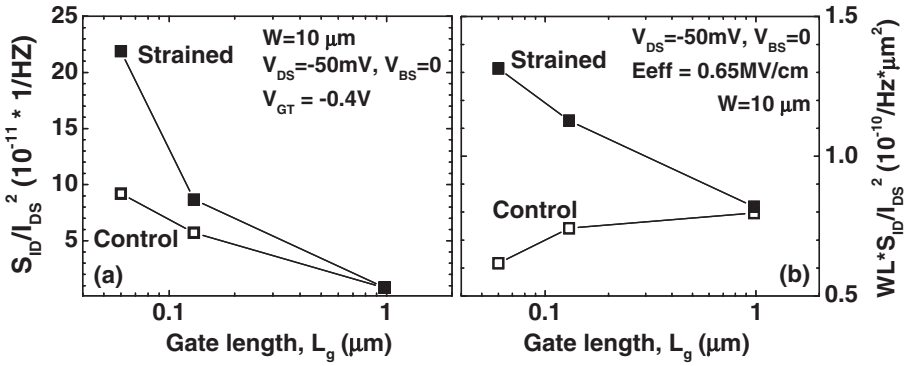

Fig. 7. S_{ID}/I_{DS}^2 measured under a specified E_{eff} of 0.65 MV/cm for strained and control pMOSFET with $L_g = 0.06$, 0.13, and 0.98 μm: (a) S_{ID}/I_{DS}^2; (b) $S_{ID}/I_{DS}^2 \times WL_g$.

opposite trends are demonstrated for the strained and control devices in $S_{ID}/I_{DS}^2 \times WL_g$ against L_g scaling. The control pMOSFET indicate a decreasing function whereas the strained pMOSFET reveal an increasing trend versus L_g scaling. Therefore, Fig. 7(a) indicates a remarkably faster increase of S_{ID}/I_D^2 with L_g scaling for strained pMOSFET and more than 80% higher S_{ID}/I_D^2 in 60 nm devices compared with the long channel device ($L_g = 0.98$ μm). This result actually is in contradiction with what was published for nMOSFET and cannot be explained by the well-known number fluctuation model.[16] Referring to Fig. 4(a), the dramatic RSCE revealed in control pMOSFET indicates a highly non-uniform channel doping profile due to halo implantation and potentially worse LFN based on the number fluctuation model.[16] However, the experimental for pMOSFET exhibits an opposite trend that is the control pMOSFET with apparently worse RSCE have much lower LFN.

Regarding other potential reasons responsible for the worse LFN in strained pMOSFET, like stress induced excess traps or dipoles proposed by Maeda *et al.*,[7] they cannot be justified due to a contraction with the measured gate leakage currents J_g in which the strain pMOSFET presents a lower J_g than control pMOSFET, shown in Fig. 3. In addition, a remarkably different trend in strain engineering effect on LFN in terms of $(\Delta S_{ID(s,c)}/I_D^2)/(S_{ID(c)}/I_D^2)$ as shown in Fig. 7 and interface traps density denoted as $\Delta N_{it(s,c)}/N_{it(c)}$ shown in Fig. 2 under L_g scaling suggests that carrier number fluctuation is no longer an appropriate model to explain our observation. Note that $\Delta S_{ID(s,c)}/I_D^2$ means the difference between $S_{ID(s)}/I_D^2$ (strained) and $S_{ID(c)}/I_D^2$ (control). With the downscaling of L_g, the $\Delta N_{it(s,c)}/N_{it(c)}$ decreases whereas $(\Delta S_{ID(s,c)}/I_D^2)/(S_{ID(c)}/I_D^2)$ increases significantly. The measured results are exactly in contradiction with the number fluctuation model, according to which the LFN (S_{ID}/I_D^2) is proportional to the interface trap density N_{it}.[17]

The aforementioned arguments motivate our interest in exploring a truly appropriate model for an accurate prediction of LFN in pMOSFET. Figure 8 exhibits S_{ID}/I_{DS}^2 versus I_{DS} under various V_{GT}, V_{BS}, and L_g for both strained and control pMOS. Herein, the S_{ID}/I_{DS}^2 follows a function proportional to $1/I_{DS}$ over the whole range of bias conditions. The results indicate that mobility fluctuation model derived according to Hooge empirical formulas, given by eq. (3) or (4) is the dominant mechanism governing pMOSFETs' LFN:[18]

$$\frac{S_{ID}}{I_{DS}^2} = \frac{1}{f}\frac{qV_{DS}}{I_{DS}}\frac{\alpha_H \mu_{eff}}{L_{eff}^2}, \tag{3}$$

$$\frac{S_{ID}}{I_{DS}^2} = \frac{q}{f}\frac{1}{WL_{eff}C_{ox}} \times \frac{\alpha_H}{V_{GT}}, \quad V_{GT} = (V_{GS} - V_T), \tag{4}$$

where α_H is the Hooge parameter and L_{eff} is the effective channel length.

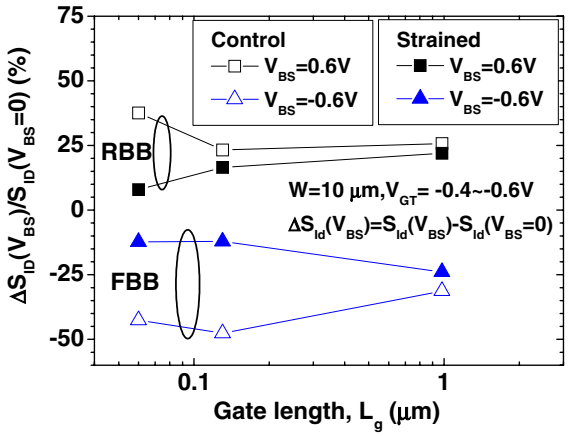

Fig. 9. (Color online) Change of S_{ID} under FBB (V_{BS} = −0.6 V) as well as RBB (V_{BS} = 0.6 V) and normalized to the reference S_{ID} at ZBB (V_{BS} = 0), denoted as $\Delta S_{ID}(V_{BS})/S_{ID}(V_{BS}=0)$ measured for strained and control pMOSFET with various L_g = 0.06, 0.13, and 0.98 μm.

Note that S_{ID}/I_{DS}^2 exhibits a dramatic increase with L_g scaling in both strained and control devices, and strained pMOSFET suffer much higher LFN in terms of S_{ID}/I_{DS}^2 for aggressively scaled dimensions at 0.13 μm and 60 nm. The mobility fluctuation model with an expression of eq. (3) for varying I_{DS} or eq. (4) for varying V_{GT} can predict the dependence of the dramatic increase of S_{ID}/I_{DS}^2 on device parameters (W, L_{eff}, C_{ox}, μ_{eff}, α_H, I_{DS}, V_{GT}) and more importantly help explore the origins responsible for the worse LFN in strained pMOSFET. The increase of effective mobility (μ_{eff}) or Hooge parameter (α_H) and the decrease of effective channel length (L_{eff}) will lead to higher LFN in terms of S_{ID}/I_{DS}^2 under the specified I_{DS}. For the strained pMOSFET, the implantation profile difference reflected by Fig. 4 may also contribute to shorter effective channel length and lead to higher LFN. It explains why the strained pMOSFET with short L_g (0.13 and 0.06 μm) indeed gain the benefit of higher μ_{eff} but suffer worse LFN, as shown in Figs. 7 and 8. According to eq. (4), the effective ways to suppressing LFN can be the increase of device dimensions (W, L_{eff}), the increase of $|V_{GT}|$, and the reduction of α_H. The local strain cooperating with body biases effect on the Hooge parameter α_H emerges as an interesting topic.

As it is well known that dynamic body biases method has been proven in DTMOS platform for low power design, we propose that this method may become a potential solution for low noise design. Figure 9 presents the dynamic body biases effect on LFN in terms of $\Delta S_{ID}(V_{BS})/S_{ID}(V_{BS}=0)$ where $\Delta S_{ID}(V_{BS}) = S_{ID}(V_{BS}) - S_{ID}(V_{BS}=0)$ under FBB ($V_{BS} = -0.6$ V) and RBB ($V_{BS} = 0.6$ V). For both strained and control pMOSFETs, FBB can reduce S_{ID} [$\Delta S_{ID}(V_{BS}) < 0$] attributed to reduced normal effective field E_{eff}. On the other hand, RBB makes LFN worse with $\Delta S_{ID}(V_{BS}) > 0$. However, the dynamic body bias effect on LFN is degraded in strained pMOSFET with a smaller amount of $\Delta S_{ID}(V_{BS})/S_{ID}(V_{BS}=0)$, particularly worse for the shortest devices with $L_g = 60$ nm. The significant V_T lowering and degraded body bias effect shown in Fig. 4 for strained pMOSFET explains the diminishing benefit from FBB on LFN.

Table I presents the strain effect on LFN and μ_{eff} in terms of normalized amount such as $[\Delta S_{ID(s,c)}/I_D^2(V_{BS})]/[S_{ID(c)}/I_D^2(V_{BS})]$ and $\Delta\mu_{eff(s,c)}(V_{BS})/\mu_{eff(c)}$ under dynamic body biases ZBB (V_{BS} = 0), FBB (V_{BS} = −0.6 V), and RBB (V_{BS} = 0.6 V), and V_{GT} = −0.4 V. Data were measured from control and strained pMOSFETs with L_g = 0.06, 0.13, and 0.98 μm.

Table I. The strain effect on LFN and μ_{eff} in terms of $[\Delta S_{ID(s,c)}/I_D^2(V_{BS})]/[S_{ID(c)}/I_D^2(V_{BS})]$ and $\Delta\mu_{eff(s,c)}(V_{BS})/\mu_{eff(c)}$ under dynamic body biases ZBB (V_{BS} = 0), FBB (V_{BS} = −0.6 V), and RBB (V_{BS} = 0.6 V), and V_{GT} = −0.4 V. Data were measured from control and strained pMOSFETs with L_g = 0.06, 0.13, and 0.98 μm.

L_g (μm)	$[\Delta S_{ID(s,c)}/I_D^2(V_{BS})]/[S_{ID(c)}/I_D^2(V_{BS})]$			$\Delta\mu_{eff(s,c)}(V_{BS})/\mu_{eff(c)}$		
	0.98	0.13	0.06	0.98	0.13	0.06
FBB (%)	1	156	209	5	37	64
ZBB (%)	0	55	128	7	44	75
RBB (%)	−29	41	10	7	48	85

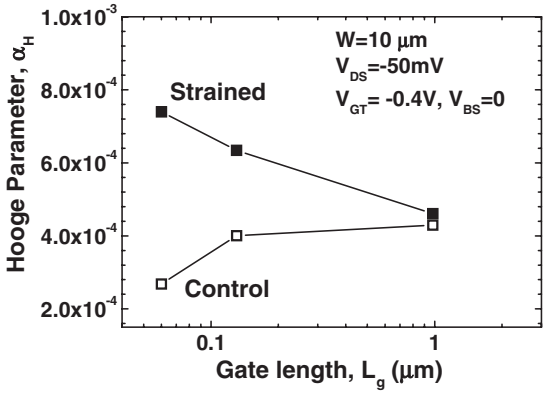

Fig. 10. Hooge parameter α_H extracted from S_{ID}/I_{DS}^2 measured under V_{GT} = −0.4 V and V_{BS} = 0 for strained and control pMOSFET with various L_g (0.98, 0.13, 0.06 μm).

$I_D^2(V_{BS})]$ and $\Delta\mu_{eff(s,c)}(V_{BS})/\mu_{eff(c)}$ at $V_{GT} = -0.4$ V and under dynamic body biases (FBB, ZBB, RBB). Note that $\Delta S_{ID(s,c)}/I_D^2(V_{BS})$ is defined as $S_{ID(s)}/I_D^2 - S_{ID(c)}/I_D^2$ and $\Delta\mu_{eff(s,c)}(V_{BS})$ is equal to $\mu_{eff(s)} - \mu_{eff(c)}$ under a specified V_{BS}. The results summarized in Table I reveal interesting effects from dynamic body biases. For FBB, the increase of LFN in strained pMOSFETs $[S_{ID(s)}/I_D^2(V_{BS})]$ compared to control pMOSFET $[S_{ID(c)}/I_D^2(V_{BS})]$ becomes larger whereas the μ_{eff} enhancement in strained pMOSFET over the control ones becomes smaller. As for RBB, an opposite trend was demonstrated for LFN and μ_{eff}, i.e., the increase of LFN due to strain gets smaller but the μ_{eff} enhancement over control ones becomes larger. It can be explained that the control pMOSFET benefit from FBB in the suppression of $S_{ID(c)}/I_D^2(V_{BS})$ and enhancement of $\mu_{eff(c)}$, attributed to lower E_{eff} from FBB. In this way, the control pMOSFET has much less LFN than strained pMOSFET and it is demonstrated with larger difference in $S_{ID}/I_D^2(V_{BS})$ given by $\Delta S_{ID(s,c)}/I_D^2(V_{BS})$. Also, the larger FBB effect in control pMOSFET facilitates more E_{eff} reduction and μ_{eff} enhancement, and then the smaller difference from that of strain pMOSFET denoted as $\Delta\mu_{eff(s,c)}(V_{BS})$.

4.2 Strain and body biases effect on Hooge parameter α_H

Referring to Table I, mobility fluctuation model given by eq. (3) or (4) is the most relevant mechanism to explain the uni-axial compressive strain effect on LFN of pMOSFET, and Hooge parameter α_H appears as the most key factor determining LFN in terms of S_{ID}/I_D^2. Figure 10 makes a comparison of α_H between the strained and control pMOSFETs over various L_g, and exhibits a remarkable

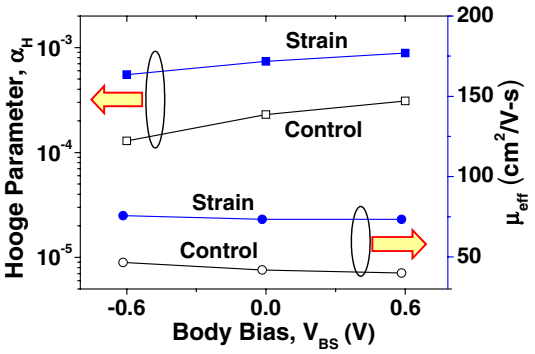

Fig. 11. (Color online) Hooge parameter α_H extracted from $S_{ID}/I_{DS}{}^2$ and Effective mobility μ_{eff} vs V_{BS} extracted from I–V for 60 nm strained and control pMOS, at $V_{GT} = -0.4$ V, $V_{BS} = -0.6$, 0, 0.6 V.

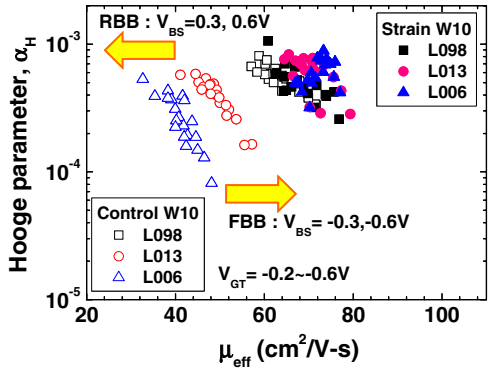

Fig. 12. (Color online) Hooge parameter α_H vs μ_{eff} under FBB ($V_{BS} = -0.3$, -0.6 V) and RBB ($V_{BS} = 0.3$, 0.6 V). FBB can increase μ_{eff} and reduce α_H.

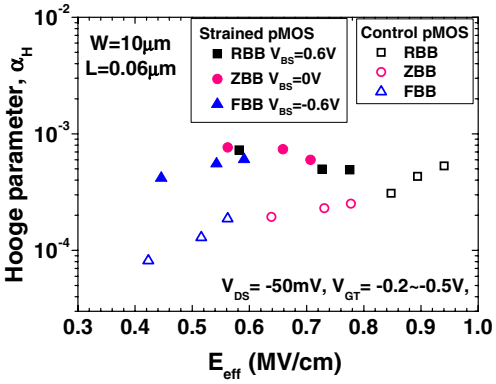

Fig. 13. (Color online) The α_H vs E_{eff} for strained and control devices with $L_g = 0.06$ μm, under dynamic body biases FBB ($V_{BS} = -0.6$ V), ZBB, and RBB ($V_{BS} = 0.6$ V).

increase of α_H with L_g scaling in strained devices but a decrease in control devices. It suggests the local strain will increase α_H and makes LFN worse. The larger α_H in the strained pMOSFET, assuming negligible difference in L_{eff} from e-SiGe suggests that mobility fluctuation becomes worse potentially from accelerated phonon scattering in the strained lattice.[19)]

Figure 11 indicates that α_H and μ_{eff} of control pMOSFET are very sensitive to V_{BS} but those of strained pMOSFET show a weak dependence. Note that FBB can effectively increase μ_{eff} and reduce α_H for control pMOSFET and contribute much lower $S_{ID}/I_D{}^2$. The critical dependence of α_H on μ_{eff} shown in Fig. 12 can facilitate an understanding of the mechanism responsible for dynamic body biases effect on LFN. FBB can help increase μ_{eff} under a specified V_{GT} due to smaller normal field (E_{eff}) resulted from reduced body depletion charge. The increase of μ_{eff} in this way can achieve lower α_H and then realize lower LFN. On the other hand, the μ_{eff} enhancement from the uni-axial strain is accompanied with larger α_H and leads to the penalty of worse LFN.

According to eq. (3), the effective ways to suppressing LFN (flicker noise) can be classified as the increase of device dimensions (W, L_{eff}), the increase of V_{GT}, and the reduction of α_H. Figure 13 illustrates α_H versus E_{eff} for strained and control pMOSFET ($L_g = 60$ nm) in which E_{eff} is varied by changing V_{GT} from -0.2 to -0.5 V, under FBB, ZBB, and RBB. For control pMOSFET, the α_H increases with E_{eff} under all biasing conditions. As for strained pMOSFET, the α_H is higher than that of control pMOS and shows a weak dependence on E_{eff} under various body biases (FBB, ZBB, and RBB). Note that the Hooge parameter α_H responsible for LFN is determined by mobility fluctuation instead of mobility itself. The statement can be understood by eqs. (5)–(8).[20)] The remarkable difference in the E_{eff} dependence of α_H between the strained and control pMOSFET suggests different mechanisms dominant in mobility fluctuation. For control pMOSFET, the strong E_{eff} dependence of α_H suggests that the mobility fluctuation is dominated by the component of surface roughness scattering, i.e., the third term of eq. (8). It can be understood that the larger E_{eff} tends to drive the inversion carriers closer to the gate oxide/channel interface and make surface roughness worse. This increase of surface roughness can enhance mobility fluctuation and reflect its effect on α_H.[20)] However, for strained pMOSFET, the weak E_{eff} dependence of α_H suggests that the mobility fluctuation is dominated by the component of phonon scattering, i.e., the first term of eq. (8). The mechanism proposed for control pMOSFET cannot be applied to strained pMOS:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_i} + \frac{1}{\mu_{sr}}, \tag{5}$$

$$\Delta\left(\frac{1}{\mu_{eff}}\right) = \Delta\left(\frac{1}{\mu_{ph}} + \frac{1}{\mu_i} + \frac{1}{\mu_{sr}}\right), \tag{6}$$

where

$$\Delta\left(\frac{1}{\mu_{eff}}\right) = \left(\frac{-1}{\mu_{eff}^2}\right)\Delta\mu_{eff},$$

$$\Delta\left(\frac{1}{\mu_{ph}} + \frac{1}{\mu_i} + \frac{1}{\mu_{sr}}\right) = \frac{-\Delta\mu_{ph}}{\mu_{ph}^2} + \frac{-\Delta\mu_i}{\mu_i^2} + \frac{-\Delta\mu_{sr}}{\mu_{sr}^2}$$

$$\therefore \frac{\Delta\mu_{eff}}{\mu_{eff}^2} = \frac{\Delta\mu_{ph}}{\mu_{ph}^2} + \frac{\Delta\mu_i}{\mu_i^2} + \frac{\Delta\mu_{sr}}{\mu_{sr}^2}. \tag{7}$$

According to the original definition, α_H, $\alpha_{H,ph}$, $\alpha_{H,i}$, and $\alpha_{H,sr}$ are proportional to $\Delta\mu_{eff}$, $\Delta\mu_{ph}$, $\Delta\mu_i$ and $\Delta\mu_{eff}$, respectively, as

$$\alpha_H = \left(\frac{\mu_{eff}}{\mu_{ph}}\right)^2 \alpha_{H,ph} + \left(\frac{\mu_{eff}}{\mu_i}\right)^2 \alpha_{H,i} + \left(\frac{\mu_{eff}}{\mu_{sr}}\right)^2 \alpha_{H,sr}. \tag{8}$$

The different body biases dependence of α_H between strained and control pMOSFET leads to apparently smaller $\Delta\alpha_{H(S,C)}$ $(= \alpha_{H(Strain)} - \alpha_{H(Control)})$, when operating under ZBB and RBB. This interesting result is consistently reflected by the smaller $\Delta S_{ID(S,C)}/I_D{}^2$ under RBB shown in Table I. Considering that mobility fluctuation is the dominant mechanism responsible for LFN in pMOSFET, the body biases dependence of $\Delta S_{ID(S,C)}/I_D{}^2$ and $\Delta\alpha_{H(S,C)}$ can be explained as follows. For strained pMOSFET, the mobility fluctuation is dominated by accelerated phonon scattering, which is nearly independent of E_{eff} and leads to the weak body biases dependence of α_H. On the other hand, for the control pMOSFET, the mobility fluctuation is primarily governed by surface roughness scattering, which definitely increases with increasing E_{eff} and then results in significant body biases effect on α_H. The mentioned argument can consistently explain the strain effect on LFN and its body bias dependence. The interesting observation suggests that the difference of interface property and scattering process near the channel surface can make the mobility fluctuation different between the strained and control pMOSFET.

5. Conclusions

The uni-axial compressive strain can realize multiple advantages in nanoscale pMOSFETs, such as 65–80% boost of μ_{eff}, I_{DS}, and G_m in linear and saturation regions and 15–20% lower J_g under strong inversion. The remarkable increase in G_m and I_{DS} can boost gate speed and RF/analog circuit performance in terms of f_T and f_{max}. However, this local strain leads to worse LFN with more than 80% higher $S_{ID}/I_D{}^2$ in 60 nm devices. The number fluctuation model widely used for nMOSFETs is no longer valid and cannot explain the local strain as well as scaling effects on LFN measured from pMOSFETs. Mobility fluctuation model can predict the novel LFN characteristics in the dependence on local strain, geometry scaling, and bias conditions. The increase of Hooge parameter α_H due to local strain is identified as the major factor responsible for worse LFN in strained pMOSFET. FBB can increase μ_{eff}, reduce α_H, and improve LFN, all contributed from the reduced E_{eff}. Unfortunately, the dynamic body biases effect is degraded in strained pMOSFET in nanoscale and cannot make significant contribution in LFN. On the other hand, RBB degrades μ_{eff} and makes LFN worse for both control and strained pMOSFET; however their difference in LFN performance becomes smaller, particularly under increasing E_{eff}, because the strained pMOSFET is less sensitive to body bias. The strain engineering for mobility enhancement is useful in high speed digital design but will introduce an adverse impact on analog and RF circuits. For control pMOSFET, FBB is proven as an effective solution for improving μ_{eff} and speed (f_T and f_{max}) as well as LFN ($S_{ID}/I_D{}^2$, α_H), without resort to strain engineering.

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