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Fracture prediction of dissimilar thin film materials in Cu/low-k packaging

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Abstract For current semiconductor technology, interfacial crack in stacked thin films of Cu/low-k damascene integration is a critical reliability issue that needs to be urgently resolved. In addition to the measurement of 4-point bending test, how to precisely estimate the adhesion energy between dissimilar films through simulation, based on fracture mechanics is important while designing robust interconnect structures as well as developing next-generation low-k materials. Distinct from the former studies, this research proposes a novel tie-release crack prediction technique based on finite element calculations in order to consider the stress-induced impacts on the thermo-mechanical reliability of the microelectronic package with a low-k chip during the different cracking length of film interfaces. To ensure the correctness and feasibility of the presented technique, a plastic ball array (PBGA) package with stacked Cu/low-k interconnects is implemented as test vehicle to validate actual testing data of experiments and evaluate the variation of interfacial cracking energy while silicon chip becomes thinner. Through the combination of J-integral approach with the technique of global–local sub-modeling, all the predicted results for the forgoing referred cases reveal a good agreement with the physical behaviors of devices. Therefore, it can be concluded that the proposed methodology is highly reliable in estimating the occurrence opportunities of interfacial crack.

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1 Introduction

Managing inner mechanical stress and strain is crucial to ensure elevated yield and high reliability in advanced back-end-of-line (BEOL) of Cu/low-k technology. One of the most urgent failure modes that needs to be improved is the occurrence of interfacial crack or associated delaminated interfaces at multi-layers Cu/low-k interconnects while the external loading conditions, such as the condition of dicing by sawing blades and the wire bonding impact during the packaging processes, are introduced [1]. The incident of metal peel off appears when the ball is lifted and part of the interconnect structure is torn from the chip device [2]. In investigating the thermo-mechanical reliability of the above-mentioned fractured issue, several interfacial damage models with regard to the FE analysis, which possess the capability of crack location prediction and cracking energy estimation, are continually developed to improve as well as to optimize the design of Cu/low-k interconnect structure [2, 3]. Mercado et al. [4] indicated the regions of stacked low-k films in flip chip packaging most prone to fracture by means of a comparison with the critical magnitude of interface stress. Similar work in the fractured investigation of whole backend wafer processes with the essential material system of Cu/SiLK is implemented [5]. The interfacial strength between dissimilar materials in the mentioned approach would be over-estimated as a result of the assumption of ideal adhesion. In addition, in view of the proviso of having initial defects or cracks, the key fracture index, so-called energy release rate (G), calculated by J-integral approach [4, 6, 7], virtual crack closure

technique (VCCT) [8, 9], and stress intensity factors [10], is widely used to assess the possibility of fractured occurrence of advanced packaging with a low-k silicon chip in contrast with the critical crack driving force (Gc). Alternatively, cohesive zone model (CZM) [11, 12], which considers the nucleation and evolution of the interfacial crack into account, is utilized to predict the fracture/deformation phenomenon of six stacked vertical Cu/low-k interconnect structure below the bond pads. However, that the obstacle of numerical analysis to simulate the brittle interface behavior is difficult to eliminate as a result of snap-back behavior [12]. Furthermore, a method of multi-level sub-modeling is extensively introduced into the FE simulation of low-k package as a result of a drastic difference of structural dimension between low-k stacked films and packaging components [4, 6, 10–13]. To resolve the above-mentioned difficulty in FE modeling, the concept of equivalent material properties can be used in stacked low-k films [13]. However, the accuracy of simulated results in the foregoing literatures regarding the validation of sub-modeling technique has little interpretation while the effect resulted from the neglect of delicate constituent in global and lower-order models becomes critical. Moreover, the sustained effects of the accumulated strain and deformation within a prescribed damage model during a whole loading process have not been duly considered in simulation-based prediction, especially the ones dealing with the complicated structures of novel electronic devices. For this reason, the research presents a tie-release prediction technique combined with the global–local FE technique to estimate the cracking energy of dissimilar Cu/low-k interconnects in advanced packaging structure. In addition, through the calculation of J-integral approach and the verification of 4-PBT, the proposed methodology is promising to the prediction of interfacial fracture in various devices.

2 Interfacial fracture mechanics methodology

An important expression for calculating the energy release rate is known as the J-integral [14, 15]. This research adopts the approach integrated with tie-release prediction technique to assess the possibility of crack extension. The detailed description is in the following section.

2.1 J-integral approach

For the purpose of determining the uppermost safe working loading for a given defect or a prescribed crack, J-integral concept (or G parameter), developed by Rice [15], is an excellent approach to evaluate the fracture toughness and defined as (referred to Fig. 1):

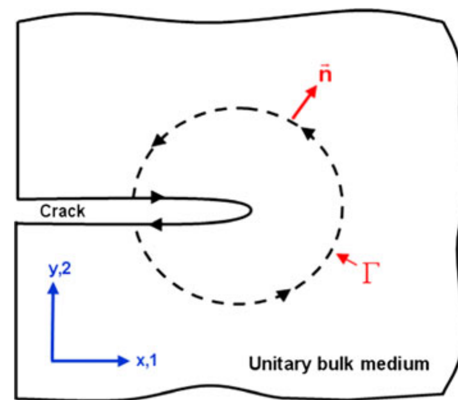

Fig. 1 Line J-integral around a crack in two-dimensions

$$J = \int_{\Gamma} \left(W dy - T_i \frac{\partial u_i}{\partial x} ds \right) \quad (1)$$

$$W = W(x, y) = \int_{0}^{\varepsilon} \sigma_{ij} d\varepsilon_{ij} \quad (2)$$

where (x, y) is the coordinated system whose x-axis exists parallel to the fracture surface. Γ denotes an arbitrary curve surrounding the crack tip in the x–y plane, W is the strain energy density per unit volume, ds is a small element of the contour arc length on Γ, T_i is the traction vector with regard to stress tensor by $T_i = \sigma_{ij} n_j$, u_i is the displacement vector, and n_j is the outward normal on Γ. From the viewpoint of fracture mechanics amount of the total potential energy decreased is fully converted to the increment of crack advance under the assumption of static condition and no energy is lost through heat dissipation. The crack growth initiates at a certain critical value Jc of J.

2.2 Path contour selection of J-integral in interfacial fracture issues

Rice has demonstrated that J-integral is independent of the integration contour [15]. However, this path independence is lost for interfacial crack problems because of the discontinuity of stress/strain on the interface of adjacent materials. In order to resolve this urgent issue, Suo and Shi [16, 17] theoretically found that a rectangular contour is apt for the J-integral calculation in interfacial crack. As shown in Fig. 2, their work also indicated that a stable J-value can be obtained when the parameter $b \to 0$ and the ratio of $b/a \to 0$. On the other hand, Xu et al. [18] and our previous work [7] discussed the feasibility of a rectangular path adopted in the FE estimation of crack/delamination advance for the package and IC devices as well. Consequently, the path contour suggestion of J-integral with a rectangular form is performed in this investigation to

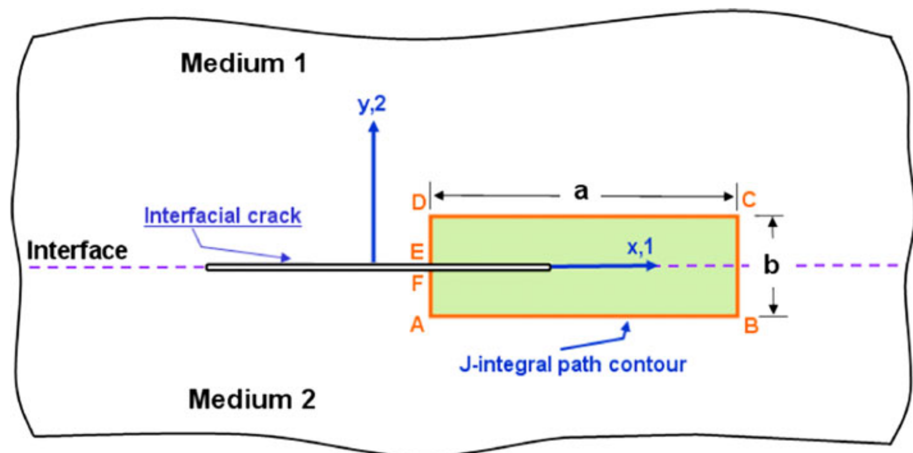

Fig. 2 Nomenclature and coordinates for terms used in the interfacial crack of J-integral calculation with a rectangular path contour

consider the fracture prediction by means of the tie-release technique combined with the global–local FE approach in Cu/low-k packaging.

2.3 Tie-release prediction technique

As explained from the foregoing observations, the damage models with an assumed crack length or defect have been widely adopted but only responded to the stress distribution at that moment instead of considering the effect of whole stress history on the physical behavior of the crack advancement. For this reason, a node tie-release crack prediction technique integrated with a nonlinear FE analysis is proposed in this research to further estimate the thermo-mechanical reliability of electronic devices. The procedures of this presented prediction method are described in detail as follows. Firstly, the most vulnerable location, examined in testing experiments, such as the defective interface of dissimilar materials in a device is bonded in a node-tied manner. For the purpose of obtaining worthy results on stress/strain and cracking energy estimations from the iterative calculations of FE analysis on interface delamination, it should be noted that the interface needs to be associated with a finer FE mesh. Subsequently, under the conditions of an applied load and a well-defined operation environment in the FE analysis, the growth of the fracture surfaces behind the crack front is expected to occur by gradually releasing the tied nodes in accordance with the failure criterion of materials when this mentioned FE analysis is continuously solved following the last simulated results. It should be noted that the nonlinear mechanical responses of the structure under analysis during the overall loading process are involved and accumulated by using this prediction technique. Finally, the termination of the crack extension within the device structure would be achieved when a converged result of the FE analysis simulation is obtained. In other words, the mechanical behavior of whole interfacial cracking process for dissimilar materials could be observed and analyzed at the moment.

3 Simulation-based fracture growth analyses

3.1 Procedures of finite element simulation

When using the presented methodology integrated with the failure criteria of the interface in dissimilar materials such as the critical interfacial toughness of an energy-based J-integral value and the stress failure criterion regarding a concerned bonding interface, the nodes at the adhesive interface of the critical locations within an analytic structure can be tied and released to simulate the occurrence of crack continuously growing during a whole loading process. Prior to discuss the feasibility of node tied or released approach in the simulation of crack growth, the J-integral approach used to predict the magnitude of interfacial cracking energy is necessary to be assured. In this research, a PBGA package with a low-k chip is implemented as a testing vehicle to analyze the fractured behavior of dicing induced damage. Due to that a lower percentage of copper trace distributed over the bottom portion of low-k interconnects leads into a weaker mechanical strength, a 3 μm length of pre-crack is consequently embedded in the interface between the bottoms of low-k films (M1 layer) and the inter level dielectric (ILD) close to the die edge. A sketch for the illustration of FE modeling is shown in Fig. 3. A large silicon chip scale with 100 mm^2 and 0.7 mm thick is concerned. The chip is bonded to the bismaleimide triazine (BT) substrate of 1.2 mm thickness through about 3 μm thickness of die-attach epoxy. Moreover, several hundred nanometers thick of stacked low-k films is inserted between the molding compound and the silicon chip. For the purpose of simplifying the J-integral calculation in the complicated Cu/low-k packaging

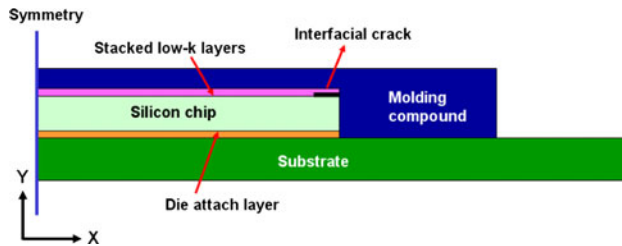

Fig. 3 Schematic of PBGA with stacked Cu/low-k interconnects before mounting on board

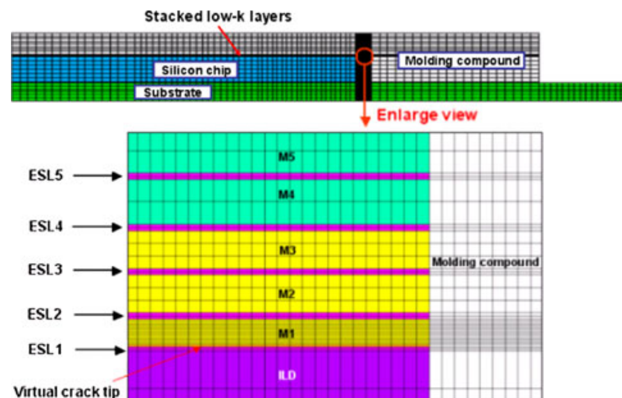

Fig. 4 Half symmetry FE model of PBGA with stacked Cu/low-k interconnects

Table 1 The list of the material properties used in FE analysis

Materials	E (GPa)	CTE (ppm/°C)	Poisson ratio
Silicon chip	160	3	0.28
Inter level dielectric (ILD)	58.8	1.5	0.3
Etch stop layer (ESL)	58.8	1.5	0.3
Inter metal dielectric (IMD)	10	23	0.3
USG	80	1.5	0.3
SiN	130	10	0.3
SiO_2	80	10	0.28
Molding compound	24	20	0.3
BT substrate	$26 - x$, $26 - y$, $11 - z$	$15.7 - x$, $15.7 - y$, $57 - z$	$0.36 - xy$, $0.36 - yz$, $0.11 - xz$
Die-attach epoxy	6	100	0.35

structure, a 2-D FE analysis integrated with a half symmetry constraints in the displacements is used in the study. Figure 4 shows the enlarged view of local region of interconnects including the etch stop layers (ESLs) and the low-k layers (Mx). Table 1 lists the detailed material properties utilize in FE analysis. The procedure of cooling down for molding compound component, whose temperature range is from 180 °C to room temperature, is regarded as the external loading to examine the packaging impact on the interfacial crack of stacked low-k films. The obtained value of predicted cracking energy for ESL1/M1 interface is 1.87 J/m^2. The foregoing result can be further reconfirmed by comparing the measured data and the predicted FE results of 4-PBTs.

3.2 Validation of numerical results using 4-PBTs

In order to verify the accuracy of J-value prediction, the interfacial toughness measured by using 4-PBTs, was selected for comparsion with the estimation of FE analysis. As shown in Fig. 5, that the geometrical framework of 4-PBT to examine the adhesion of TiN/Al film interface was considered in the research as a result of the surface condition of low-k film and its interfacial toughness affected by the fabricated process is apparent. In the above-mentioned apparatus, the distances between inner the supports (2D) and between the outer loading line and the inner hold (L) were 16 and 3 mm, respectively. In addition, both the thickness of glass wafer and the silicon wafer, equal to 1 mm, were identical. The length and width of testing specimen are 25 mm (L1) and 2 mm (B), respectively. The detailed thickness of thin films are also shown in Fig. 6a. Based on the same skeleton in geometry, the FE model on accordance with the assumption of plane strain was constructed (Fig. 6b). Table 2 shows the mechanical properties of materials used in the simulation. It should be noted that the critical load P (12.7 N) applied in FE analysis was identical to the corresponding experiments [19]. The averaged value of 3.672 J/m^2 predicted for TiN/Al interface was obtained and shown in Fig. 9. As compared with the corresponding measured data 3.68 J/m^2 and the conclusion of provided by Wang [19], the simulated results exhibit an excellent agreement with the experiment event.

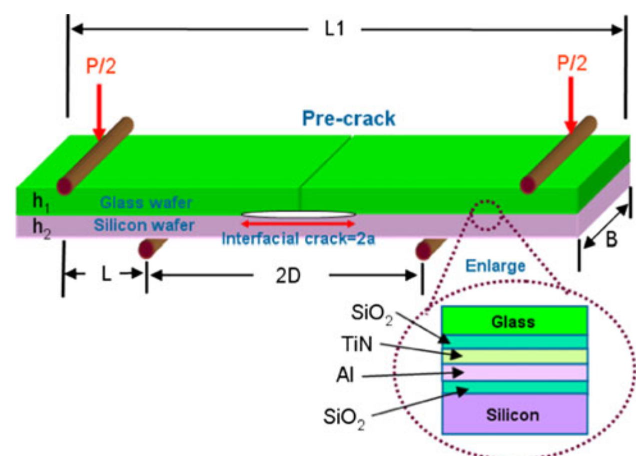

Fig. 5 Schematic picture for the loading conditions and dimensions of 4-PBTs

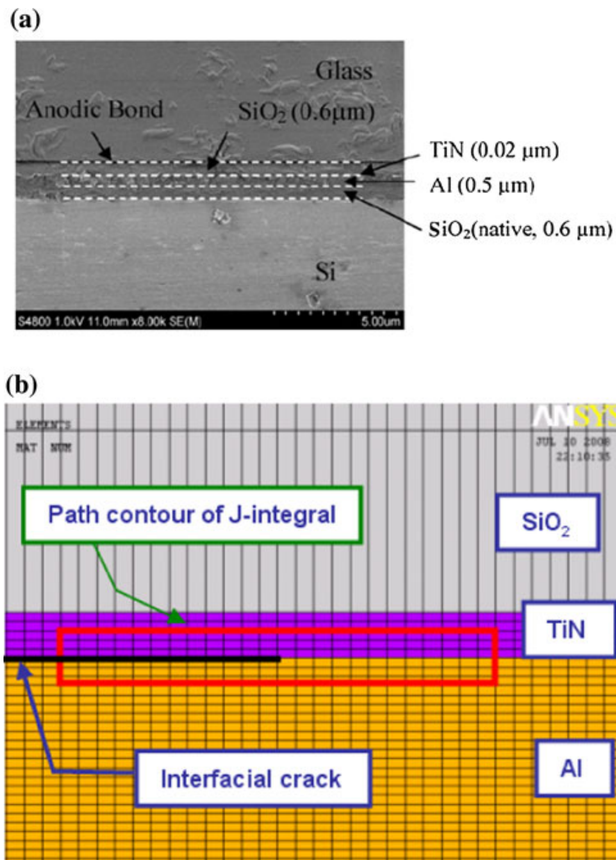

Fig. 6 The cross-section of 4-PBT specimen: **a** sandwiched thin film structure, **b** the arrangement of FE analysis for an interfacial crack of TiN/Al interface during testing [19]

Table 2 Data of material properties adopted in the FE performance of 4-PBTs

Material	Young's modulus (GPa)	Poisson's ratio
Silicon wafer	169.5	0.23
Glass wafer	60	0.2
SiO_2	80	0.28
TiN	80.6	0.208
Al	70	0.33

Therefore, it was successfully validated the prediction methodology of interfacial crack energy. Subsequently, on the basis of the foregoing prerequisite, the discussion and analysis of tie-release prediction technique is regarded to be meaningful and valuable as well.

4 Results and discussion

As the requirements for electronic equipment including portable information terminals must be reduced in size and in thickness, the thin-film type of silicon chip made using ground or etch methods has been proposed for such shrinkage in the foregoing dimensions. In addition, low-k materials on the active surface of the IC chip have an intrinsically lower elastic modulus and poor adhesion compared with other dielectric materials. Consequently, there is a high possibility that an interfacial crack may occur under the combinations of the aforementioned thin chip with Cu/low-k interconnects. Hence, prior to discussing the tie-release prediction technique, the thickness of the silicon chip and the crack tip opening displacement (CTOD) belong to the interface of dissimilar materials are supposed to be the major geometry parameter concerns for the crack growth.

4.1 Impacts of silicon chip thickness on the crack growth of Cu/low-k films interfaces

It was found that the silicon die thickness has a significant impact on the J-integral value (Fig. 7) As referred to in Figs. 3 and 4 when a larger rigidity was provided though a thicker die thickness (above 600 μm), and the thickness of the molding compound was fixed at 600 μm, then a larger J-integral value is expected as a result of the coefficients of thermal expansion (CTE) of M1 layer being dominant at the moment. This provides a larger CTE mismatch between the M1 and ESL1 layers. When the flexibility of the silicon die increases as the die thickness lowers, and the materials (M1 and die-attach layer) at both sides of the die have larger CTEs than the die, then the larger thermal stress being induced from the foregoing geometrical combination (thicker die) is reduced. In other words, the J-integral value reduces as the die thickness is decreased. However, when the silicon die thickness, which continues to provide a larger flexibility, is smaller than the die attach thickness (approximately 25 μm) as well as the dominant material property of the die attach layer with a high CTE of

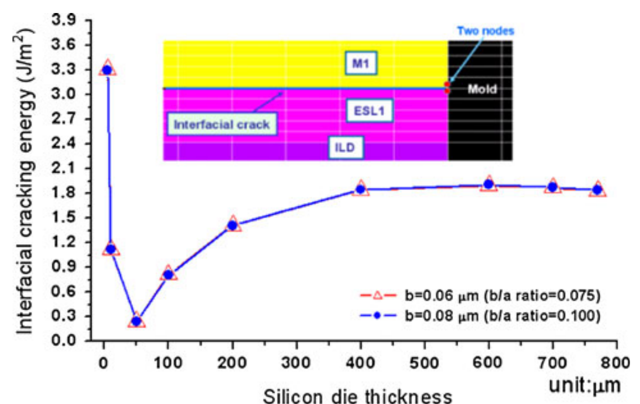

Fig. 7 The reduction of the silicon chip thickness affecting the variance of the J-integral value

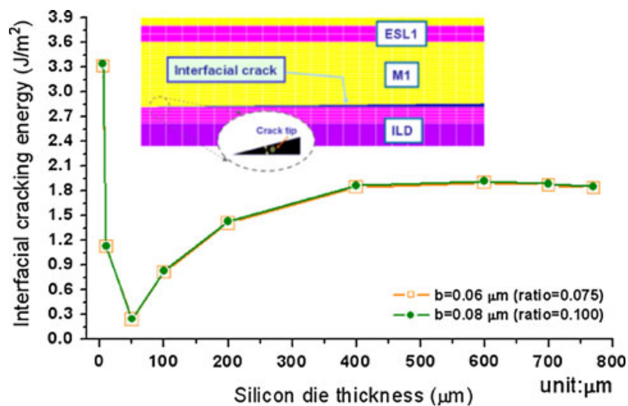

Fig. 8 Interfacial cracking energy predictions with a fixed crack tip opening displacement (CTOD) while changes in the silicon chip thickness

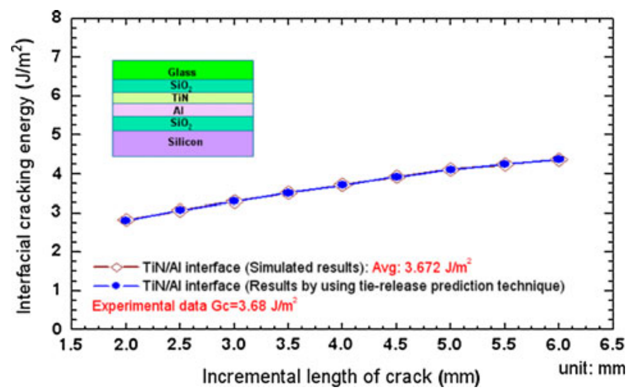

Fig. 9 Predicted results of TiN/Al adhesion energy by means of J-integral calculation with a rectangular path contour in a 4-PBT frame

100 ppm/°C, then the larger thermal stress driving the crack growth is generated by the larger CTE mismatch between the ESL1 layer and the die attach layer. Moreover, because the CTE mismatch between the die attach layer and the ESL1 layer (1.5 ppm/°C) is larger than the CTE mismatch between the M1 layer (23 ppm/°C) and the ESL1 layer, a larger J-integral value was obtained. It should be noted that the mark "ratio" in Figs. 7 and 8 means the dimensionless ratio of b/a when J-value is calculated (refer to Fig. 2). On the other hand, when a fractured condition with a larger CTOD (about 0.3 μm) as shown in Fig. 8 was considered, the analytic results indicated that the parameter of CTOD with much small size did not have a significant effect on the cracking energy. The foregoing consequence is believed to be resulted from the assumption of linear-elastic analysis or the existence of a slight magnitude of CTOD.

4.2 Application of tie-release technique in 4-PBTs

According the 4-PBTs apparatus described in reference [19], the experimental data of TiN/Al interface is predicted and verified by the simulations with difference pre-crack lengths, as shown in Fig. 9. The researches utilize another method by tying the nodes along above-mentioned interface and gradually release the nodes close to the latest crack tip to consider the effect of applied stress/strain history on the crack advance. For the FEA model of 4-PBTs, initially all the nodes of TiN/Al interface are tied. Next, apply the external loading to obtain the simulated result of the first step. Then, release certain nodes behind crack tip to suppose the crack continuing growth, and then re-simulate the latest model based on the revealed state of the former result. By means of the above-mentioned interpretation, the effect resulted from crack growth could be approximately obtained. Figure 10 shows the enlarged view of simulated condition while a 2.5 mm crack length is reached. As compared with the approach of embedding a pre-crack, the results are almost the same (Fig. 9). It is also to justify that the tie-release technique is feasible to investigate the mechanical behavior of interfacial fracture.

4.3 Interfacial fracture of stacked low-k packaging

The procedure for this crack prediction technique applied to the low-k PBGA package is explained as follows. First, find the possible locations to form the interfacial cracks such as the interface of the M1/ESL1 layers within the PBGA structure. Next, construct the FEA model of the PBGA package. To combine the use of calculating a stable J-integral value for the crack of dissimilar materials, the density of the finite element meshes around the crack tip must meet the abovementioned requirement. In addition, it has the advantage of observing a growing crack by releasing the proper amount of nodes belonging to the fracture surfaces. Next, tie the nodes which have identical positions along the fracture interface of the M1/ESL1 layers, as shown in Fig. 11. It should be noted that a small distance along this interface of the M1/ESL1 layers to the boundary of the molding compound does not tie nodes in order to suppose that a micro defect exists at the foregoing location. Moreover, the contact pair elements are spread on the fracture surfaces to avoid incorrect estimation resulting from simulated prediction as caused by the penetration behavior of the fracture surfaces when an interfacial crack continues to extend. Then solve the 2D FEA.

In accordance with the earlier reports [20, 21], the interfacial adhesion of the Cu/low-k film during various fabrication processes such as deposited film, CMP, and so on is at the range of 3–5 J/m^2. Therefore, a smaller energy release rate of 3 J/m^2 was regarded as a serious fracture criterion of the interfacial crack occurring on the interface of the M1/ESL1 layers. Meanwhile, a crack length starting from 1.5 μm, through 2, 3, 5, 8, 12, and 17 μm to 21.5 μm simulated by the present crack prediction technique was

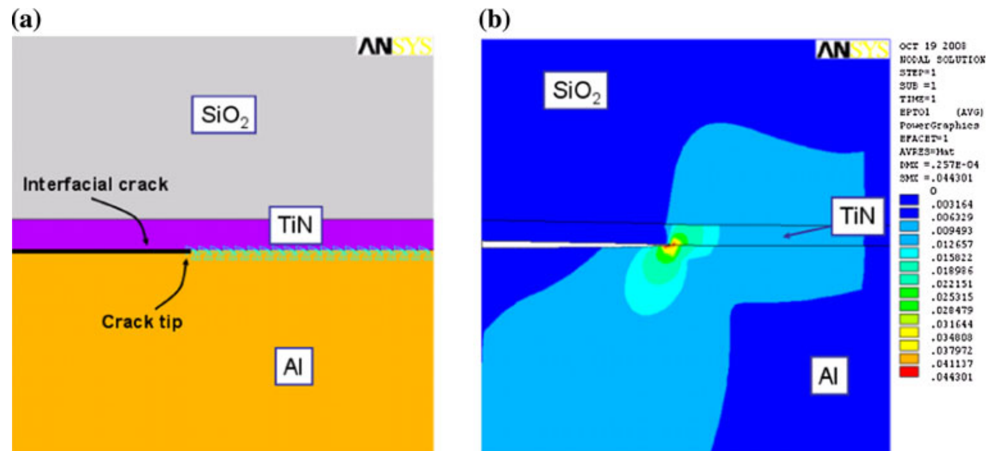

Fig. 10 Enlarged view of the FEA model combined with the tie-release technique for the 4-PBTs when the interfacial crack is equal to 2.5 mm: **a** nodes at the critical interface are tied before incremental loading, **b** the contour of the 1st principal total strain close to the region of crack tip along TiN/Al interface

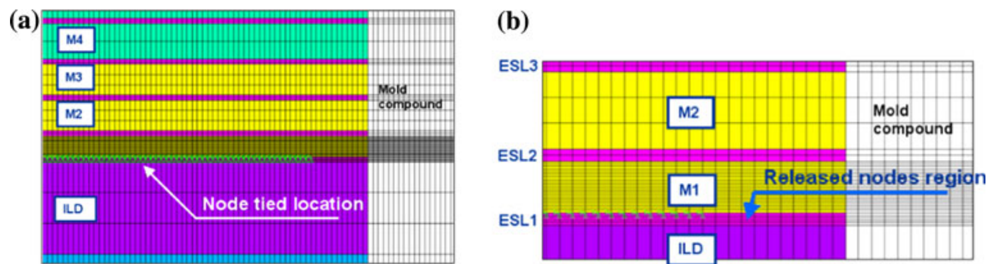

Fig. 11 Enlarged view of the FEA model for the PBGA package with Cu/low-k interconnects: **a** nodes at the critical interface are tied before loading, **b** nodes are gradually released to visualize the behavior of interfacial crack growth after loading

selected to calculate each J-integral value corresponding to the abovementioned size of the crack growth. The effect of the stress/strain history during the whole loading progress in this FEA was also considered (See Fig. 11b). Finally, when a crack extension of 21.5 μm was achieved, the FEA was ended to obtain the trend of the J-integral value variation with an increase in the crack length. Besides the proposed tie-release prediction technique, other procedures of the FEA for the low-k PBGA structure were all similar with the descriptions in the foregoing sections. When a temperature load from 180 °C to the room temperature of 25 °C was applied, a comparison between the FEAs using and not using the contact pair elements to prevent the penetration of fracture surface behind the crack tip was also performed. As shown in Fig. 12, the results reveal that a higher J-integral value follows a larger crack length. In addition, the rate of raising the crack driving force tends toward a stable condition when it has a larger interfacial crack length. According to the critical energy release rate G_c, as well as the criterion of crack growth determined by experiments such as the 4-point bending test, if a size of the micro defect larger than about 5 μm exists at the interface of the M1/ESL layers, a crack extension along this interface is more likely to occur when the crack energy exceeds the interfacial toughness of 3 J/m^2. In addition, when this PBGA structure does not provide the energy to this crack anymore, the phenomenon of a drop and a termination in the crack growth is expected to take place after occurence of a certain crack growth. On the other hand, from the viewpoint of physics, because a partial energy in the concerned structure would be consumed by the contact behavior resulting from the fracture surfaces instead of being fully taken as the required energy of the crack advance, the analytic result showed that the propagation of interfacial crack with a contact pair setting between dissimilar materials had a lower J-integral value in all examined crack lengths compared with the conditions without contact settings (See Fig. 14). Therefore, the simulated results greatly meet the physical sense. From the

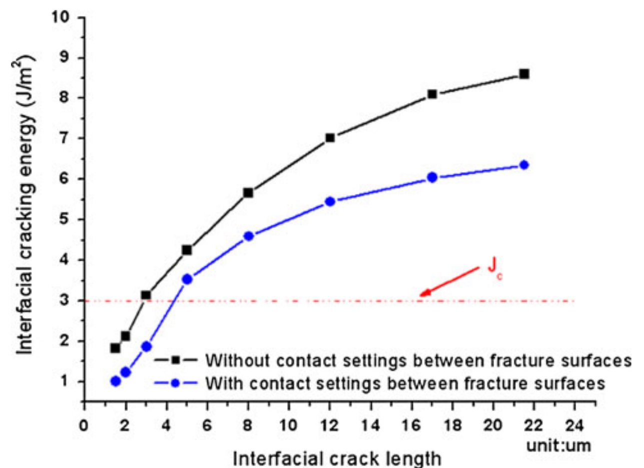

Fig. 12 Variation of crack energy when a crack growth of the urgent Cu/low-k interface is predicted using the tie-release prediction technique

predicted results for the fracture analysis of the PBGA package with Cu/low-k interconnects, the presented tie-release crack prediction technique integrated with an energy-based calculation of a stable J-integral value has been shown to be reliable in this research.

4.4 Utilization of global–local modeling approach combined with node tie-release prediction technique in a low-k packaging structure

Due to the low-k package has the difficulty in the dimensional match of simulation modeling when the reliability issue is urgently concerned at the moment. For the reason, the global–local technique, called specified boundary condition (SBC) method, is integrated with the tie-release technique to resolve the foregoing subject as well as to enhance the applied breadth of present methodology in this research. As shown in the Fig. 13, in order to prevent that the stress/strain fields adjacent to the interested region of interfacial crack occurrence in the global model would have an opportunity to distort the actual mechanical behavior around the crack, the intercepted boundary conditions corresponded to the identical location in the global model, which is applied in the local model, is far away from the crack tip in accordance with the St. Venant's principle. As compared results indicated in the Fig. 14, the global–local modeling technique could have an excellent capability to perform compatibly with the proposed tie-release technique.

5 Conclusions

For the purpose of considering the stress-induced impacts on the thermo-mechanical reliability of electronic interconnects during the cracking growth process of dissimilar materials in such devices of Cu/low-k stacked structures and advanced packaging structures as well, a novel crack prediction technique based on the finite element calculation by means of tied or released nodes is systematically proposed and investigated in this research. Upon using the presented method integrated with the failure criteria of the interface in dissimilar materials such as the critical interfacial toughness of an energy-based J-integral value and the stress failure criterion regarding the concerned bonding interface, the nodes at the adhesive interface of the critical locations within an analytic structure can be tied and released to simulate the occurrence of crack advance during the whole loading process. It also has the advantage of considering the effect of the accumulated stress/strain on the interfacial crack when the nonlinear behaviors of the structure urgently need to be given attention. To validate the reliability of the proposed prediction methodology, both the usual 4PBTs apparatus and an advanced PBGA packaging structure with stacked Cu/low-k interconnects in the fracture issues are implemented as the test vehicles to demonstrate the difference with the traditional prediction techniques. In the foregoing low-k package, the cracking energy and the crack advance or delamination between the Cu/low-k interfaces were successfully predicted. Through a comparison with the interfacial toughness of the bi-material interface, a possibility for the crack extension can be precisely estimated in different crack lengths that grow from a micro defect within the device configuration.

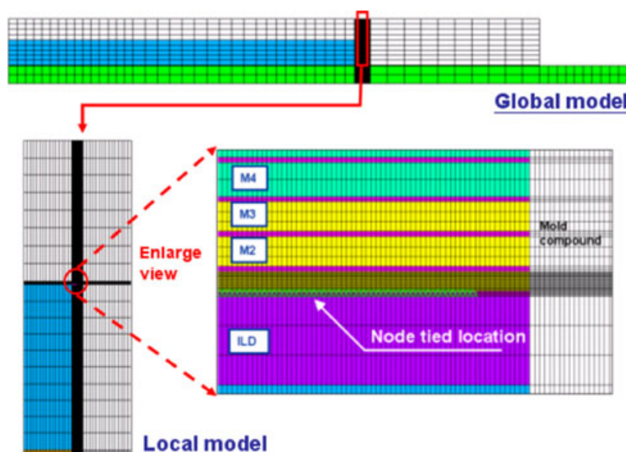

Fig. 13 The SBC approach combined with the tie-release technique utilized in the interfacial fracture prediction of a low-k PBGA package

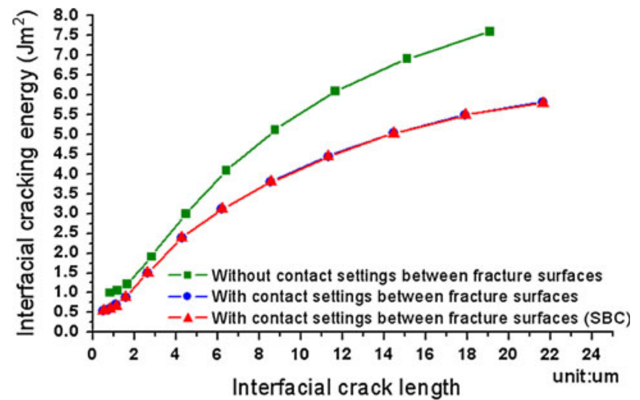

Fig. 14 The curves of cracking energies of low-k film interfaces predicted by means of the SBC approach combined with the tie-release prediction technique

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