[8] J. S. Byun, H. B. Jeon, K. H. Lee, and J. Jang, "Effect of Cl incorporation on the stability of hydrogenated amorphous silicon," *Appl. Phys. Lett.*, vol. 67, pp. 3786–3788, 1995.
[9] W. E. Spear, "The study of transport and related properties of a-Si : H by transient experiments," *J. Non-Cryst. Solids*, vol. 59–60, pp. 1–13, 1983.

Improved Output ESD Protection by Dynamic Gate Floating Design

Hun-Hsien Chang and Ming-Dou Ker

***Abstract*—A dynamic gate floating design is proposed to improve ESD robustness of the CMOS output buffers with small drive capability. By using this novel design, the human-body-model (machine-model) ESD failure threshold of a 2-mA CMOS output buffer has been practically improved from 1 KV (100 V) to greater than 8 KV (1500 V) in a 0.35-μm CMOS process.**

***Index Terms*—ESD, ESD protection, output buffer.**

I. Introduction

Electrostatic discharge (ESD) robustness of CMOS IC's had been found to be seriously degraded by the advanced deep-submicron CMOS technologies [1]–[3]. To improve ESD robustness of the output transistors, the ESD-implant process and the silicide-blocking process had been widely used in the deep-submicron CMOS technologies [3]–[5]. Besides the advanced process modifications to improve ESD robustness of the output buffers, the symmetrical layout structure had been emphasized to realize the large-dimension output transistors by ensuring the uniform turn-on phenomenon along the multiple fingers of the output transistor [6]. To further enhance the uniform turn-on phenomenon among the multiple fingers of the output transistors, a gate coupling design had been reported to achieve uniform ESD power distribution on the large-dimension output transistors [7]–[11]. But in the practical applications, the output buffers in a cell library have different drive capability specifications, for example, 2, 4, 8, $\cdots$, 24 mA, etc. But, the cell layouts of the output buffers with different drive capabilities are still drawn in the same layout style and area for programmable application. To adjust the different output sink (drive) currents of the output buffer, different fingers of the poly gates in the output NMOS (PMOS) are connected to the pre-buffer circuit, while the other unused poly-gate fingers are connected to ground (VDD). Due to the asymmetrical connection on the poly-gate fingers of the output NMOS in the layout, the ESD turn-on phenomenon among the fingers becomes quite different even if the layout is still symmetrical. This generally causes a very low ESD level for the output buffer, even if the output buffer has a total large device area.

Manuscript received December 22, 1997; revised May 4, 1998. The review of this brief was arranged by Editor C.-Y. Lu. This work was supported by the Design Service Division of Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, R.O.C., under Contract C87084.

H.-H. Chang is with Integrated Circuits and Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu 310, Taiwan, R.O.C.
M.-D. Ker is with VLSI Design Division, Computer and Communication Research Laboratories (CCL), Industrial Technology Research Institute (ITRI), Hsinchu 310, Taiwan, R.O.C. (e-mail: mdker@vlsi.ccl.itri.org.tw).

Publisher Item Identifier S 0018-9383(98)06437-5.

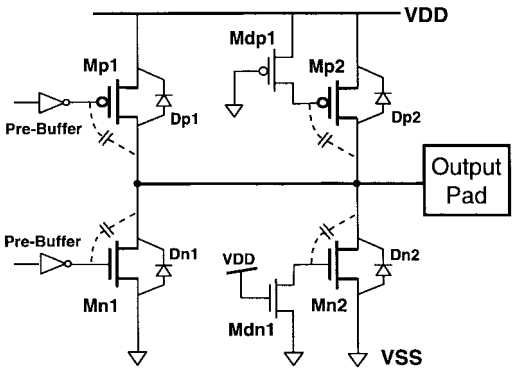

Fig. 1. The output buffer with a small drive capability in a 0.35-μm CMOS process. The gate of the unused Mn2 (Mp2) is connected to VSS (VDD) through a small-dimension Mdn1 (Mdp1) to perform the traditional gate coupling effect for ESD protection.

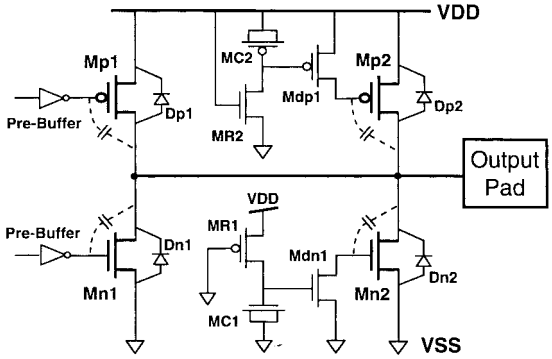

Fig. 2. The dynamic gate floating design to improve ESD level of the output buffers with small drive capability in a 0.35-μm CMOS process.

In this paper, a dynamic gate floating design is proposed to improve ESD level of the output buffers with different drive capabilities in a 0.35-μm CMOS process [12].

II. Output ESD Protection Design

A. Traditional Gate Coupling Design

To enhance the turn-on uniformity of the output buffers, the poly gates of the unused NMOS (PMOS) in the output buffers are connected to VSS (VDD) through a small-dimension NMOS Mdn1 (PMOS Mdp1) [10], as shown in Fig. 1. The Mdn1 (Mdp1) cooperated with the parasitic drain-to-gate capacitance in the Mn2 (Mp2) performs the gate coupling effect to turn on the Mn2 (Mp2) during the ESD stress [9]–[11]. In the normal operating conditions, the gate of Mp2 (Mn2) is connected to VDD (VSS) through the turned-on Mdp1 (Mdn1) to keep the Mp2 (Mn2) off. The output drive (sink) current is provided by the Mp1 (Mn1). For an output buffer with a smaller drive capability, such as only 2mA, the device dimension of the Mn1 (Mp1) is much smaller than that of the Mn2 (Mp2). In a 0.35-μm CMOS cell library, a 2-mA output buffer has the device dimension (W/L) of 30/0.5 (μm/μm) for both the Mn1 and Mp1. But, in the cell layout of the 2-mA output buffer, it also has the device dimension of 450/0.5 (690/0.5) for the Mn2 (Mp2). The gate to drain contact distance in the Mn2, Mp2, Mn1, and Mp1

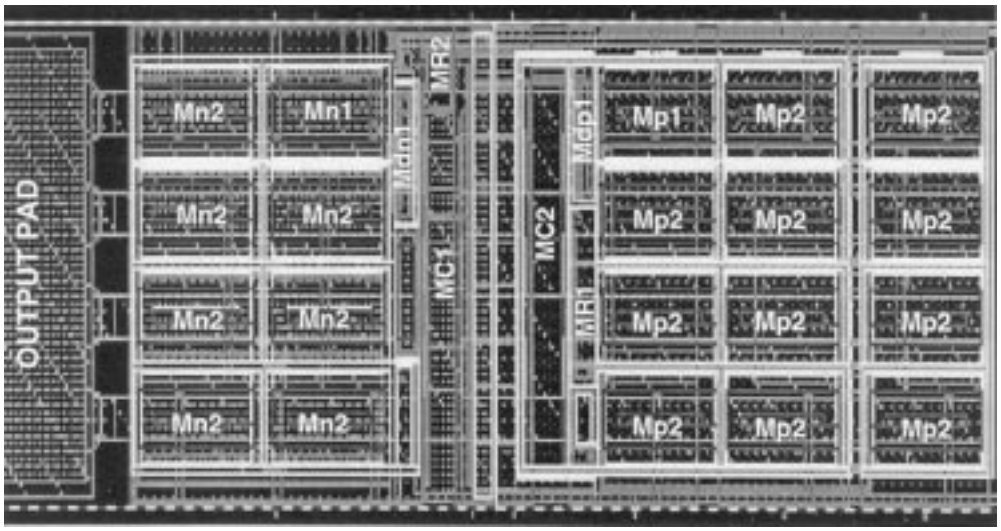

Fig. 3. The layout example of the 2-mA output buffer in the 0.35-μm CMOS process with the dynamic gate floating design.

is the same of 2.6 μm in all output buffers. The device dimensions of the Mdn1 and Mdp1 are both designed as 20/0.35 (μm/μm).

There are four modes of ESD test combinations from the output pin to the VDD or VSS pins [11], [13]. In the ND-mode (PS-mode) ESD stress, the output PMOS (NMOS) is reverse biased and broken down by the ESD voltage. But, in the NS-mode (PD-mode) ESD stress, the parasitic drain-to-bulk diode in the NMOS (PMOS) is forward biased to bypass the ESD current. Due to the low operating voltage, the diode in the forward biased condition can sustain much high ESD stress. But, the NMOS or PMOS in the breakdown condition with high snapback voltage are easily damaged by the ESD energy. Thus, the worst cases of the ESD stresses on an output buffer are the ND- and PS-mode ESD events.

The output buffers with different drive capability specifications are tested in the human-body-model (HBM) ESD event by the *Zapmaster* ESD tester. Both the ESD-implant process and the silicide-blocking process are used in all output buffers. The PS-mode and ND-mode ESD test results are summarized in Table I. Due to the different connections on the gates of the output Mn1 and the unused Mn2, the PS-mode ESD level of the 2-mA output buffer is only 1 KV. But the 8-mA output buffer can sustain the PS-mode ESD voltage of 2 KV. While the drive capability of the output buffer is increased with a larger device dimension on Mn1, the output buffer has a higher ESD level (>2.5 KV). Although the cell layout areas and the total device dimensions (Mn1+Mn2) of these output buffers (2, 4mA, ...) are all the same in the cell library, the ESD level of these output buffers are quite different. Even if using the gate coupling effect with the NMOS Mdn1 (PMOS Mdp1) to help the uniform turn-on between the Mn1 and Mn2 (Mp1 and Mp2), the HBM ESD level of the output buffer with a small Mn1 (Mp1) but a large Mn2 (Mp2) is still below the general industrial ESD specification of 2000 V.

TABLE I
THE HUMAN-BODY-MODEL (HBM) ESD LEVEL OF THE OUTPUT BUFFER PROTECTED BY THE TRADITIONAL GATE COUPLING DESIGN (FIG. 1)

HBM ESD Stress \ Output Buffers	2-mA Buffer	4-mA Buffer	8-mA Buffer	12-mA Buffer	24-mA Buffer
ND-Mode	1.5KV	2KV	2.5KV	> 2.5KV	> 2.5KV
PS-Mode	1.0KV	1.5KV	2.0KV	> 2.5KV	> 2.5KV

B. Dynamic Gate Floating Design

The dynamic gate floating design to improve ESD robustness of an output buffer with small drive capability is shown in Fig. 2. As comparing to the traditional gate coupling output buffer in Fig. 1, two additional MR2 and MC2 (MR1 and MC1) devices are designed to dynamically float the gate of Mp2 (Mn2) during the ND-mode (PS-mode) ESD-stress condition, but the gate of Mp2 (Mn2) is connected to VDD (VSS) in the normal operating condition. The MC1 and MC2 devices are functioned as the capacitors, and the MR1 and MR2 devices are functioned as the resistors. Because the gate of Mn2 (Mp2) is floated in a time period during the PS-mode (ND-mode) ESD transition, the coupled voltage through the drain-to-gate capacitance can be really held on the gate of Mn2 (Mp2) to uniformly turn on the Mn2 (Mp2). Because the Mn2 and Mp2 are fabricated by both the ESD-implant process and the silicide-blocking process in the 0.35-μm CMOS technology, the turned-on Mn2 and Mp2 with large device dimensions can sustain a much higher ESD level.

A practical design example of the 2-mA output buffer has the same device dimensions to those of Fig. 1. The additional MR1 and MR2 have the device dimension (W/L) of 1.7/45 (μm/μm) to perform a high resistance, and the MC1 and MC2 have the device dimension of 65/8 (μm/μm) to perform a high capacitance to realize the dynamic gate floating design. The typical cell layout of the 2-mA output buffer in the 0.35-μm CMOS process is demonstrated in Fig. 3, which occupies a total layout area of 84 $\times$ 326 μm^2 including the bond pad of 80 $\times$ 80 μm^2.

In the PS-mode ESD stress, the positive ESD voltage is applied to the output pad while the VSS is grounded but the VDD is floated. Due to the sharp rising edge of the ESD voltage, the gates of Mn2 and Mn1 are coupled with some positive voltage through the drain-to-gate parasitic capacitance in the Mn2 and Mn1. During the PS-mode ESD stress, the positive ESD voltage on the pad is also diverted into the floated VDD power line through the parasitic diode Dp2 (Dp1) in the Mp2 (Mp1). The drain of MR1 is therefore charged by the ESD voltage on the VDD power line. The gate-grounded PMOS MR1 functions as a resistor to charge the gate of Mdn1. The NMOS MC1 functions as a capacitor to store the gate voltage of Mdn1. Initially, the voltage stored on the capacitor MC1 is zero before the ESD voltage is applied to the output pad. But, the voltage stored on the capacitor MC1 is increased through the MR1 while the VDD power line is charged by the ESD current through the Dp2 and Dp1. The

TABLE II
THE HUMAN-BODY-MODEL (HBM) ESD LEVEL OF THE OUTPUT BUFFER PROTECTED BY THE DYNAMIC GATE FLOATING DESIGN (FIG. 2)

HBM ESD Stress \ Output Buffers	2-mA Buffer	4-mA Buffer	8-mA Buffer	12-mA Buffer	24-mA Buffer
ND-Mode	> 8KV	> 8KV	> 8KV	> 8KV	> 8KV
PS-Mode	> 8KV	> 8KV	> 8KV	> 8KV	> 8KV

TABLE III
THE MACHINE-MODEL (MM) ESD LEVEL OF THE 2-mA OUTPUT BUFFER

MM ESD Stress \ Output Buffers	2-mA Buffer with the Traditional Gate Coupling Design (Fig.1)	2-mA Buffer with Dynamic Gate Floating Design (Fig.2)
ND-Mode	150V	1600V
PS-Mode	100V	1500V

increase speed of the gate voltage on the MC1 is strongly dependent on the RC time constant of the resistor MR1 and the capacitor MC1. With a higher resistance MR1 and a larger capacitance MC1, the coupled voltage through the drain-to-gate capacitance of Mn2 can be held on the gate of Mn2 in a longer time period. Therefore, the Mn2 with a large device dimension can be instantaneously turned on to bypass ESD current from the output pad to VSS.

In the ND-mode ESD stress, the negative ESD voltage is applied to the output pad while the VDD is grounded but the VSS is floated. The negative ESD voltage on the pad is diverted into the floated VSS power line through the parasitic diode Dn2 (Dn1) in the Mn2 (Mn1). The NMOS MR2 with its gate connected to VDD functions as a resistor, whereas the PMOS MC2 functions as a capacitor. The negative ESD voltage on the VSS power line charges the gate of Mdp1 through the MR2. The decrease speed of the gate voltage on the Mdp1 is strongly dependent on the RC time constant of the resistor MR2 and the capacitor MC2. A higher resistance MR2 and a larger capacitance MC2 are therefore designed to keep the Mdp1 off in a longer time, so the gate of Mp2 can be dynamically floated in a longer time period. By using this dynamic gate floating design, the coupled negative voltage through the drain-to-gate capacitance of Mp2 can be held on the gate of Mp2 in a long time period. Therefore, the Mp2 with a large device dimension can be instantaneously turned on to bypass the negative ESD voltage from the output pad to the grounded VDD.

III. EXPERIMENTAL RESULTS

The HBM ESD test results of the output buffers in Fig. 2 with the dynamic gate floating design are listed in Table II. The HBM ND-mode (PS-mode) ESD level of the 2-mA output buffer with the traditional gate coupling design in Fig. 1 is only 1.5 KV (1 KV). But, the HBM ND-mode (PS-mode) ESD level of the 2-mA output buffer with the same device dimensions can be improved greater than 8 KV by using the dynamic gate floating design. In Table II, the dynamic gate floating design is not used in the output buffers with the drive capability greater than 12 mA, because the device dimension of the output Mn1 (Mp1) is greater than that of the Mn2 (Mp2) in such output buffers.

The machine-model (MM) ESD test results of the 2-mA output buffers between the designs in Figs. 1 and 2 are compared in Table III. The 2-mA output buffer with the traditional gate coupling design in Fig. 1 can sustain the MM PS-mode (ND-mode) ESD level of only 100 V (150 V), but the 2-mA output buffer with the dynamic gate floating design in Fig. 2 can pass the MM ESD stress of 1500 V. These ESD test results have practically verified the effectiveness of the dynamic gate floating design to improve ESD robustness of the output buffer with a small-dimension output Mn1 (Mp1) but a large-dimension unused Mn2 (Mp2).

IV. CONCLUSION

A dynamic gate floating design has successfully improved ESD level of the small-driving output buffers. The gates of the unused NMOS/PMOS in the output buffers are dynamically floated during the ESD stress, so the unused NMOS/PMOS with large device dimensions can be instantaneously turned on to bypass the ESD current. By using this dynamic gate floating design, the HBM ND-mode (PS-mode) ESD level of the 2-mA output buffer in a 0.35-μm CMOS process has been significantly improved from 1.5 KV (1 KV) up to greater than 8 KV without increasing the total layout area of the output cell. The MM ND-mode (PS-mode) ESD level of the 2-mA output buffer has been also effectively improved from 150 V (100 V) up to greater than 1600 V (1500 V).

REFERENCES

[1] S. Voldman and V. Gross, "Scaling, optimization and design consideration of electrostatic discharge protection circuits in CMOS technology," in *1993 EOS/ESD Symp. Proc.*, pp. 251–260.
[2] A. Amerasekera and C. Duvvury, "The impact of technology scaling on ESD robustness and protection circuit design," in *1994 EOS/ESD Symp. Proc.*, pp. 237–245.
[3] I. Kurachi, Y. Fukuda, N. Miura, and F. Ichikawa, "Analysis of soft breakdown failure with ESD on output buffer nMOSFET's and its improvement," *IEEE Trans. Ind. Applicat.*, vol. 30, pp. 358–364, 1994.
[4] S. Daniel and G. Krieger, "Process and design optimization for advanced CMOS I/O ESD protection devices," in *1990 EOS/ESD Symp. Proc.*, pp. 206–213.
[5] S. G. Beebe, "Methodology for layout design and optimization of ESD protection transistors," in *1996 EOS/ESD Symp. Proc.*, pp. 265–275.
[6] T. L. Polgreen and A. Chatterjee, "Improving the ESD failure threshold of silicided nMOS output transistors by ensuring uniform current flow," *IEEE Trans. Electron Devices*, vol. 39, pp. 379–388, 1992.
[7] C. Duvvury and C. Diaz, "Dynamic gate coupling of NMOS for efficient output ESD protection," in *Proc. IRPS*, 1992, pp. 141–150.
[8] C. Duvvury, C. Diaz, and T. Haddock, "Achieving uniform nMOS device power distribution for submicron ESD reliability," in *IEDM Tech. Dig.*, 1992, pp. 131–134.
[9] S. Ramaswamy, C. Duvvury, and S.-M. Kang, "EOS/ESD reliability of deep sub-micron NMOS protection devices," in *Proc. IRPS*, 1995, pp. 284–291.
[10] C.-D. Lien, "Electrostatic discharge protection circuit," U.S. Patent 5 086 365, 1992.
[11] M.-D. Ker, C.-Y. Wu, T. Cheng, and H.-H. Chang, "Capacitor-couple ESD protection circuit for deep-submicron low-voltage CMOS ASIC," *IEEE Trans. VLSI Syst.*, vol. 4, pp. 307–321, Sept. 1996.
[12] M.-D. Ker, H.-H. Chang, C.-C. Wang, H.-R. Yeng, and Y.-F. Tsao, "Dynamic-floating-gate design for output ESD protection in a 0.35-μm CMOS cell library," in *Proc. IEEE Int. Symp. Circuits and Systems*, 1998, pp. 216–219.
[13] EOS/ESD Standard for ESD Sensitivity Testing, EOS/ESD Association, Inc., NY, 1993.