A 2-V 2-GHz BJT Variable Frequency Oscillator

Wei-Zen Chen and Jieh-Tsorng Wu, *Member, IEEE*

***Abstract*— A new LC-tuned negative-resistance variable-frequency oscillator (VFO) is described. Frequency tuning is accomplished by using a variable-impedance converter (VIC) to simulate the varactor function. A negative-impedance converter provides the necessary negative resistance for oscillation and also functions as the voltage level shifters for the VIC. A low-voltage translinear circuit is used to linearize the tuning characteristic of the VFO. Implemented in a 0.8 μm 12 GHz f_T BiCMOS technology, the VFO has a tuning range from 1.55 to 2.02 GHz, while consuming 15 mA from a -2 V supply.**

***Index Terms*— Negative impedance converter, variable frequency oscillator, variable impedance converter, voltage-controlled oscillator.**

I. Introduction

VARIABLE-frequency oscillators (VFO's) phase locked to a low-frequency clean reference are commonly used as local oscillators in the radio-frequency wireless transceivers. The VFO's are required to 1) exhibit low internal phase noise for easy optimization for the phase-locked loops; 2) consume little power for battery-powered applications; and 3) be suitable for monolithic integration for small size.

Monolithic VFO's based on the LC-tuned negative-resistance oscillator principle have shown potentials to meet the above requirements [1]–[6]. The VFO's can be depicted with a conceptual schematic shown in Fig. 1, which includes a resonator, a negative-impedance converter (NIC), and a varactor. The resonator is used to reduce the side-band noise of the oscillating signal and can be implemented using on-chip spiral inductors [7], [8] or bonding wires [3], [9]. The NIC provides the necessary negative resistance to sustain oscillation. The magnitude of the NIC's conductance $1/R$ must be larger than the parallel resistive loading $1/R_p$. When oscillating, the signal swing is eventually determined by the circuit nonlinear phenomenon that introduces additional energy loss to balance the energy generated by the NIC [10]. The oscillation frequency of the VFO can be expressed as

$$f_o = \frac{1}{2\pi}\sqrt{\frac{1}{L(C_p + C_v)}}. \tag{1}$$

The frequency f_o can be varied by changing the capacitance of the varactor C_v.

The frequency tuning range of a VFO must be sufficiently large to cover process and temperature variations. For monolithic integration, the varactors are often implemented with the nominal pn-junctions provided by the IC technologies. The VFO's frequency tuning range is severely limited using this tuning scheme, especially at low supply voltage [6]. Although it is also possible to achieve frequency tuning by mixing two resonators with different resonant frequencies [11], while avoiding the use of varactor. The VFO frequency can be changed by varying the weighting of the two resonators in the signal path. There is a tradeoff, however, between the resonator's quality factor and the VFO's frequency tuning range.

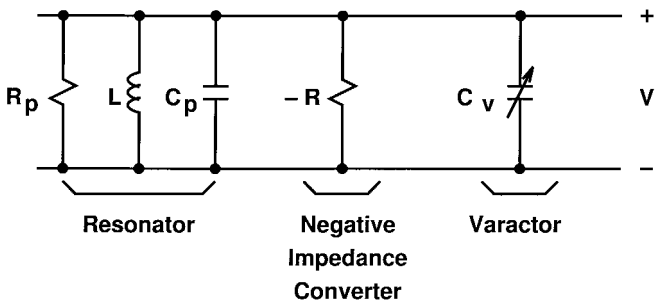

Fig. 1. LC-tuned negative-resistance VFO conceptual schematic.

This paper describes a 2-V LC-tuned VFO that employs a variable-impedance converter (VIC) to simulate a varactor, while achieving a wide frequency tuning range under a low supply voltage [12]. This VIC circuit is described in Section II. Its high-frequency characteristic is also analyzed and discussed. The new VFO and the auxiliary circuits are described in detail in Section III. Several design considerations are also discussed. A prototype VFO chip has been fabricated using a 0.8 μm 12 GHz f_T BiCMOS technology. Measurement results are presented in Section IV. The VFO achieves a wide tuning range of about 500 MHz extending from 1.5 GHz–2 GHz. And finally, conclusions are given in Section V.

II. Variable Impedance Converter

The operation principle of the variable-impedance converter (VIC) can be described using the circuit shown in Fig. 2. Transistors Q7 and Q8 are two voltage-level shifters. The Q5–Q6 emitter-coupled pair degenerated by a fixed passive element Y_1 produces a differential current I_e in response to the input voltage variation, i.e., $I_{e+} - I_{e-} \approx Y_1 \cdot (V_+ - V_-)$. The Q1–Q2 and Q3–Q4 pairs are two current splitters, dividing the I_{e+} and I_{e-} currents, respectively. The output current I can be expressed as $I_+ - I_- = a \cdot (I_{e+} - I_{e-})$, where the gain factor a has a value between $+1$ and -1 and is determined by the differential control voltage V_c. Thus, the equivalent differential admittance of the VIC can be expressed

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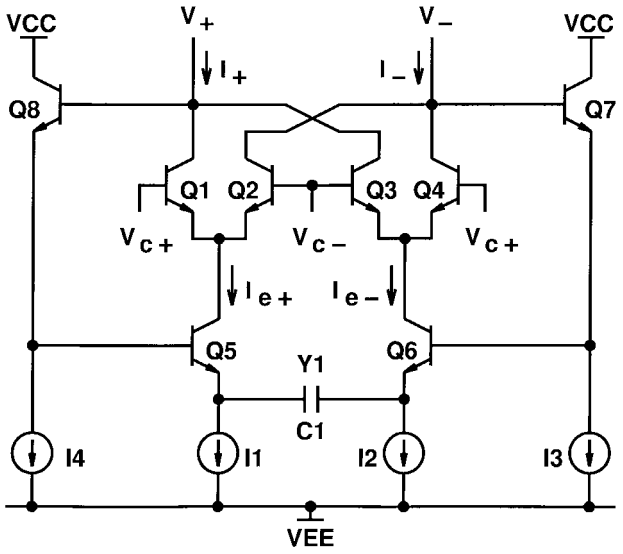

Fig. 2. VIC circuit schematic.

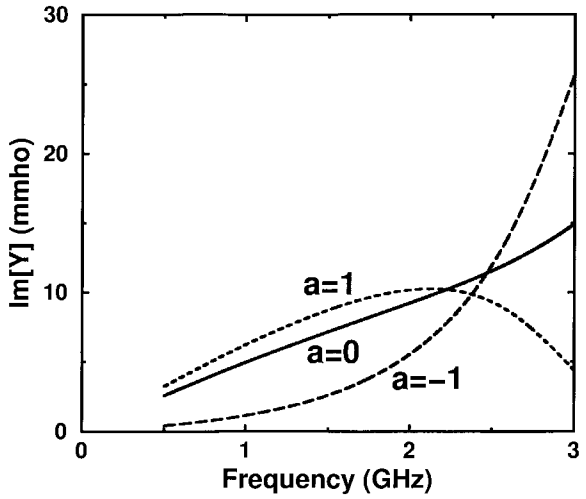

Fig. 3. Simulated VIC admittance imaginary-part frequency behavior.

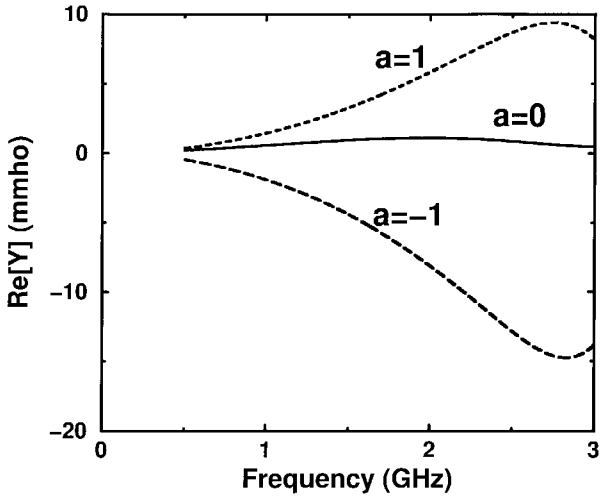

Fig. 4. Simulated VIC admittance real-part frequency behavior.

as $Y_{VIC} = (I_+ - I_-)/(V_+ - V_-) = a \cdot Y_1$, which emulates a variable-admittance element. If the passive element Y_1 is a capacitor, then the VIC functions as a varactor.

A more detailed analysis of the circuit of Fig. 2 can be made by considering the high-frequency behaviors of the devices. It can be shown that the Q5–Q6–C1 emitter-coupled pair is the most crucial part of the circuit that dominates the VIC's frequency behavior at the frequencies of interest. Neglecting the nonideal effects caused by Q7 and Q8, the differential current I_e can be approximated by

$$I_e(s) \approx V(s) \times \frac{sC_1}{1 + s\left(\frac{2C_1 + C_{\pi 5}}{g_{m5}}\right) + s^2\left(\frac{2C_1 r_{b5} C_{\pi 5}}{g_{m5}}\right)} \quad (2)$$

where r_{b5}, g_{m5}, and $C_{\pi 5}$ are the small-signal base resistance, transconductance, and base-emitter capacitance of Q5 and Q6, respectively. At frequencies much less than the transition frequency (f_T) of Q1–Q4, the phase shift between I and I_e can also be neglected. And the equivalent admittance of the VIC can be expressed as

$$Y_{\rm VIC}(j\omega) = a \times \frac{j\omega C_1}{1 - \omega^2\left(\frac{2C_1 r_{b5} C_{\pi 5}}{g_{m5}}\right) + j\omega\left(\frac{2C_1 + C_{\pi 5}}{g_{m5}}\right)} + j\omega C_{pv} = \mathrm{Re}[Y] + j\,\mathrm{Im}[Y] \quad (3)$$

where C_{pv} is the parasitic capacitance associated with V_+ and V_- nodes. Through the control of a, the imaginary part of the $Y_{\rm VIC}(j\omega)$, $\mathrm{Im}[Y]$, can be varied, resulting in the change of the VFO's oscillation frequency. The appearance of $\mathrm{Re}[Y]$, real part of the $Y_{\rm VIC}(j\omega)$, is mainly due to the phase shift in the VIC's signal path.

Figs. 3 and 4 show the SPICE-simulated frequency behaviors of a VIC using transistors from a 0.8 μm BiCMOS technology. Small-signal device parameters are: $g_{m5} = 170$ m℧, $r_{b5} = 100\ \Omega, C_{\pi 5} = 2.2$ pF, and $C_1 = 1.1$ pF. The parasitic capacitors at the emitters of Q5 and Q6 must be included in calculating C_1. From Fig. 3, it is clear that, at low frequencies, the $\mathrm{Im}[Y]$ behaves as a capacitor, whose value can be varied with a. When $a = 0$, the parasitic capacitance C_{pv} with a value of approximately 0.7 pF is exposed. The capacitance C_{pv} is mainly contributed by the collector-to-substrate junctions of Q1–Q4, and the collector-to-base junctions of Q1–Q4 and Q7–Q8. However, as frequency approaching a critical point, ω_c, where

$$\omega_c = 2\pi f_c = \sqrt{\frac{g_{m5}}{2C_1 r_{b5} C_{\pi 5}}} \quad (4)$$

the ω^2 term in (3) can no longer be neglected. Its effect is the reduction of the equivalent capacitor that is variable. At $\omega \approx \omega_c$, the variable capacitor vanishes, and $\mathrm{Im}[Y] = \omega C_{pv}$. For $\omega > \omega_c$, the value of the variable capacitor changes sign, causing nonmonotonic characteristic in the VFO's transfer function. In the above case, the f_c is 2.98 GHz using (4). The f_c is further degraded to 2.4 GHz due to the additional phase shifts in Q1–Q4 and Q7–Q8. The asymmetric $\mathrm{Im}[Y]$ response between the $a = 1$ and $a = -1$ cases in Fig. 3 are mainly caused by the base resistors of Q1–Q4.

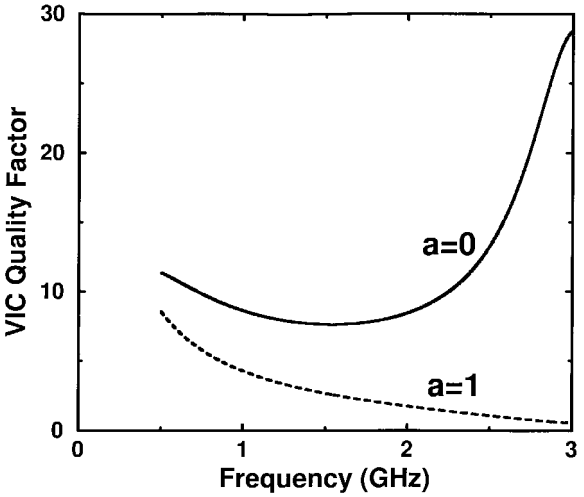

Fig. 5. Simulated VIC quality factor frequency behavior.

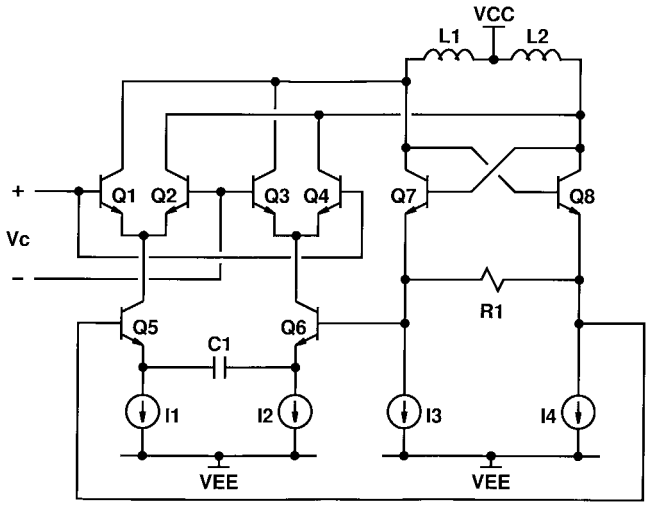

Fig. 6. VFO circuit schematic.

The frequency behavior of the $\mathrm{Re}[Y]$ shown in Fig. 4 can be viewed as a resistor in parallel with the $\mathrm{Im}[Y]$. The conductance of the resistor depends on the frequency as well as the value of a. For $a = 0$, the VIC is essentially disabled and $\mathrm{Re}[Y] \approx 0$. For $a > 0$ and $\omega < \omega_c$, the conductance is positive and its value increases with frequency. The positive conductance can degrade the quality factor of the entire VFO of Fig. 1, or even prevent the VFO from oscillating. For $a < 0$ and $\omega < \omega_c$, the conductance is negative and its absolute value also increases with frequency. The negative conductance can improve the quality factor of the entire VFO.

Fig. 5 shows the frequency behavior of the VIC's quality factor (Q), which is defined as $Q = \mathrm{Im}[Y]/\mathrm{Re}[Y]$. In the case of $a = 0$, the VIC is equivalent to the parasitic capacitor C_{pv} in parallel with a resistor resulting from the Early effect in Q1–Q4. The Q is about 9 at 2 GHz. For $a > 0$, the Q is decreased with increasing frequency. At $a = 1$, the Q is about three at 1.5 GHz, and meanwhile the VFO operates at the lower end of the frequency tuning range. When the VFO's oscillation frequency is increased by decreasing a, the corresponding VIC's Q is also improved. The Q ranges from three to five for 1.5–1.6 GHz oscillation frequency, from five to eight for 1.6–1.8 GHz oscillation frequency, and from eight to ten for 1.8–2 GHz oscillation frequency.

III. Variable-Frequency Oscillator

The circuit schematic of the new VFO is shown in Fig. 6. The VIC varactor consists of transistors Q1–Q6 and capacitor C1. The I1 and I2 current sources must be large enough to allow sufficient ac current flowing through C1. The required condition is

$$I_{1,2} > \Delta V \cdot \omega C_1 \tag{5}$$

where ΔV is the voltage swing of the differential oscillating signal, and ω is the oscillation frequency. The VFO's frequency tuning range can be widen by increasing C1, but at the expense of larger power consumption, since both I1 and I2 have to be increased accordingly. The upper end of the tuning range is also limited by ω_c of (4).

The Q7–Q8 cross-coupled pair and the resistor R1 are configured as a negative-impedance converter (NIC). Transistors Q7 and Q8 also function as the voltage level shifters for the VIC of Fig. 2. The negative resistance looking into the collectors of Q7 and Q8 can be approximated by

$$\frac{1}{Y_{\mathrm{NIC}}} = Z_{\mathrm{NIC}} \approx -R_1\left(1 + s\,\frac{C_{\pi 7}}{g_{m7}}\right) - \frac{2}{g_{m7}} \tag{6}$$

where g_{m7} and $C_{\pi 7}$ are the small-signal transconductance and base-emitter capacitance of Q7 and Q8 respectively. To guarantee oscillation, the real part of $-Y_{\mathrm{NIC}}$ must be larger than the parallel combination of the energy loss in L1 and L2, representing by R_p of Fig. 1, in addition to $\mathrm{Re}[Y]$ of the VIC.

The VFO oscillating signal voltage swing ΔV will stop growing when the remaining energy generated by the NIC is absorbed by the extra energy loss introduced by the large-signal nonlinear effects. The major nonlinear phenomena in the VFO occur when Q7 (or Q8) enters the cut-off region, and when Q8 (or Q7) enters the saturation region. If the two current sources in the NIC, I3, and I4, are large enough so that

$$I_{3,4} > \frac{\Delta V}{R_1} \tag{7}$$

then Q8 (or Q7) will be saturated before Q7 (or Q8) being cut off. In this case, ΔV is limited by the forward biasing of the collector junctions, i.e., $\Delta V \approx V_{BC(\mathrm{on})}$, where $V_{BC(on)}$ is the forward-biased voltage of the collector junctions.

The collectors of Q7 and Q8 are connected to an output buffer with 50 Ω driving capability. The output buffer consists of two emitter followers followed by a resistor-degenerated emitter-coupled pair.

For the VIC of Fig. 6, the current gain a is an exponential function of the control voltage V_c. Translinear circuits are often used to linearize the transfer function. Conventional translinear circuits require additional $V_{BE(\mathrm{on})}$ voltage drop, however, making them unsuitable to drive the VFO under a supply voltage below a 2 V. The low-voltage translinear frequency control circuit shown in Fig. 7 is used to generate the V_c instead. The control input V_f causes a linear change in the differential collector current $I_{c9} - I_{c10}$ of the Q9–Q10

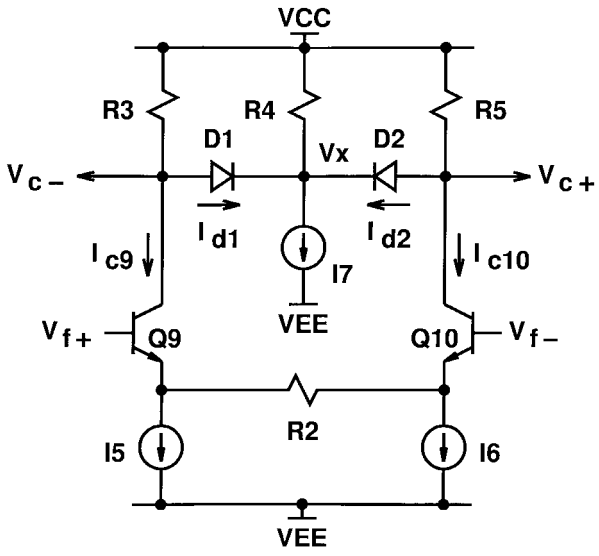

Fig. 7. Translinear frequency control circuit schematic.

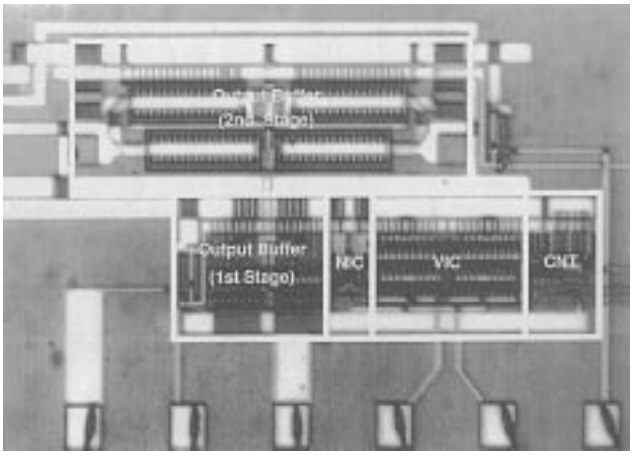

Fig. 8. VFO chip micrograph.

emitter-coupled pair degenerated by the R2 resistor. Since the D1 and D2 diodes are designed to be always forward-biased, the voltage fluctuation at V_{c+}, V_{c-}, and V_x are small, leaving the currents flowing through the resistors, R3–R5, relatively unchanged. Therefore, the differential collector current also causes a linear change in the differential diode current, i.e., $I_{d2} - I_{d1} \approx I_{c9} - I_{c10}$. If p-channel MOSFET's are available, both R3 and R5 can be replaced with constant current sources, resulting in a more accurate translinear function.

The V_c output of the frequency control circuit drives the Q1–Q2 and Q3–Q4 current splitters in the VIC directly. The diode current ratio I_{d2}/I_{d1} is mirrored by the VIC's collector current ratios I_{c1}/I_{c2} and I_{c4}/I_{c3}. The VIC's a factor can then be expressed as

$$a = \frac{I_{d2} - I_{d1}}{I_{d2} + I_{d1}}. \tag{8}$$

Since $I_{d2} + I_{d1}$ has little variation, the gain factor a thus becomes a linear function of the control input V_f.

The minimum supply voltage for the VFO is $V_{BE(on)}$ of Q5–Q6 plus $V_{BE(on)}$ of Q7–Q8 plus $V_{BC(on)}/2$ of Q7–Q8, which is approximately 2 V at room temperature. It has been demonstrated in simulations and experiments that the VFO can still operate even in the low-voltage cases in which the two current sources in the VIC, I1 and I2, are temporarily forced into the operation regions where the output currents are no longer constant.

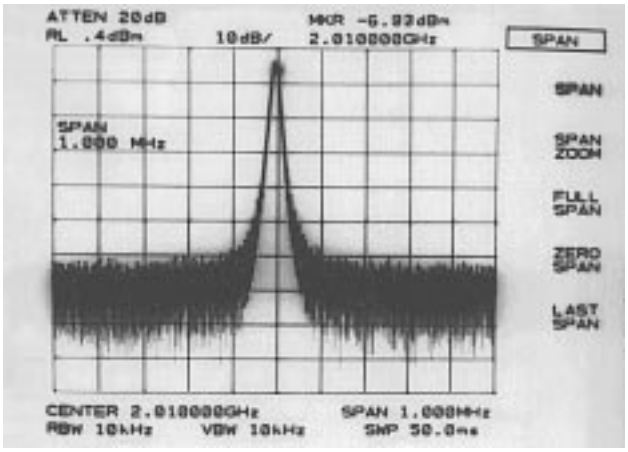

Fig. 9. Measured VFO output spectrum at 2 GHz.

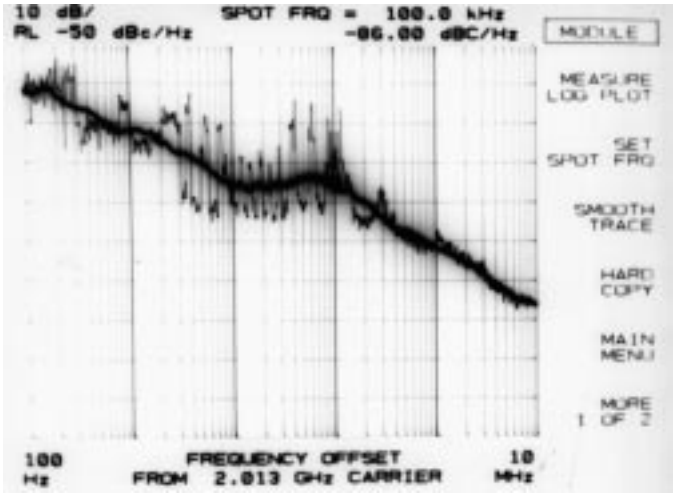

Fig. 10. Measured VFO output phase noise at 2 GHz.

IV. Experimental Results

A VFO experimental chip was fabricated using a 0.8 μm 12 GHz f_T double-poly double-metal BiCMOS technology. The VFO is integrated in a phase-locked-loop frequency synthesizer chip. The chip micrograph is shown in Fig. 8. The area occupied by the VFO is 1050 $\times$ 1500 μm^2. In this prototype, the inductors L1 and L2 are both implemented with bonding wires and are approximately 5 nH. The resistor R1 in the NIC is a 100 Ω polysilicon resistor. The capacitor C1 in the VIC is a 0.7 pF double-poly capacitor. Besides C1, parasitic capacitors at the emitters of Q5 and Q6 also contribute additional capacitance for the voltage-to-current conversion in the VIC.

The chip is attached directly to a circuit board for testing. Fig. 9 shows the VFO's output spectrum at 2 GHz. The output power is -6 dBm when driving a 50 Ω differential load. Fig. 10 shows the measured phase noise of the VFO's output at 2 GHz. The phase noise is -86 dBc/Hz at 100 kHz offset. No significant variation in phase noise is observed for 2 V

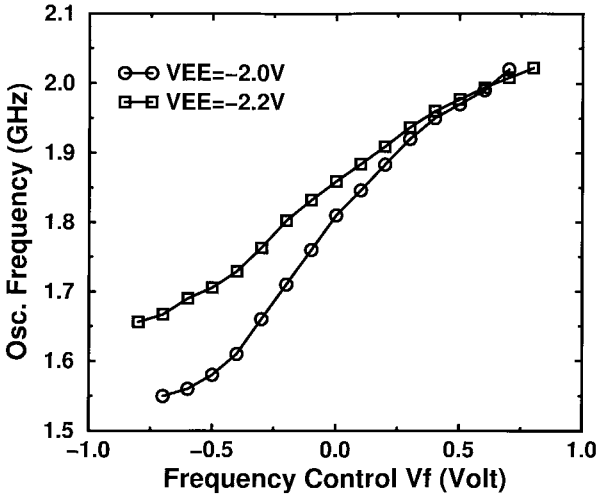

Fig. 11. Measured VFO frequency tuning characteristic.

and 2.2 V supply voltages. Fig. 11 shows the measured VFO's frequency tuning characteristic. The frequency range is from 1.55–2.02 GHz for the 2 V supply and from 1.65–2.02 GHz for the 2.2 V supply. The VFO and the frequency control circuit together consume 15 mA of current, while the output buffer consumes 40 mA.

V. Conclusion

A monolithic LC-tuned negative-resistance VFO has been described. Frequency tuning is accomplished by using a VIC to simulate the varactor function. The maximum operation frequency of the VIC is limited to ω_c of (4). Due to both the early effect in its transistors and the phase shift in its signal path, the VIC can affect the quality factor of the VFO's resonating network. The necessary negative resistance for oscillation is provided by a NIC, which also functions as the voltage level shifters for the VIC. A low-voltage translinear frequency control circuit is used to linearize the voltage-to-frequency transfer function. Implemented in a 0.8 μm 12 GHz f_T BiCMOS technology, the VFO can operate from a single 2-V supply and consumes a total current of 15 mA. It achieves a maximum oscillation frequency of 2 GHz and a frequency tuning range of 30%. The phase noise is -86 dBc/Hz at 100 kHz offset for the 2 GHz output. With a companion output driver, the VFO can deliver -6 dBm output power to a 50 Ω differential load.

References

[1] M. Soyuer and R. Meyer, "High-frequency phase-locked loops in monolithic bipolar technology," *IEEE J. Solid-State Circuits*, vol. 24, pp. 787–795, June 1989.

[2] L. Dauphinee, M. Copeland, and P. Schvan, "A balanced 1.5 GHz voltage controlled oscillator with an integrated LC resonator," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 1997, pp. 390–391.

[3] J. Craninckx and M. Steyaert, "A 1.8-GHz CMOS low-phase-noise voltage-controlled oscillator with prescaler," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1474–1482, Dec. 1995.

[4] M. Soyuer, K. Jenkins, J. Burghartz, and M. Hulvey, "A 3 V 4 GHz nMOS voltage-controlled oscillator with integrated resonator," *IEEE J. Solid-State Circuits*, vol. 31, pp. 2042–2044, Dec. 1996.

[5] A. Rofougaran, J. Rael, M. Rofougaran, and A. Abidi, "A 900 MHz CMOS LC-oscillator with quadrature outputs," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 1996, pp. 392–393.

[6] B. Razavi, "A 1.8 GHz CMOS voltage-controlled oscillator," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 1997, pp. 388–389.

[7] N. Nguyen and R. Meyer "Si IC-compatible inductors and LC passive filters," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1028–1031, Aug. 1990.

[8] J. Chang, A. Abidi, and M. Gaitan, "Large suspended inductors on silicon and their use in a 2 μm CMOS RF Amplifier," *IEEE Electron Device Lett.*, vol. 14, pp. 246–248, May 1993.

[9] J. Craninckx and M. Steyaert "Low-noise voltage-controlled oscillators using enhanced LC-tanks," *IEEE Trans. Circuits Syst.*, vol. 42, pp. 794–804, Dec. 1995.

[10] D. Pederson and K. Mayaram, *Analog Integrated Circuits for Communication: Principles, Simulation, and Design*. Norwell, MA: Kluwer, 1991.

[11] N. Nguyen and R. Meyer, "A 1.8-GHz monolithic LC voltage-controlled oscillator," *IEEE J. Solid-State Circuits*, vol. 27, pp. 444–450, Mar. 1992.

[12] W.-Z. Chen and J.-T. Wu, "A 2 V 2 GHz BJT variable-frequency oscillator," in *Proc. Bipolar/BiCMOS Circuits and Technology Meet.*, Sept. 1997, pp. 61–63.

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Dr. Wu is a member of Phi Tau Phi.