Excellent Low-Pressure-Oxidized Si_3N_4 Films on Roughened Poly-Si for High-Density DRAM's

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Abstract—**High-reliability and good-performance stacked storage capacitors with high capacitance value of 17.8 fF/μm^2 has been realized using low-pressure-oxidized thin nitride films deposited on roughened poly-Si electrodes. This novel electrodes are fabricated by H_3PO_4-etched and RCA-cleaned. The leakage current density at +2.5 and −2.5 V are 9.07×10^{-9} and -2.4×10^{-8} A/cm^2, respectively, fulfilling the requirements of 256 Mb DRAM's. Weibull plots of time-dependent-dielectric-breakdown (TDDB) characteristics under constant current stress and constant voltage stress also show tight distribution and good electrical properties. Hence, this easy and simple technique is promising for future high-density DRAM's applications.**

I. Introduction

To promote the density of dynamic-random-access-memories (DRAM's), the cell area in DRAM structures must be reduced. Reduction of cell capacitance, resulting from the memory cell miniaturization, is one of the most serious problems. From the calculated equation of the capacitance, there are three ways to increase the capacitance of DRAM capacitors. One is to enlarge the effective surface area of the storage-nodes [1]–[5], another is to reduce the thickness of the dielectrics [6], [7], and the other is to utilize high dielectric constant materials [8]. Many advanced structures have been investigated to increase the surface area of the storage-nodes, however, it is difficult to carry out these complicated storage-node structures by using conventional processes. On the other hand, the high dielectric constant materials still have high leakage current and low reliability which must be furthermore conquered in the future for high-density DRAM applications. In this letetr, the combination of the first two concepts to increase the cell capacitance of DRAM capacitors is proposed. The roughened poly-Si which is etched by hot phosphoric acid (H_3PO_4) and cleaned by standard RCA procedures can enlarge the surface area more than three times, resulting from the formation of micro-islands on the poly-Si. Via low-pressure oxidizing the thin nitride films, thinner as well as better oxide/nitride/oxide dielectrics for DRAM capacitors are achieved. To use these two techniques, novel capacitors with high capacitance, low leakage current, and high reliability are successfully implemented.

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II. Experimental Procedures

Capacitors with doped and roughened poly-Si bottom electrodes were fabricated on Si substrate covered with 3000-Å thick SiO_2 which was grown at 1050 °C in a steam ambient. To avoid the poly-Si broken during H_3PO_4 treatment, double-layered poly-Si structure was used in this work. A 1000-Å thick LPCVD poly-Si was deposited at 620 °C and then phosphorous-implanted with 30 KeV, 4×10^{15} cm^2. After these wafers were annealed at 850 °C for 30 min, the native oxide was removed by diluted 5% HF solutions and a 2000-Å thick poly-Si was deposited again. These wafers were phosphorous-implanted with 30 KeV, 6×10^{15} cm^2 and annealed at 850 °C for 30 min. After the native oxide was removed, these wafers were etched by 85% phosphoric acid (H_3PO_4) at 120 °C for 150 min. Prior to the thin nitride films deposition, these wafers were cleaned by standard RCA cleanup procedures. A 50 Å-thick nitride films were deposited at 750 °C by LPCVD using the SiH_2Cl_2/NH_3 mixture and then some of these samples were oxidized at 850 °C, 760 torr for 30 min in dry O_2 ambient. The others were performed by low-pressure oxidation at 850 °C, 0.5 torr for 30 min in dry O_2 ambient. A 2700 Å-thick poly-Si were deposited as the top electrodes and was doped by $POCl_3$-diffused at 850 °C for 40 min. Consequently, capacitance-voltage (C–V) measurements revealed the effective oxide thickness ($t_{\mathrm{ox,eff}}$) which was calculated from the capacitance using the oxide dielectric constant of 3.9 and the mask area, flat plate, not including the sidewalls of the electrodes.

III. Results and Discussion

The dielectric film formed by low-pressure oxidation of thin nitride is called as LPO and the other one formed by atmospheric-pressure oxidation of thin nitride is APO. The effective oxide thicknesses ($t_{\mathrm{ox,eff}}$) for the LPO and APO on the prepared roughened poly-Si electrodes are 19.4 and 22.5 Å, respectively, which are calculated from the capacitance measured by C–V method. The capacitance of 17.8 fF/μm^2 ($t_{\mathrm{ox,eff}} = 19.4$ Å) is not enough. Nevertheless, the electrode sidewall for the stacked-capacitor structure can be simultaneously performed and the capacitance for the 256-Mb DRAM's can be therefore achieved [5]. Fig. 1 compares the cumulative failure rates under constant voltage (6 V) test for the capacitors with LPO and APO dielectric films under both gate polarities. For each type of samples, 25 capacitors were tested to construct the time-to-breakdown (T_{BD}) statistics. Obviously, the capacitors with LPO show longer T_{BD} for both

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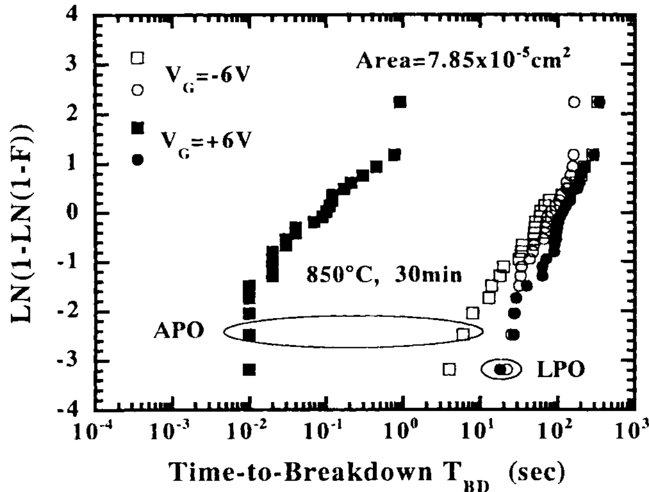

Fig. 1. Weibull plots of TDDB characteristics under constant voltage (6 V) stress for the capacitors with LPO and APO under both gate polarities.

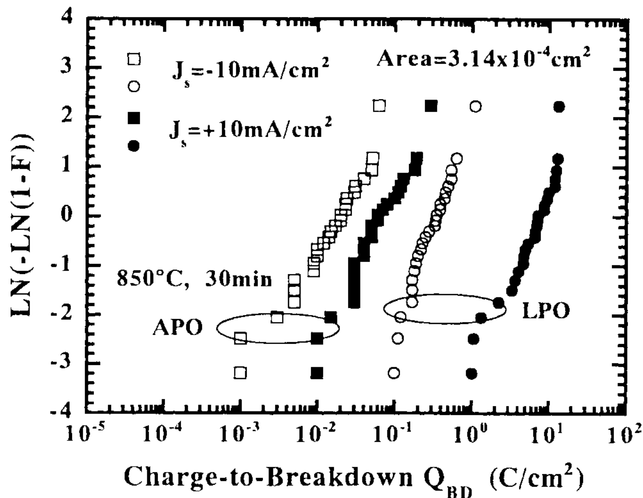

Fig. 2. Weibull plots of charge-to-breakdown (Q_{BD}) under constant current stress (10 mA/cm^2) for the capacitors with LPO and APO under both gate polarities.

polarities than those with APO. In addition, the capacitors with LPO possess tighter and similar distribution for both stress polarities. In constrast, the capacitors with APO express a wider distribution than those with LPO, particularly in positive gate-bias (+Vg). It has been reported that low pressure oxidation of thin nitride film is able to grow the oxide on the top and bottom of the nitride layers and only bottom oxide formed for the atmospheric pressure oxidation [7]. Therefore, an ONO stacked dielectric was formed on the roughened poly-Si surface in LPO samples and only NO structure in APO samples. Owing to this ONO structure, the capacitors with LPO is surmised to result in the longer and tighter T_{BD} distribution. Fig. 2 shows the Weibull plots of TDDB characteristics under constant current (10 mA/cm^2) stress for the capacitors with LPO and APO under both gate polarities. Both gate currents were applied on the capacitors with an area of 3.14×10^{-4} cm^2, lithography mask area. Whatever the

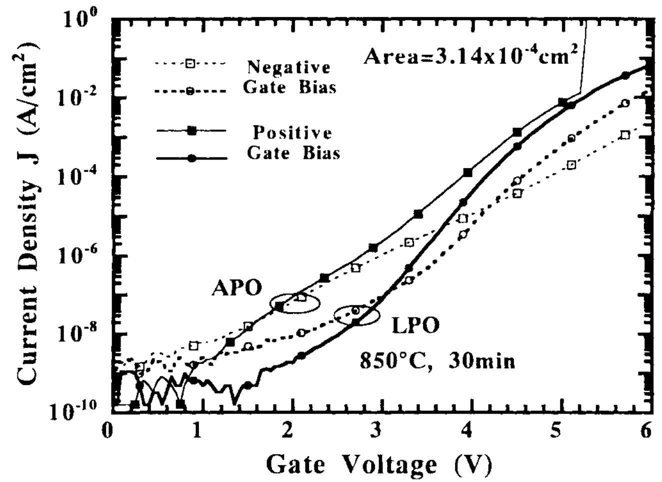

Fig. 3. The curves of current density versus voltage (J–V) for the capacitors with LPO and APO biased at both gate polarities.

gate polarities, the capacitors with LPO have a longer as well as tighter t_{BD} distribution than those with APO. This result is consistent with previous researches [6]. Hence, low-pressure oxidation is an effective method for reducing the defect density of the dielectric films and improving the reliability. The curves of current density versus voltage (J–V) for the capacitors with LPO and APO biased at both gate polarities are shown in Fig. 3. A significient reduction in leakage current is also observed for the capacitors with LPO for both gate polarities as compared to those with APO at low applied voltage. For the capacitors with LPO, the current densities at +2.5 V and −2.5 V are 9.07×10^{-9} A/cm^2 and -2.4×10^{-8} A/cm^2, respectively, and are better than previous reports [2], [5], [9]–[11]. However, the current densities are 4.15×10^{-7} A/cm^2 and -2.75×10^{-7} A/cm^2 at the same biases for the APO sample and they are higher than one order as compared to LPO ones. The reduction in leakage current for LPO is believed to be due to the formation of ONO stacked structure on the roughened poly-Si [7]. Therefore, the technique of low-pressure oxidation can not only decrease the leakage current but also decrease $t_{\mathrm{ox,eff}}$ with respect to the APO one. The TDDB lifetime-characteristics extracted from time-to-50% cumulative-failure as a function of applied voltage are shown in Fig. 4. Capacitors with LPO show much longer t_{BD} than those with APO at the same voltage for positive gate bias. Under negative gate bias, the capacitors with LPO is similar to those with APO. This result is consistent with the outcome of Fig. 1. The long-term lifetime can be predicted by using Fig. 4 and the capacitors with LPO are estimated to survive long enough for more than ten years at a stress voltage ~3.8 V which is larger than the operating voltage for 256 Mb DRAM's.

IV. Conclusion

In summary, the low-pressure oxidation of thin nitrides on the roughened poly-Si exhibits high capacitance (17.8 fF/μm^2, i.e., $t_{\mathrm{ox,eff}}$ is 19.4 Å), low leakage current under both gate polarities, and high reliability for constant current and constant voltage stress. Since the electrical properties of the dielectrics

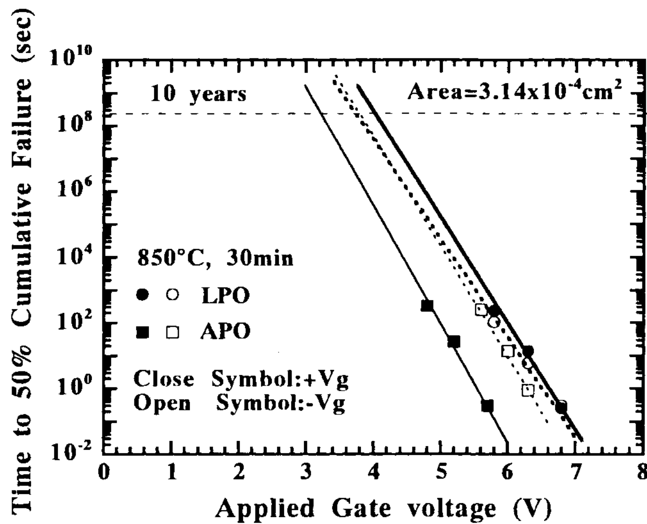

Fig. 4. The TDDB lifetime extracted from the time-to-50% cumulative-failure as a function of applied voltage.

on the roughened poly-Si can satisfy the requirements of 256 Mb DRAM's, this easy and simple technology is promising for future high-density DRAM's applications, especially, as the stacked-capacitor structure is used and the sidewalls of the electrodes are considered.

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