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# A study of tilt angle effect on Halo PMOS performance

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### **Abstract**

The Halo structure is usually adopted in deep submicrometer MOS devices for punchthrough prevention. The tilt angle of the Halo implant determines the dopant distribution which induces anti-punchthrough operation. In this paper, we investigate the impact of the tilt angle on the Halo PMOS device performance via two-dimensional (2D) simulations. We find that the ratio of on-current to off-current is constant for all tilt angles of Halo implant, implying an equivalent DC performance for all tilt angles. The equivalence can be traced back to a self compensation between the body factor and source resistance. The result implies that a low tilt angle should be adopted for Halo devices, for it gives a small threshold voltage and thus a high noise margin. The methodology used in analyzing body factor and source resistance can also be applied to analyze other devices. © 1998 Elsevier Science Ltd. All rights reserved.

### 1. Introduction

In deep submicron MOS technology, various techniques have been used to enhance device speed. The goal is to maximize the on-state current, while simultaneously keeping the off-state leakage current below a certain level [1-3], or to reduce parasitic capacitance [4-6]. However, existing fabrication techniques have several major issues which make the goals difficult to achieve. For example: (i) range and deviation of implant does not reduce with device scaling, and (ii) required process thermal cycles cause some dopant spread to be relatively large in deep submicrometer dimensions [7-9]. Both issues can cause dopant spread in the drain or channel to induce the following negative phenomena: (i) drain (or lightly doped drain) dopant spread gives increased off-state leakage current, and (ii) channel dopant spread gives increased junction and intrinsic capacitances. Both phenomena lead to device speed degradation.

To obtain a high device speed, devices with innovative architectures have, therefore, been proposed [10–13]. These structures include super-steep retrograde-well doping profile (called SSR) [10], large tilt angle drain [11], and Halo anti-punchthrough implant (or called pocket implant) [1,2,13]. Among these structures, SSR and Halo are developed specifically for preventing the punchthrough effect, while maintaining limited body effect and junction capacitance.

The Halo structure has a local dopant pocket placed next to the drain and source junctions (named the Halo implant). The Halo implant can be independently adjusted for preventing punchthrough. The dopant spread in the channel frees from the conventional duty of punchthrough suppression, and can be reduced (to be less than the channel dimension) to give a reduced body effect. Thus, only a medium level of dopant focus is required, allowing for a reasonable thermal budget in wafer processing. For this reason, the Halo structure has been widely adopted [21] in state-of-theart CMOS technology. On the other hand, the SSR structure requires a precisely-controlled doping profile uniformly distributed through the channel, with its concentration peak (in the vertical direction) being at

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Table 1 Process flow

Process step	Process conditions
P-type formation	< 100 > substrate, Boron 1.3e15 cm <sup>-3</sup>
N-well formation	Phosphorus $1.3 \times 10^{13}$ cm <sup>-2</sup> ,
	energy = 460  keV
Channel implant	Phosphorus $2 \times 10^{12}$ cm <sup>-2</sup> ,
	energy = 40  keV
Gate oxide	thickness = $55 \text{ Å}$
Poly deposition	thickness = $0.1 \mu m$ , length = $0.18 \mu m$
Halo implant	material/dose/energy/tilt: Arsenic * cm <sup>-2</sup> ,
	energy = 130 keV, tilt angle = *degree
LDD implant	$BF_2 1 \times 10^{13} \text{ cm}^{-2}$ , energy = 25 keV
Spacer formation	length = $0.08 \mu m$
P + S/D implant	$BF_2 2 \times 10^{15} \text{ cm}^{-2}$ , energy = 30 keV
RTA annealing	1000°C, 30 s

the main leakage current path [10]. This requires an extremely low thermal budget during wafer processing, making the SSR structure practically more difficult to obtain.

The benefits of the Halo structure for eliminating the off-state leakage current has been demonstrated in some previous works [1, 5, 13]. Rodder et al. demonstrated that the Halo structure can improve the threshold voltage lowering and the ratio of drive current to off-state [1]. However, the Halo structure may also induce several negative phenomena that can significantly degrade the on-state drive current and dynamic speed, thus offsetting the advantage gained at reducing off-state leakage current. These phenomena include increased source resistance and body effect, increased junction capacitance, and enhanced hot electron degradation. Hence, a great profile design of Halo implant to give effective punchthrough stop, while simultaneously avoiding the above-mentioned phenomena, is very needed.

As so motivated, in this paper we give an investigation of the profile design of Halo implant. We use 2-D simulations, and focus our attention on the effect of tilt angle of Halo implant, since the tilt angle significantly influences the dopant distribution. Our goal is to develop a general methodology for device optimization by analyzing internal physical parameters such as body factor and source resistance, and their mutual interactions and impacts on terminal characteristics such as current. As these internal physical parameters cannot be measured, the only way to obtain an analysis for them is through simulation.

This paper is organized as follows: Section 2 describes the simulation experiment environment. Section 3 gives trade-off analysis of the on-state and off-state currents under various tilt angles and implant conditions. Section 4 concludes the paper.

## 2. Simulation experiment

In designing the Halo implant, three variables are considered adjustable: dose, energy and tilt angle. Among these parameters, impacts of dose and energy are well known: increased dose can strengthen the anti-punchthrough capability, and increased energy can bring the Halo implant to a deeper part of the channel. On the other hand, the effect of the tilt angle is not intuitively clear, and the study of it has not been reported in the literature, at least to the authors' knowledge. To investigate the influence of the tilt angle, we will study the current-voltage characteristics, and the distributions of depletion charge and local resistance on the equivalent circuit level [17]. The latter data can help us to identify contribution of the Halo implant distribution on each equivalent circuit component.

A Halo PMOS with channel length of  $0.18 \, \mu m$  is simulated for this study. The process flow is briefly described in Table 1. The tilt angle and dose of Halo implant, with values denoted by the symbol, are used as the parameters for the study. The split conditions for Halo implant are listed in Table 2. All other process conditions are also set as constants.

To obtain a reliable device simulation, two calibration procedures need to be executed beforehand, i.e. the doping profiles at various process sequences [16, 20, 21] and the electrical characteristics of the device [17, 19]. The profile calibration is based on SIMS data of one-dimensional (1D) doping profiles, with the implant doses close to the target values and with thermal cycles identical to the target process

Table 2 Split conditions

	HALO implant condition		
Split number	Dose/cm <sup>-2</sup>	Tilt angle (degree)	
A	$3 \times 10^{12}$	0	
В	$7 \times 10^{12}$	0	
C	$9 \times 10^{12}$	0	
D	$1 \times 10^{12}$	15	
E	$3 \times 10^{12}$	15	
F	$5 \times 10^{12}$	15	
G	$1 \times 10^{12}$	30	
H	$2 \times 10^{12}$	30	
I	$3 \times 10^{12}$	30	
J	$5.2 \times 10^{12}$	30	
K	$8.5 \times 10^{11}$	40	
L	$1 \times 10^{12}$	40	
M	$2 \times 10^{12}$	40	
N	$3 \times 10^{12}$	40	

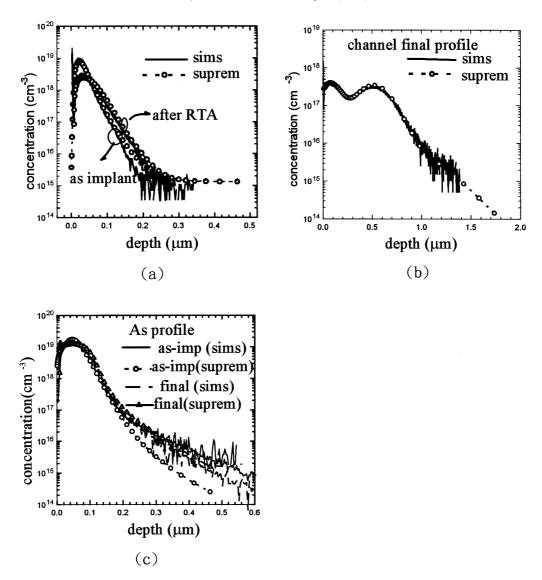


Fig. 1. Comparison of SIMS data and SUPREM simulation. (a) Bf2, (b) phosphorus, (c) arsenic.

flow. The as-implant profiles are calibrated by adjustparameters in the dual distribution [16, 20]. Diffusion and maximum-damage parameters are adjusted to fit profiles after thermal cycles. The comparison of simulated doping profiles and SIMS data is given in Fig. 1(a)-(c), showing good agreement in both as-implant and final distributions. In Fig. 1(a), Bf2 is implanted by an energy of 30 KeV, and with a dose of  $3 \times 10^{13}$  cm<sup>-2</sup>. In Fig. 1(b), the phosphorus implant includes a first dose of  $1.3 \times 10^{13}$ cm<sup>-2</sup> by 460 KeV (well implant), a second dose of  $5 \times 10^{12}$  cm<sup>-2</sup> by 120 KeV (field implant), and a third dose of  $3 \times 10^{12}$  cm<sup>-2</sup> by 60 KeV (threshold implant). In Fig. 1(c), the arsenic is implanted with a dose of  $10^{14}$  cm<sup>-2</sup> by an energy of 100 KeV. All samples in this calibration experiment receive a 30 s RTA annealing of 1000°C after the source and drain implantation. The profiles included in this comparison cover the Halo profile as represented by arsenic, the channel profile as represented by phosphorus, and lightly-doped drain profile as represented by boron. In addition to the vertical profile, the lateral straggling of the implant further affects the lateral electrical field and thus, the punchthrough phenomenon. We obtain the parameters of lateral straggling via 2D Monte Carlo simulations of implanted dopants. The diffusion simulation is carried out based on full coupling of interstitial, vacancy and dopants [21], with diffusion, segregation and damage parameters, extracted based on SIMS data after various thermal cycles.

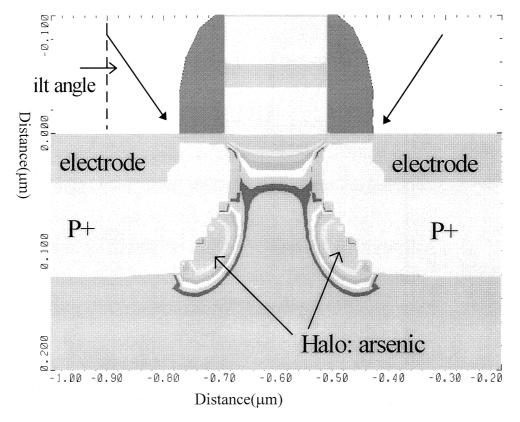


Fig. 2. Cross-sectional view of a 0.18  $\mu$ m Halo PMOS.

The electrical characteristics of device simulation are calibrated based on a fabricated device from a 0.25  $\mu$ m technology. This process has a similar thermal cycle as our target process listed in Table 1. Calibrated parameters include  $ecp.mu = 7.5 \times 10^5$  V/m (critical electrical field), and GSurfp = 0.9 (fitting parameter) in the SRFMOB2 model [16]. With both calibrated profiles and the electrical characteristics, the analysis of the tilt angle of the Halo implant will proceed in the next section.

# 3. Effect of the Halo implant tilt angle

The simulated device cross-section is shown in Fig. 2, with a tilt angle for the Halo implant of 45°. The arsenic Halo dopant is clearly shown to be distributed in the form of a pocket next to the drain junction.

### 3.1. On-state and off-state currents

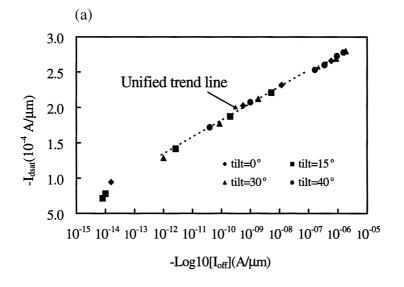
Denote by  $I_{\rm dsat}$  the on-state conduction current and  $I_{\rm off}$  of the off-state leakage current. We define  $I_{\rm dsat}$  to be taken at  $V_{\rm ds}=-1.9~{\rm V}$  and  $V_{\rm gs}=-1.8~{\rm V}$ , and

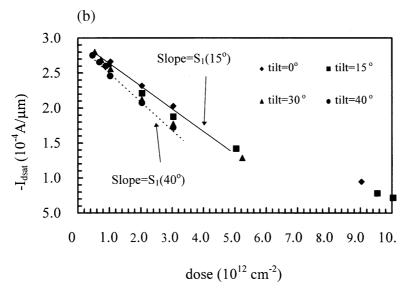
 $I_{\rm off}$  to be taken at  $V_{\rm gs}=-0.1\,{\rm V}$  and  $V_{\rm ds}=-1.9\,{\rm V}$ . With the definition, the simulated scatter plots of  $I_{\rm dsat}$  vs  $I_{\rm off}$  for various tilt angles and implant doses are shown in Fig. 3(a). It is clearly shown that all splits lie on a unified trend line, indicating that all splits are identical. This implies that the same  $I_{\rm dsat}$  can be obtained based on the same  $I_{\rm off}$  constraint, provided that proper implant doses are given. Based on this observation, one can conclude that the tilt angle of the Halo implant, though affecting the Halo dopant distribution, does not affect the ultimate device drive current.

This equivalence of device DC performance is further verified based on an analysis of the impact of implant dose on  $I_{\rm dsat}$  and  $I_{\rm off}$ . Firstly, a novel figure of merit parameter S is defined to model the sensitivity of  $I_{\rm dsat}$  vs  $I_{\rm off}$ , i.e.

$$S = \frac{\delta I_{\text{dsat}}}{\delta I_{\text{off}}}.$$
 (1)

The parameter S can be further decomposed into two sensitivity parameters  $S_1$  and  $S_2$  in the form of  $S = S_1 \times S_2$ , with:





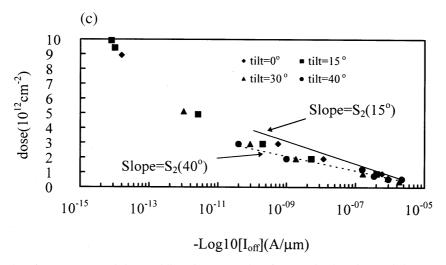
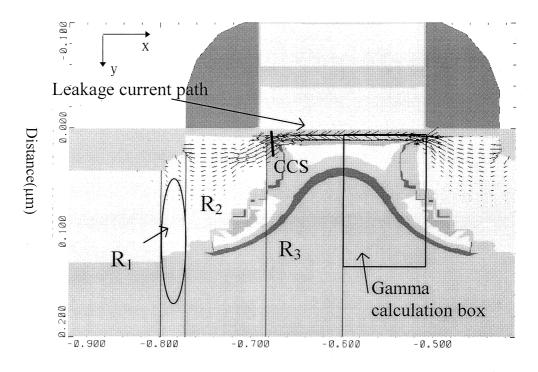


Fig. 3. (a) Scatter plot of  $I_{\rm dsat}$  vs  $I_{\rm off}$ , and the trend line. (b) Scatter plot of  $I_{\rm dsat}$  vs implant dose and slope  $S_1$ . (c) Scatter plot of implant dose vs  $I_{\rm off}$  and slope  $S_2$ .



# Distance(µm)

Fig. 4. Gamma calculation box and resistances in the PMOS.

$$S_1 = \frac{\delta I_{\text{dsat}}}{\delta dose} \tag{2}$$

and

$$S_2 = \frac{\delta dose}{\delta I_{\text{off}}}. (3)$$

The scatter plots of  $I_{\rm dsat}$  vs dose and of dose vs  $I_{\rm off}$  are shown in Fig. 3(b) and (c), respectively, with the parameters  $S_1$  and  $S_2$  given by the slopes of the regression lines. It is found that the Halo implant of a large tilt angle (40°) strongly degrades the device on-state current, comparing with that of a small tilt angle (15°). Here, in this particular example,  $S_1(40^\circ) = -4.1 \times 10^{-17}$  and  $S_1(15^\circ) = -3 \times 10^{-17}$ . This stronger  $I_{\rm dsat}$  degradation from larger Halo tilt angle can be attributed to the fact that Halo dopants are located closer to the channel surface, giving increased channel dopants. The on-state current degradation here can be induced by either increased body effect charge [2], increased  $V_{\rm th}$  or increased source and drain parasitic resistance; this will be discussed later.

The dependence of  $I_{\rm off}$  on *dose* is similar, with the sensitivity parameter  $S_2$  at  $15^{\circ}$  (with the value of  $-7.2 \times 10^{11}$ ) larger than that at  $40^{\circ}$  (with the value of  $-5.26 \times 10^{11}$ ). This differentiation in the off-state cur-

rent sensitivity can also be attributed to the location of Halo dopant. As before, a larger tilt angle gives a stronger suppression of the leakage current. Since  $S = S_1 \times S_2$ , we observe that the resulting sensitivities S of both tilt angles are equivalent. This equivalence indicates that the tilt angle of the Halo implant need not be used as a device tuning parameter in the process development. To further explore and investigate this equivalence, we analyze two device parameters on the equivalent circuit level [17], i.e. source resistance  $R_s$  and body factor  $\gamma$ , as they are the two major parameters which can be affected by Halo dopant, and which can also affect both the on-state and off-state leakage currents.

# 3.2. Body factor and source resistance

In analyzing the body factor  $\gamma$ , note that we are only interested in the local body factor close to the source and drain junctions, as the channel part does not receive the Halo implant and will not be affected. We define a box for calculating  $\gamma$ , namely the *gamma calculation box*, close to the junctions as shown in Fig. 4. We calculate the average depletion charge density inside this box via:

Table 3
Resistance and body factor

Split	$R_1(\Omega)$	$R_2(\Omega)$	$R_3(\Omega)$	Total Res. $(\Omega)$	$\gamma(V^{1/2})$
A	5.28	268	1526	1799	0.3794
В	3.41	161	2486	2650	0.5320
C	2.25	115	3379	3497	0.5947
D	4.95	366	1111	1482	0.3022
E	2.44	300	1599	1902	0.4419
F	4.21	195	2101	2300	0.5466
4.91	365	1137	1507	0.2753	
H	4.54	269	1437	1711	0.3342
4.93	290	1665	1959	0.3858	
J	3.91	180	2288	2472	0.4789
K	4.91	355	1123	1483	0.2529
L	4.85	356	1157	1518	0.2613
M	4.44	259	1479	1743	0.3109
N	3.99	271	1725	2000	0.354

$$\gamma = \frac{\sqrt{2q\epsilon_s \bar{N}_d}}{C_{\text{ox}}},\tag{4}$$

where  $\bar{N}_{\rm d}$  is the average depletion charge density in the box defined as:

$$N_{\rm d} = \frac{\int_{(x,y) \text{inthebox}} N_{\rm d}(x,y) dx dy}{\int_{(x,y) \text{inthebox}} dx dy}.$$
 (5)

In Eq. (4),  $C_{\rm ox}$  is the unit area gate oxide capacitance, q is the unit charge, and  $\epsilon_{\rm s}$  is the silicon dielectric constant. In analyzing the source resistance  $R_{\rm s}$ , we divide the channel resistance close to the source into three sections,  $R_1$ ,  $R_2$  and  $R_3$ ;  $R_1$  denotes the resistance in the source diffusion region,  $R_2$  the resistance in the lightly-doped drain (LDD) region (under the spacer), and  $R_3$  the channel-to-LDD crowding resistance. These resistances are shown in Fig. 4. Let CCS be a channel cross-section in the y-direction across the channel, as shown in Fig. 4. These resistances are extracted by taking the ratio of quasi-Fermi-potential drop across each resistor and the channel current via the following equation:

$$R_{\rm s} = \frac{\Delta \bar{\phi}_{\rm qf}}{\int_{ccs} J {\rm d}y},\tag{6}$$

with

$$\Delta \bar{\phi}_{qf} = \frac{\sum_{ccs} \phi_{qf} J}{\sum_{ccs} J}.$$
 (7)

In Eq. (6),  $\phi_{qf}$  denotes the quasi-Fermi potential, or equivalently the channel potential,  $\Delta$  the difference operator of the quantities at the two nodes of each resistor, and J the current density via the unit cross-sectional area in the channel. The parameter  $\phi_{qf}$  is meant to extract the weighted mean of quasi-Fermi potential using the current density J as a weighting par-

ameter. Among the three resistances,  $R_3$  dominates the source resistance  $R_8$ .

The calculated body factor  $\gamma$  and resistances  $R_1$ ,  $R_2$ and  $R_3$  are listed in Table 3, for various tilt angles and dose splits of the Halo implant. To explore the impact of  $\gamma$  and  $R_s$  on the performance equivalence, we note that split E (with 15° tilt angle) and split N (with 40° tilt angle) have similar  $I_{dsat}$ , based on an equivalent dose of  $3 \times 10^{12}$  /cm<sup>2</sup>. However, the parameter  $\gamma$  for split E is much larger than that for split N. This can be attributed to the fact that the localized pocket with high tilt angle only increases the local doping concentration in the upper part of the gamma-calculationbox. Owing to a large angle during implantation, a considerable portion of the implant dose has also been blocked by the gate polysilicon, thus further reducing the value of  $\gamma$ . The concentration in the lower part of the box is low, as this part does not receive the Halo dopant. Hence,  $\gamma$  for the device with a high tilt angle is small. On the other hand, the Halo implant of lower tilt angle has comparatively more uniformly distributed Halo dopant throughout the box. This, together with the fact that only a very limited implant dose is blocked by gate polysilicon, gives the Halo implant of lower tilt angle a larger  $\gamma$ . The values of  $\gamma$  for various splits are shown in Fig. 5, showing that with similar  $I_{dsat}$ ,  $\gamma$  increased with decreased tilt angle, for a tilt angle ranging from  $15^{\circ}$  (labeled as *DEF*) to  $40^{\circ}$ (labeled as KLMN). This difference shown in  $\gamma$  must be self compensated by other effects, which we suggest are due to  $R_s$ , as the following result indicates.

Opposite to the case of  $\gamma$ , resistance  $R_3$ , which dominates  $R_s$ , decreases with decreased tilt angle. We suggest here that in the case of high tilt angle, the channel of inversion carriers is squeezed and thinned by a local Halo dopant peak close to the channel

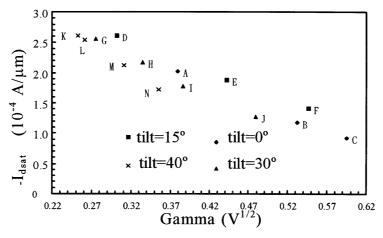


Fig. 5. The  $I_{\rm dsat}$  distribution vs body factor  $\gamma$ .

surface, and  $R_3$  increases with a decreased conduction layer thickness. Split E shows a smaller resistance  $R_3$  than split N, and this compensates the larger  $\gamma$  in split E. Fig. 6 shows the simulated  $I_{\rm dsat}$  vs  $R_3$ , with  $R_3$  in splits E (15°), I (30°) and N (40°) (which all have similar  $I_{\rm dsat}$ ); observe that  $R_3$  decreases with a decreased tilt angle.

The design of NMOS should be similar to the PMOS described here. NMOS use boron as the halo dopant. Although the broad spread of boron may give a smaller  $S_1$  and a larger  $S_2$  compared with PMOS, a similar conclusion should still be drawn.

### 3.3. Threshold voltage

In addition to on-state and off-state currents, threshold voltage  $V_{\rm th}$  is also a critical parameter for MOS devices. Ideal threshold voltage approaches to zero so that the noise margin of a CMOS inverter can be maximized [20]. The threshold voltages of all splits vs the Halo implant dose are shown in Fig. 7. It is

clearly seen that  $V_{\rm th}$  increases with an increased tilt angle, because of a high local doping concentration of the Halo dopant close to the channel surface. The high threshold voltage from the high tilt angle is different from the dependence of body factor on tilt angle, which reduces with an increased angle. This difference is due to the fact that a low tilt angle creates a high local concentration throughout the gamma-calculationbox, while a high tilt angle only creates a high concentration on the surface. The increased  $V_{\rm th}$  for a high tilt angle also reduces the  $I_{dsat}$ ; however, its effect on  $I_{dsat}$ is relatively minor compared with the body factor [17]. Based on the threshold voltage results, one can conclude that a high tilt angle, though turning off off-state leakage in a stronger manner, may give a smaller noise margin. One can particularly observe that on split N and E, both with the implant dose of  $3 \times 10^{12} / \text{cm}^2$ ,  $V_{\text{th}}(\text{split E}) = 0.4 \text{ V}$  but  $V_{\text{th}}(\text{split N}) = 0.5 \text{ V}$ . This gives a noise margin difference of NM(split E) – NM(split N) = 0.044 V, which is non-negligible for the typical 0.75 V noise margin in technology with

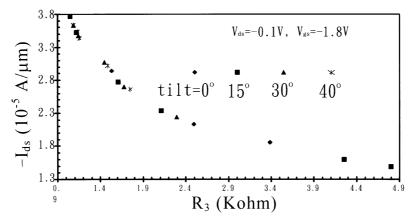


Fig. 6. The  $I_{\rm dsat}$  distribution vs resistance  $R_3$ .

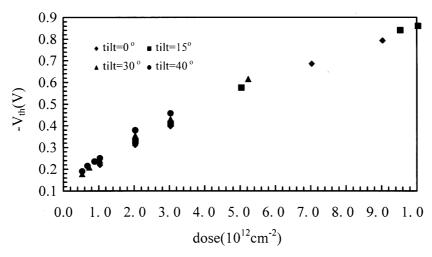


Fig. 7. Threshold voltage distribution of the Halo PMOS.

a 1.8 V power supply. By taking the noise margin into consideration, a tilt angle of less than 15° should be adopted.

#### 4. Conclusion

The impact of the Halo implant tilt angle on the PMOS performance has been investigated. A constant ratio of drive current to off-state leakage current for different tilt angles has been demonstrated, implying an equivalent DC performance for different tilt angles. This equivalence has been further explored and verified by observing a self-compensation effect between the body effect, source resistance and threshold voltage. Differentiation, however, exists in the noise margin in that lower tilt angle gives a higher noise margin. The design of NMOS can be approached similarly. The methodology of a decomposing body factor and source resistance may be applicable in analyzing other semiconductor devices.

## References

- [1] Rodder M, Hong QZ, Nandakumar M, Aur S, Hu JC, Chen I-C. A sub-0.18 μm gate length CMOS technology of high performance (1.5 V) and low power (1.0 V) In: Technical Digest of IEEE International Electron Devices Meeting, 1996. p. 563–66.
- [2] Hwang H, Lee D-H, Hwang JM. Degradation of MOSFETs drive current due to Halo ion implantation. In: Technical Digest of IEEE International Electron Devices Meeting, 1996. p. 567–70.
- [3] Gonzalez R, Gordon BM, Horowitz MA. Supply and threshold voltage scaling for low power CMOS. IEEE J Solid-State Circuits 1996;32:1210–16.

- [4] Park H-J, Ko PK, Hu C. A charge sheet capacitance model of short channel MOSFETs for SPICE. IEEE Trans Electron Devices 1991;10:376–87.
- [5] Hori T. A 0.1 μm CMOS technology with tilt implanted punchthrough stopper (TIPS) In: Technical Digest of IEEE International Electron Devices Meeting, 1994. p. 75–8.
- [6] Andoh T, Furukawa A, Kunio T. Design methodology for low-voltage MOSFETs. In: Technical Digest of IEEE International Electron Devices Meeting, 1994. p. 79–82.
- [7] Furukawa A, Teramoto A, Shimizu S, Abe Y, Tokuda Y. Channel profile control based on transient channel enhanced diffusion suppression by RTA for 0.18 μm single gate CMOS. In: Digest of IEEE Symposium on VLSI Technology, 1997. p. 87–8.
- [8] Yu B, Ju D-H, Kepler N, King T-J, Hu C. Gate engineering for performance and reliability in deep-submicron CMOS technology. In: Technical Digest of IEEE Symposium on VLSI Technology, 1997. p. 105–06.
- [9] Simard-Normandin M, Slaby C. Empirical modeling of low energy boron implants in silicon. J Electrochem Soc 1985;11:2218–23.
- [10] Shahidi GG, Warnock J, Acovic A, Agnello P, Blair C, Bucelot T. A high performance 0.15 μm CMOS. In: Technical Digest Symposium on VLSI Technology, 1993. p. 93–4.
- [11] Izawa R, Hure T, Takeda E. Impact of the gate-drain overlapped devices (GOLD) for deep submicrometer VLSI. IEEE Trans Electron Devices 1988;35:2088–93.
- [12] Hori A, Nakaoka H, Umimoto H, Yamashita K, Takase M, Shimizu N, Mizuno B, Odanaka S. A 0.05 μm-CMOS with ultra shallow source/drain junctions fabricated by 5 KeV ion implantation and rapid thermal annealing. In: Technical Digest of IEEE International Electron Devices Meeting, 1994. p. 583–86.
- [13] Sayama H, Kuroi T, Shirahata M, Okumura Y, Inuishi M, Miyoshi H. Low voltage operation of sub-quarter micron W-Polycide dual gate CMOS with non-uniformly

- doped channel. In: Technical Digest of IEEE International Electron Devices Meeting, 1996. p. 583–86.
- [14] TSUPREM4 users manual. California, USA: Technology Modeling Associate, 1996.
- [15] MEDICI users model. California, USA: Technology Modeling Associate, 1996.
- [16] Samudra GS, Seah BP, Ling CH. Determination of LDD MOSFET drain resistance from device simulation. Solid State Elect 1996;39:753–58.
- [17] Tsividis YP. Operation and modeling of MOS transistors. New York: McGraw-Hill, 1987.
- [18] Hofker WK. Implantation of boron in silicon. Phillip Research Reports 1975;8:1–121.
- [19] Kump MR, Dutton R. The efficient simulation of coupled point defect and impurity diffusion. IEEE Trans Comput Aided Des 1988;7:153–9.
- [20] Geiger RL, Allen PE, Strader NR. VLSI design techniques for analog and digital circuits. New York: McGraw-Hill, 1990.
- [21] Davari B. CMOS technology scaling, 0.1 μm and beyond. In: Technical Digest of IEEE International Electron Devices Meeting, 1996. p. 555–58.