Argon Ion-Implantation on Polysilicon or Amorphous-Silicon for Boron Penetration Suppression in p^+ pMOSFET

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***Abstract*—In this paper, a technique to use Ar ion-implantation on the p^+ α-Si or poly-Si gate to suppress the boron penetration in p^+ pMOSFET is proposed and demonstrated. An Ar-implantation of a dose over 5×10^{15} cm^{-2} is shown to be able to sustain 900 °C annealing for 30 min for the gate without having the underlying gate oxide quality degraded. It is believed to be due to gettering of fluorine, then consequently boron, by the bubble-like defects created by the Ar implantation in the p^+ gate region to reduce the B penetration. Excellent electrical characteristics like dielectric breakdown $(E_{\rm bd})$, interface state density $(D_{\rm it})$, and charge-to-breakdown $(Q_{\rm bd})$ on the gate oxide are obtained. The technique is compatible to the present CMOS process. The submicron pMOSFET fabricated by applying this technique exhibit better subthreshold characteristics and hot carrier immunity.**

***Index Terms*—Ar implantation, boron penetration, p^+ pMOSFET.**

I. Introduction

RECENTLY, p^+ poly-Si was recommended as the gate material for the surface-channel p-type metal-oxide-semiconductor field-effect transistor (pMOSFET) of the deep submicron complementary MOSFET to avoid short-channel effects [1]–[3]. However, the boron used to dope the poly-Si is easy to penetrate through the gate oxide to the underlying silicon. Especially, the incorporated-F due to BF_2 ion implantation in the p^+ poly-Si gate enhances boron penetration through the thin gate oxide into the Si substrate. This results in large threshold voltage shift, large charge trapping rate, degradation of p-channel inverse subthreshold and poor reliability of the devices [2]–[5]. Various techniques have been proposed to suppress the boron penetration. For examples, the amorphous Si gate [6]–[8] was suggested since it prevents the channeling effect and has a larger grain size to suppress boron diffusion, and the stacked gate [9] was recommended since it has the ability to getter F atoms at its layer boundaries to retard boron diffusion.

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In this paper, we propose and demonstrate another technique which utilizes argon implantation into the p^+ poly-Si gate to suppress the boron diffusion. It was reported previously that Ar-implantation in polysilicon or Si generates bubble-like defects [10]–[13]. We correlate this property to the gettering of fluorine and boron atoms at the damaged regions during Ar implantation into polysilicon or α-Si to suppress the boron penetration. The integrity of gate oxide is preserved and excellent electrical characteristics on the interface state density $(D_{\rm it})$, dielectric breakdown $(E_{\rm bd})$, and charge-to-breakdown $(Q_{\rm bd})$ of the gate oxide are obtained. This technique has been applied to fabricate pMOSFET and the fabricated devices show significant improvement on their subthreshold swing and hot carrier immunity.

II. Experiment

In this experiment, p^+ poly-Si gate MOS capacitors were fabricated for basic measurements for the characteristics of the gate oxide. CMOSFET's were also fabricated for which pMOSFET's had p^+ poly-Si gate. The capacitors were fabricated on the CMOSFET n-well region, which was phosphorus-implanted at 100 keV with a dose of 1×10^{13} cm^{-2} on a p-type (100) 15–25 Ω-cm Si wafer. The active region was defined by the conventional LOCOS process, where a thin oxide (≤100 Å) was grown at 920 °C in dry O_2 followed by annealing in N_2 for 20 min. 3000 Å of LPCVD α-Si was deposited at 560 °C on the top of the sample as the gate. For comparison, similar devices with polysilicon gate of the same thickness were also made. Some samples received Ar implantation of doses of 1×10^{15} cm^{-2}, 5×10^{15} cm^{-2}, and 1×10^{16} cm^{-2} at 80 keV, respectively. The projected range of Ar was about 900 Å which was much shallower than the thickness of the α-silicon gate. Then, BF_2 of a dose of 6×10^{15} cm^{-2} was implanted at 50 keV for all samples. After patterning and etching of the gate, the gate was thermally reoxidized to grow an additional 90 Å oxide over source/drain regions of the devices to prevent boron dose out-diffusion in subsequent annealing processes. Before the source/drain implantation, the wafers were annealed in a furnace at temperatures of 900 °C, 950°C, and 1000 °C in N_2 for 15 min, respectively. All the samples received annealing at 900 °C for 30 min after BPSG deposition. Al contacts were made, which were sintered at 410 °C for 30 min. The area of capacitors for breakdown measurement was 0.16×10^{-4} cm^2.

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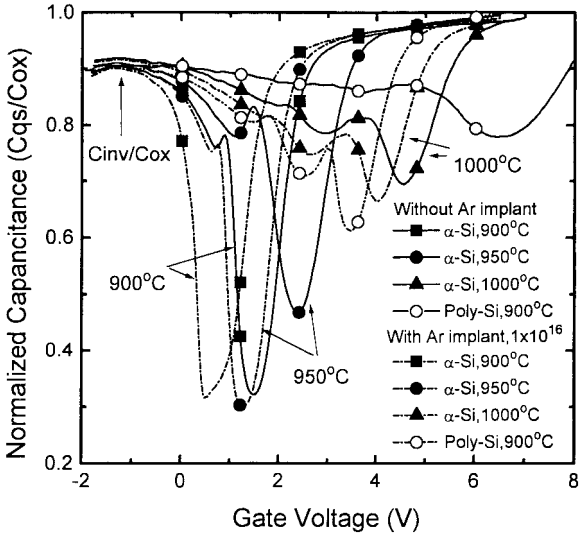


Fig. 1. The normalized quasi-static C–V result of PMOS with or without Argon implanted poly-Si gate annealed at 900 °C and α-Si gate annealed at 900, 950, or 1000 °C.

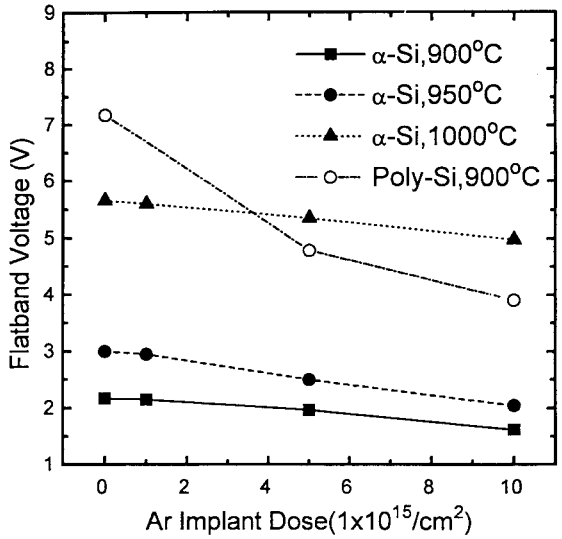


Fig. 2. The plot of the flat-band voltage ($V_{\rm fb}$) versus the dose of Ar-implanted poly-Si gate and α-Si gate.

$Q_{\rm bd}$ was measured under a constant stressing current of 100 mA/cm^2 where the n-type substrate was biased at the accumulation mode.

III. Results and Discussion

Fig. 1 shows the normalized quasi-static C–V curves of the capacitors of the α-Si gate annealed at 900, 950, and 1000 °C in N_2 for 15 min and the polysilicon gate annealed at 900 °C for 15 min, with or without Ar-implantation, respectively. The Ar-implantation dose was 1×10^{16} cm^{-2}. It can be seen that both sets of the Ar-implanted and without Ar-implanted curves shift toward right when annealing temperature is increased, and some of the high temperature curves even get distorted, indicating the boron penetration effect. However, the curves of Ar-implanted samples have less shifts than those of the sample without Ar-implant, especially for the α-Si gate for the 900 °C and 950 °C annealing curves. The curves of polysilicon gate devices have severe shifts and distortion even the annealing temperature was only 900 °C for 15 min. It was reported that the shifting and distortion were caused by the negative charges due to B-F complexes in or at the interface of the gate oxide and the shallow p^+ layer within the substrate due to boron diffusion [4], [5]. As the annealing temperature was increased to 1000 °C, however, the C–V curves of the Ar-implanted sample and without-Ar-implanted samples have serious shifts. This was because 1000 °C was so high an annealing temperature that even the Ar-implantation could not suppress the boron penetration, although the Ar-implanted sample still shows some boron suppression effect.

In Fig. 2, the flatband voltages ($V_{\rm fb}$) of the above samples after annealing are plotted as a function of dosage of Ar implanted into the α-Si gate annealed from 900 °C to 1000 °C and the poly-Si gate annealed at 900 °C. The Ar-implanted samples have lower $V_{\rm fb}$, than the samples without Ar implantation, especially for the poly-Si gate samples. Also, the higher the Ar implantation dosage, the lower the flatband voltage. For

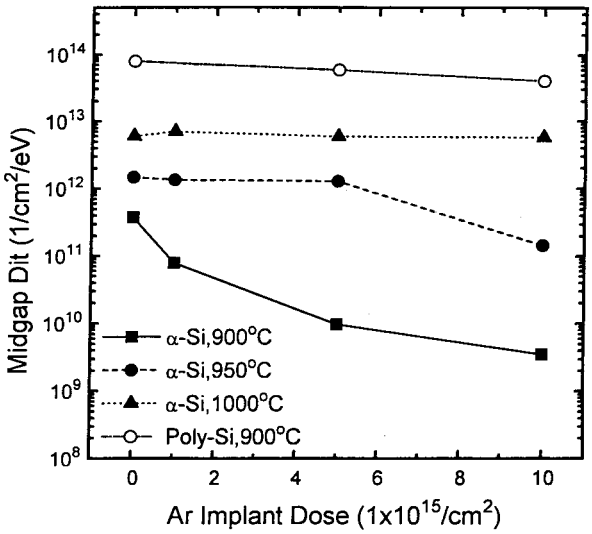


Fig. 3. The interface state density ($D_{\rm it}$) plotted with the dose of Argon implanted into poly-Si gate annealed at 900°C and α-Si gate annealed at 900, 950, or 1000 °C.

the α-Si gate samples, the Ar implantation has good suppression effect for the annealing temperature from 900 °C to 950 °C. For the annealing temperature of 1000 °C, there still show some suppression effect for the Ar-implantation, although, as mentioned previously, 1000 °C is too high an annealing temperature to make the suppression effect significant.

Fig. 3 shows the midgap interface state density ($D_{\rm it}$) versus the Ar-implanted dosage of the above samples. The interface state density was extracted by using the quasi-static and high-frequency C–V technique. From the figure, it is seen that $D_{\rm it}$ increased with the annealing temperature, indicating that boron penetration existed and became severe at the higher temperature. On the other hand, $D_{\rm it}$ decreased with the Ar-implant dosage, indicating that Ar-implantation improved $D_{\rm it}$ through suppressing boron penetration. Also it is seen that Ar-implantation can make the α-Si gate to sustain the 900 °C

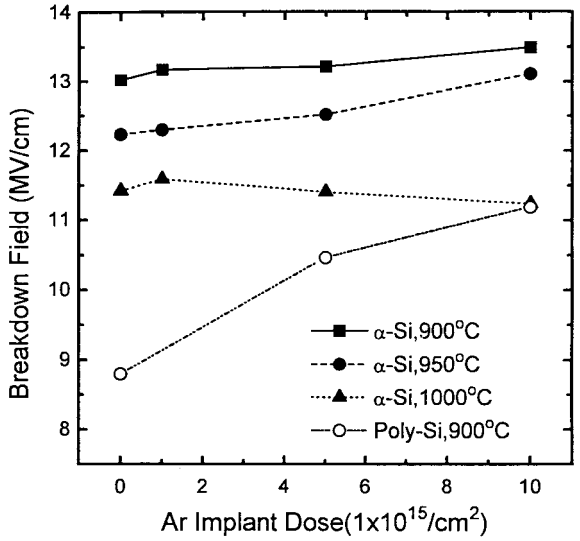


Fig. 4. The plots of the dielectric breakdown $(E_{\rm bd})$ versus the dose of Ar-implanted poly-Si gate or α-Si gate capacitor with the gate oxide thickness of about 100 Å.

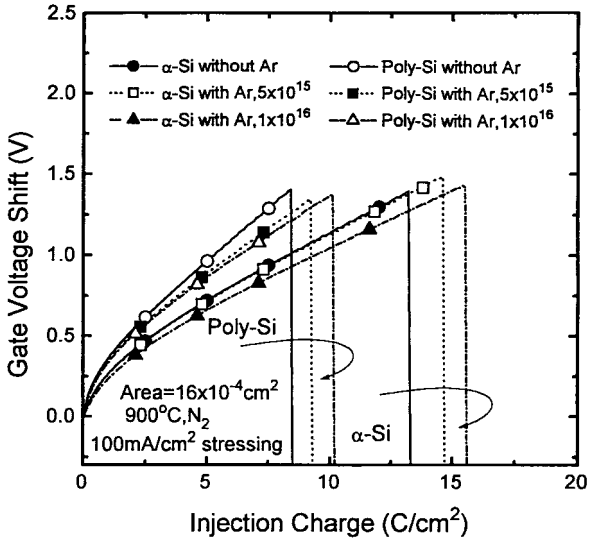


Fig. 5. The gate voltage shift (ΔV_g) under 100 mA/cm^2 stress for Ar-implanted or without Ar-implanted poly-Si gate and α-Si gate material. The capacitor area was 0.16×10^{-4} cm^2.

TABLE I
ELECTRICAL THICKNESS OF GATE OXIDES MEASURED FROM C–V CURVES

Oxide thickness by C-V(Å)	α-Si			poly-Si
Annealing temperature	900℃	950℃	1000℃	900℃
Without Ar-implant	**103**	**106.4**	**107**	**110**
With Ar-implant (1×10^{15}/cm^2)	**102.8**	**103.9**	**106.7**	-
With Ar-implant (5×10^{15}/cm^2)	**101.9**	**103.1**	**104.3**	**106**
With Ar-implant (1×10^{16}/cm^2)	**101.5**	**101.7**	**102.8**	**103**

annealing without having its oxide/Si substrate interface degraded. For the 1×10^{16} cm^{-2} implanted dose, the $D_{\rm it}$ can even be kept at the level of 1.0×10^{10}/cm^2/eV after 900 °C, 15 min annealing.

Fig. 4 shows the dielectric breakdown $(E_{\rm bd})$ with respect to the Ar-implantation dosage for various annealing temperatures. The gate oxide thicknesses used for estimating $E_{\rm bd}$ of samples are listed in Table I. All $E_{\rm bd}$'s increase with the Ar-implantation dosage for all the annealing temperatures except the 1000 °C α-Si gate samples. For the α-Si gate samples with 900 °C 15 min annealing can have $E_{\rm bd}$ above 13 MV/cm. For the poly-Si gate samples, the Ar-implantation has increased their $E_{\rm bd}$ dramatically.

The thicknesses of the gate oxides were measured both by ellipsometry and by C–V curves. The thickness measured by ellipsometry was 93 ± 2 Å and the electrical thicknesses measured by C-V curves are listed in Table I. The electrical thicknesses were extracted at $V_g - V_{\rm fb}, = 5$ V in the accumulation region of MOS capacitors. For the samples without Ar-implantation, the electrical thicknesses were slightly larger and the higher the annealing temperature, the larger the oxide thickness. Also, the poly-Si samples had the largest electrical oxide thickness. This can be explained by fluorine gettering of Ar-implantation through the "bubble effect," which will be shown and explained in a latter paragraph and TEM pictures. Due to gettering of fluorine in poly gates by Ar implantation for the Ar-implanted samples, their gate oxides had a lower fluorine concentration. It was reported that oxides incorporating fluorine have higher thicknesses [14], [15]. The less fluorine in the oxides resulted in less thicknesses for the Ar-implanted samples. For the poly-Si samples, since were most susceptible to the boron diffusion, they had the highest fluorine concentration in their oxides and they had the largest oxide thicknesses.

Fig. 5 shows the gate voltage shifts (ΔV_g) of the α-Si gate and polysilicon gate samples with and without Ar-implantation, respectively, when they were subjected to a 100 mA/cm^2 constant current stress. These samples were annealed at 900 °C for 15 min. The n-type substrate was biased at accumulation mode during $Q_{\rm bd}$ measurement. In the figure, the α-Si gate samples have small trapping rates and larger $Q_{\rm bd}$'s than those of the polysilicon gate samples. For both gates, the Ar-implanted samples have larger $Q_{\rm bd}$'s as compared to the samples without Ar-implantation, and the larger the Ar-implantation, the larger $Q_{\rm bd}$. Fig. 6 compiles the plots of the $Q_{\rm bd}$'s of all samples annealed at different temperatures under the constant current stressing of 100 mA/cm^2. The $Q_{\rm bd}$ increases with the Ar dosage for all the samples except the α-Si gate samples annealed at 1000 °C.

The above data show that the degradation of oxide was remarkably suppressed by the Ar implantation, when its dose was above 5×10^{15} cm^{-2}, into the α-Si gate for the 900 and 950 °C annealing, or the poly-Si gate for the 900 °C annealing.

Fig. 7 shows the sheet resistance as a function of the dose of Ar implanted into the α-Si annealed from 900 °C to 1000 °C and the poly-Si annealed at 900 °C. For all samples, sheet resistances increase by about 16% as samples receive Ar-implantation of a dosage of 1×10^{15} cm^{-2}, then sheet resistances stay basically constant even the dosage of the Ar-implantation increases to 1×10^{16} cm^{-2}. This increase in sheet resistances indicates that the active doping concentration of boron might have decreased with the Ar-implantation or the additional implanted Ar in the α-Si or the poly-Si gates served as scattering impurity to current conduction. This may create

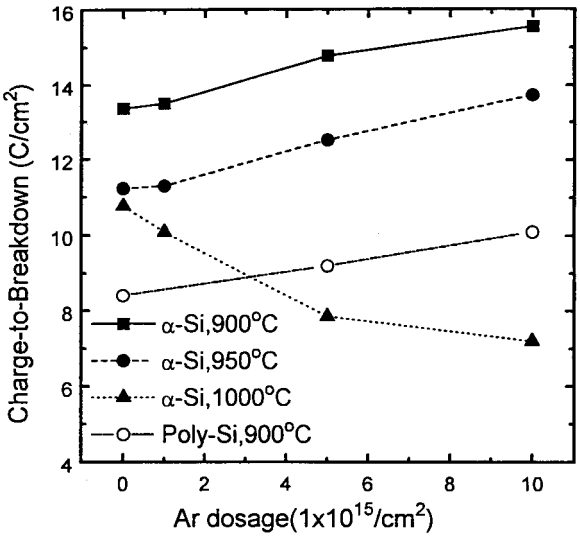


Fig. 6. The plots of the charge-to-breakdown ($Q_{\rm bd}$) versus the dose of Ar-implanted poly-Si gate or α-Si gate capacitor. The stressing current density was 100 mA/cm^2 in accumulation mode.

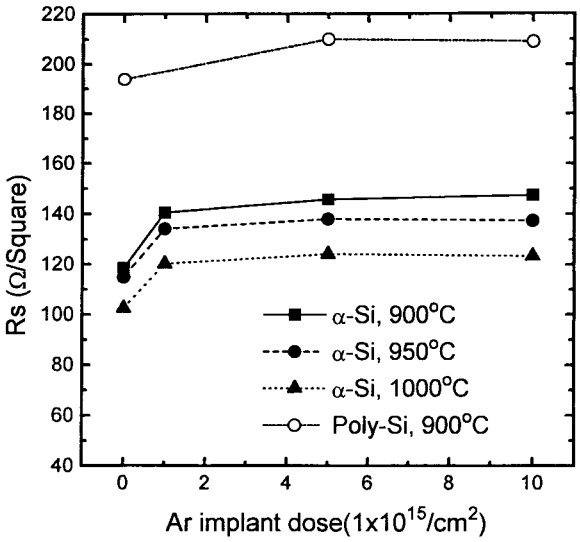
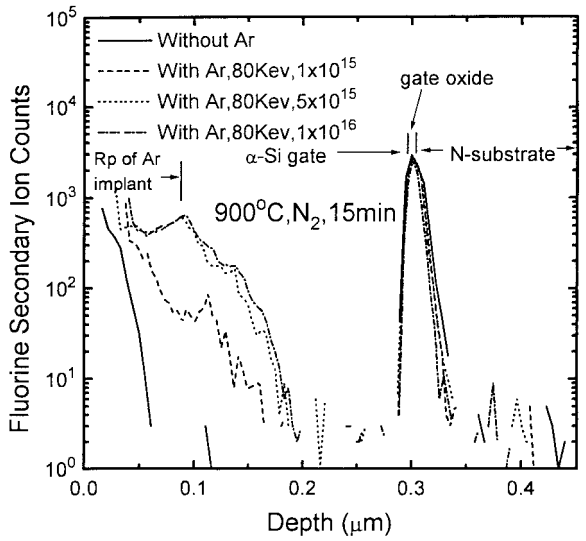
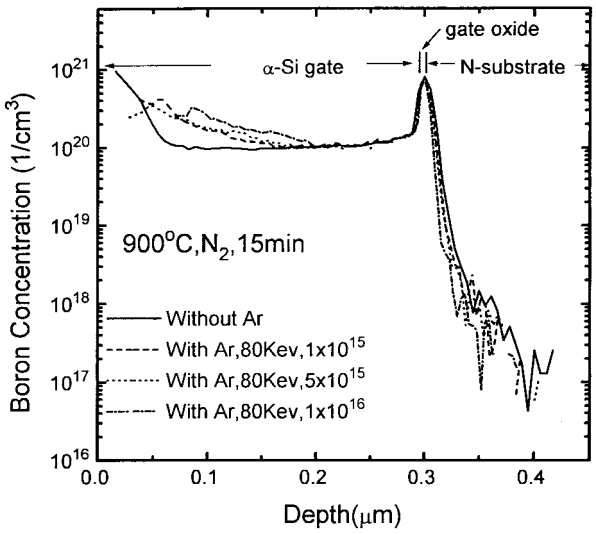


Fig. 7. Sheet resistivity as a function of the dose of Ar into α-Si annealed from 900 °C to 1000 °C or poly-Si annealed at 900 °C.



(a)

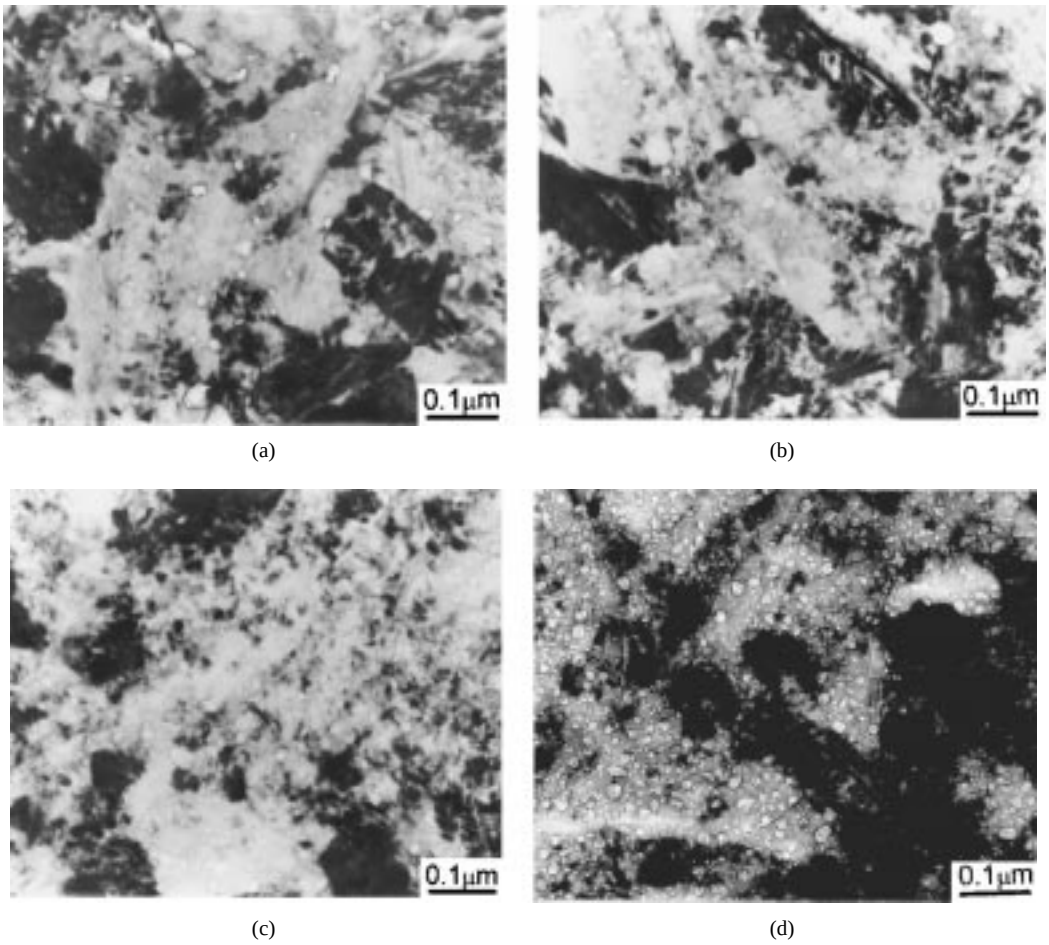


(b)

Fig. 8. The SIMS profiles of (a) fluorine and (b) boron of the α-Si gate PMOS capacitor annealing at 900 °C.

the gate depletion problem for the MOS device. However, as seen from the C–V curves of Fig. 1, the ratios of $C_{\rm inv}/C_{\rm ox}$ are almost the same for both sample with Ar-implant and without Ar-implant for both α-Si or poly-Si gate devices. The Ar-implantation did not seem to create a more serious gate depletion problem as compared with the un-implanted samples. In addition, it is mentioned that the sheet resistances of poly-Si gate samples are higher than those of the α-Si gate samples for all annealing conditions in this figure.

Fig. 8(a) and (b) shows fluorine and boron SIMS profiles, respectively, for the α-Si gate samples with and without Ar-implantation. The samples were annealed at 900 °C in N_2 for 15 min. For the Ar-implanted samples, fluorine atoms tend to segregate at the Ar-implant damaged region which is about 900 Å of the projected Ar implantation distance. The peak of the segregated fluorine increases as the Ar implant dose increases, consequently, leading to decrease of the fluorine peak at the gate oxide. Obviously, the Ar implantation into poly-Si or α-Si gate had acted as a sink for fluorine atoms, thus reduced the fluorine atoms in gate oxide film. Since the F in the gate oxide would enhance the boron penetration, the α-Si gate with Ar implantation with less fluorine in it had a less boron penetration. It can be seen in Fig. 8(b) that Ar-implanted samples have higher boron peaks at Rp on the α-Si gate and a shallower profile in the underlying silicon substrate than that of the control sample. In addition, on the Ar-implanted curves, it is noted that there is no obvious decrease of boron concentration in the region just above the oxide in the α-Si gate. This is consistent with the observation of the C–V curves of Fig. 1, where the $C_{\rm inv}/C_{\rm ox}$ of the C–V curves are almost the same for the Ar-implanted samples and the without Ar-implanted samples. This also suggests that the sheet resistance increase of the Ar-implaned samples might be caused by the impurity scattering of the implanted Ar atoms.



(a) (b)

(c) (d)

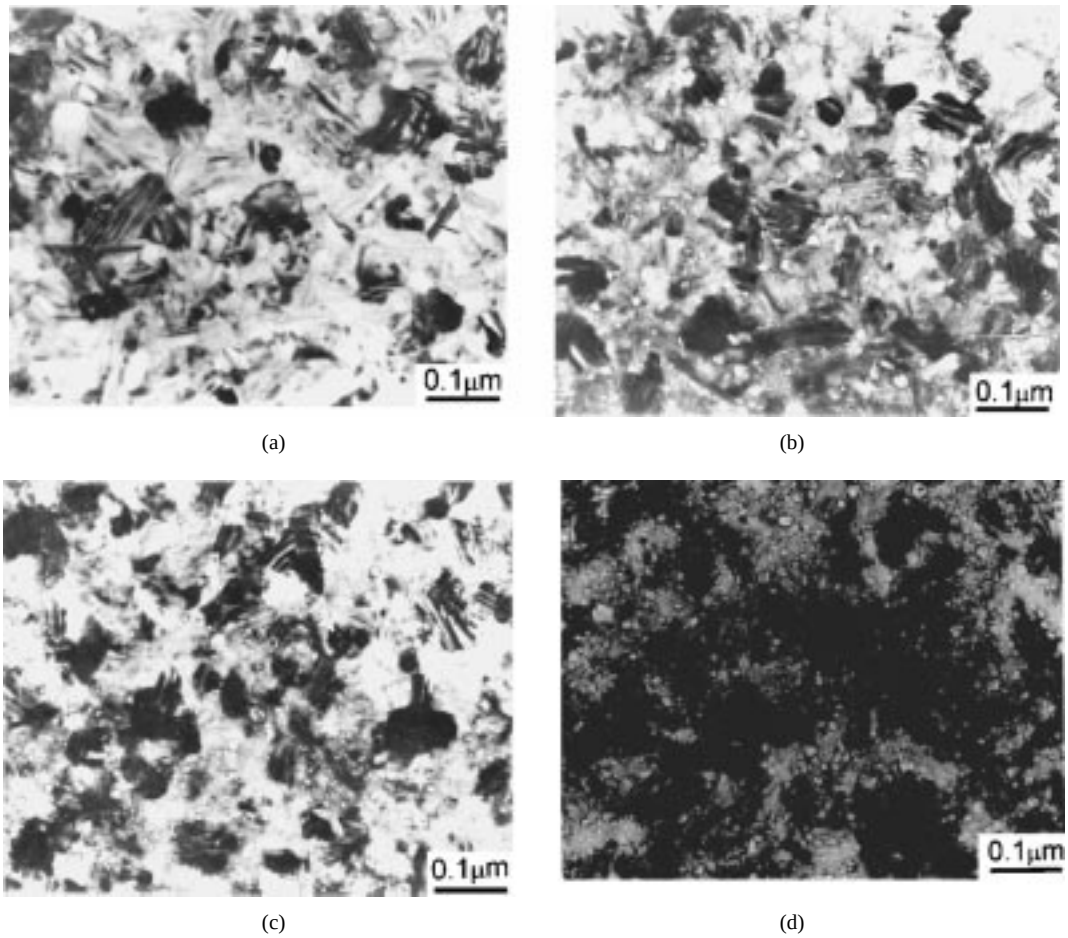
Fig. 9. The planar-view TEM of the gate material with or without Ar implant annealed at 900°C: (a) α-Si without Ar, (b) α-Si with Ar, 1×10^{15} cm^{-2}, (c) α-Si with Ar, 5×10^{15} cm^{-2}, (d) α-Si with Ar, 1×10^{16} cm^{-2}.

Fig. 9(a)–(d) shows the planar-view TEM pictures of the α-Si gate samples without Ar-implantation and with Ar-implantation of various doses annealed at 900 °C in an N_2 ambient, respectively. Fig. 10(a)–(d) shows the similar TEM pictures but for the poly-Si samples. From the pictures, it is seen that the α-Si gate samples have larger grain sizes than those of the poly-Si gate samples but for both groups of samples, the grain sizes of the Ar-implanted samples are the same as that of the sample without Ar-implantation. However, it is observed that there are bubble-like defects on the α-Si gate samples and the more the Ar-implantation, the more the defects. For the sample without Ar-implantation, it has the lowest bubble density, about 4×10^{10} cm^{-3}, but has the largest bubble size, about 80 Å up to 600 Å. For the Ar-implanted sample of the dose of 1×10^{16} cm^{-2}, it has the largest density, about 7×10^{11} cm^{-2}, but the smallest bubble size, about 30 Å–300 Å. For the poly-Si gate samples, no bubble is observed for the sample without Ar ion-implantation as shown in Fig. 10(a), and for the Ar-implanted samples, bubbles are observed but with less densities than the corresponding counterparts of the α-Si gate samples of the same doses. Table II summarizes the bubble size/density in terms of the Ar implantation dose for both α-Si gate and poly-Si gate samples. From the figures and the table, it could be suspected that these bubble-like defects have correlation with the suppression capability of samples. It is believed that these bubble-like defects behaved like gettering centers for the implanted fluorine, which in turn resulted in suppression of boron diffusion. The more the implanted Ar, the more the bubble defects, and the more the suppression effect.

TABLE II
THE CORRELATION BETWEEN BUBBLE DENSITY/SIZE AND AR IMPLANT DOSE

	Ar implant Dose($1/cm^2$)	0	1×10^{15}	5×10^{15}	1×10^{16}
α-Si	Bubble density($1/cm^2$)	4×10^{10}	2.7×10^{11}	4.7×10^{11}	7×10^{11}
	Bubble size(Å)	80-600	30-400	30-400	30-300
poly-Si	Bubble density($1/cm^2$)	None	2.1×10^{11}	3.4×10^{11}	5.2×10^{11}
	Bubble size(Å)	None	25-125	25-125	25-125

To investigate the phenomenon that the Ar-implanted sample annealed at 1000 °C did not show too much boron suppression effect, the TEM pictures for the sample were also taken. They are shown in Fig. 11. Fig. 11(a) shows the planar-view TEM picture of the α-Si gate sample with an Ar-implant of 5×10^{15} cm^{-2} annealed at 1000 °C. The sample has bubbles of larger size but lower density than those of the sample annealed at 900 °C. This larger bubble size but lower density was the result of the poly grain regrowth at the higher temperature of 1000 °C. Fig. 11(b) and (c) shows



(a) (b)

(c) (d)

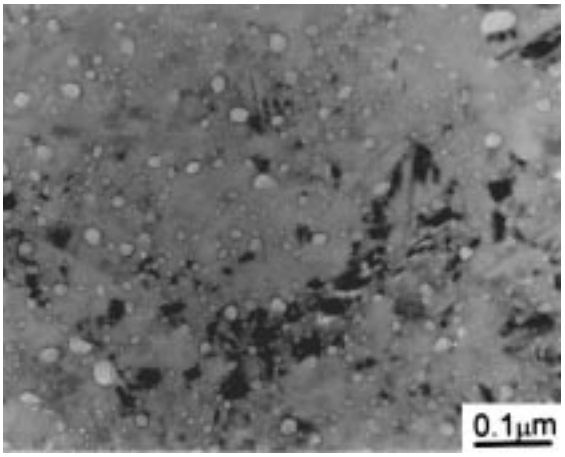
Fig. 10. The planar-view TEM of the gate material with or without Ar implant annealed at 900 °C: (a) poly-Si without Ar, (b) poly-Si with Ar, 1×10^{15} cm^{-2}, (c) poly-Si with Ar, 5×10^{15} cm^{-2}, and (d) poly-Si with Ar, 1×10^{16} cm^{-2}.

the cross-sectional TEM pictures of the α-Si gate samples with Ar-implant dose of 5×10^{15} cm^{-2} annealed at 900 °C and 1000 °C, respectively. The 1000 °C-annealed sample has grains of larger size than that of the 900 °C-annealed sample. This bubble regrowth phenomenon had also been reported and discussed by references [11], [16]. This larger size but lower density bubbles explains the decreased boron suppression ability for the sample annealed at 1000 °C. At the same time, the larger grains of the α-Si gate also resulted in larger stress on the gate oxide. This in addition degraded the oxide characteristics like $Q_{\rm bd}$, $E_{\rm bd}$, and $D_{\rm it}$, as shown in previous data.

Fig. 12 shows the threshold voltage shifts of the pMOSFET's ($W = 10$ um), made with the p^+ α-Si gate, without and with Ar-implantation, as a function of the gate length after annealing at 900 °C in N_2. It is a plot showing the short channel effect of these devices. On the plots, the more the Ar-implantation, the more negative the $V_{\rm th}$ and the less the short channel effect are observed. For the devices of the Ar-implantation of the doses above 5×10^{15} cm^{-2}, their $V_{\rm th}$ even become negative for the channel length less than 1 um. Since, the boron penetration reduces the channel doping, making the short channel effect more significant, this strongly indicates that Ar-implantation reduces the boron diffusion in the gate of the devices.

Fig. 13 shows the measured subthreshold characteristics of the same pMOSFET's. Similarly, the more the Ar-implantation, the better the off and the subthreshold characteristics of the devices, and the device without Ar-implantation has the poorest characteristics. For example, for the devices without the Ar-implant, the subthreshold swing is 112 mv/dec., but for the devices of the Ar-implant of a dose of 1×10^{16} cm^{-2}, it is reduced to be 96 mv/dec. This is because the increases of unannealed-out interface state [4] and the more acceptor type of charges in the underlying channel due to boron penetration diffusion, resulted in more subthreshold swings. For the samples with Ar implantation, the above effects became less serious.

Fig. 14 shows the hot carrier effect of the same above samples, for which their threshold voltage shifts are plotted with their stressing gate voltage $(V_g - V_{\rm th})$. During stressing, the samples were biased at a drain voltage of $V_d = -6$ V for 10 min. Since for a fixed drain voltage, if the gate stressing voltage varies from 5 V to -5 V, the gate current increases first and then decreases due to the fact that the drain-gate field increases and then decreases, the stressing gate voltage for each sample was chosen to be the value which gave the maximum gate current in order to obtain the maximum stressing. These gate voltages and maximum gate currents for various Ar implant doses are listed in Table III. In the



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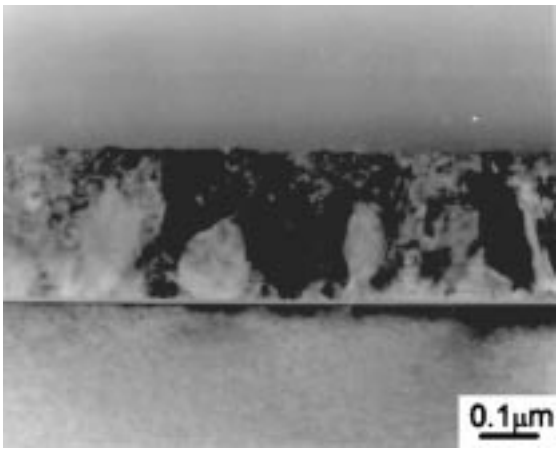

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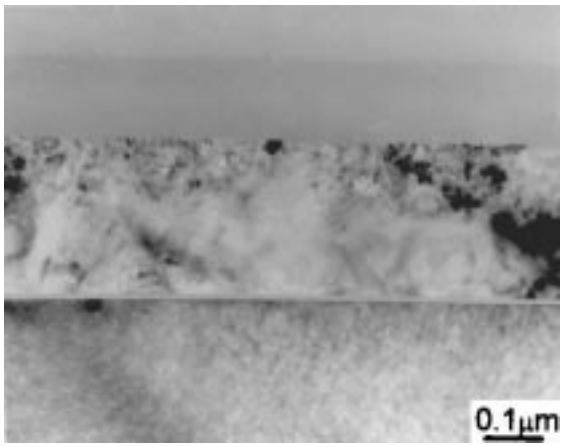

(c)

Fig. 11. (a) The planar-view TEM of α-Si gate with Ar, 5×10^{15} cm^{-2} annealed at 1000 °C, (b) the cross section TEM of α-Si gate with Ar, 5×10^{15} cm^{-2} annealed at 900 °C, and (c) the cross section TEM of α-Si gate with Ar, 5×10^{15} cm^{-2} annealed at 1000 °C.

plots of Fig. 14, $V_{\rm th}$ shift decreases with the Ar-implantation dosage. The maximum $V_{\rm th}$ shift for the sample without Ar implantation is approximately 140 mV, but is only 82 mV for the sample with the Ar-implant of a dose of 1×10^{16} cm^{-2}. This again shows that the Ar-implantation improves the hot carrier susceptibility of pMOSFET. This result is easily

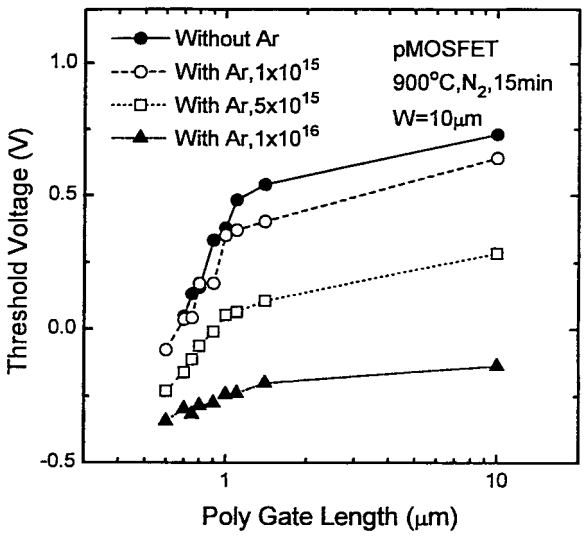

Fig. 12. Threshold voltage of pMOSFET as a function of gate length with various dose of Ar implantation.

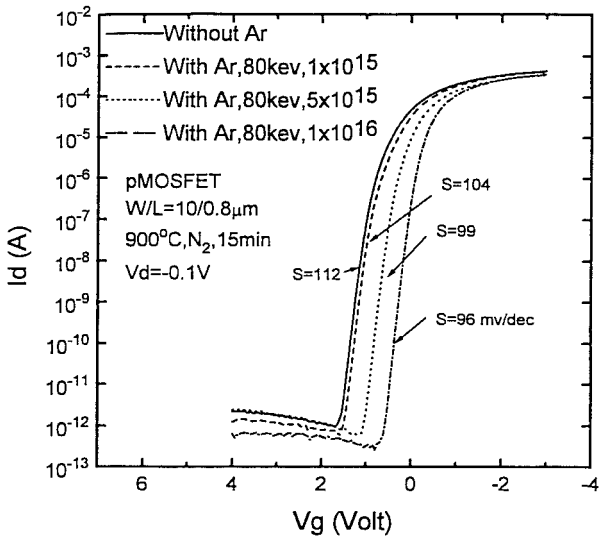

Fig. 13. Subthreshold characteristics of p^+ pMOSFET by Ar ion-implantation into α-Si with various dose at 900 °C.

explained since the Ar-implanted devices have an improved gate oxide quality as compared to that of the devices without Ar-implantation.

Hence, all the above data of Figs. 13 and 14 show that the device performance such as the subthreshold swing and the hot carrier immunity was improved by the Ar implantation, especially for the dose above 5×10^{15} cm^{-2}.

IV. Conclusion

In this paper, we have reported and demonstrated that Ar implantation into the α-Si gate or the poly-Si gate can preserve the integrity of the gate oxide of pMOSFET. The preservation is believed to be due to gettering of fluorine in the gate by the bubble-like defects which are created by the Ar-implantation. The gettering of fluorine, at the same time, getters boron in the gate, leading to suppression of boron diffusion. As a

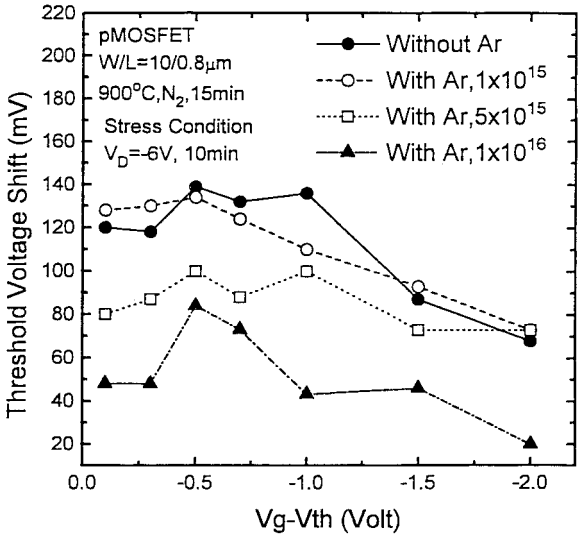

Fig. 14. Hot-carrier induced threshold voltage shift of the sample as a function of stress gate voltage under stress condition of $V_d = -6$ V, 10 min.

TABLE III
MAXIMUM GATE CURRENTS AND THEIR APPLIED GATE VOLTAGES FOR VARIOUS Ar IMPLANT DOSES

Ar implant Dose(1/cm^2)	0	1×10^{15}	5×10^{15}	1×10^{16}
Maximum gate current, Ig(nA)	4.45	3.41	3.12	2.78
Gate Voltage for Maximum Ig (V)	-0.1	-0.21	-0.35	-0.48

result, smaller $V_{\rm fb}$ shift, lower $D_{\rm it}$, larger $E_{\rm bd}$ and $Q_{\rm bd}$, are obtained as compared to the conventional devices of the same α-Si gate, or the poly-Si gate, when they are annealed at 900 or 950 °C. As a consequence, the device performance, such as the subthreshold swing and the hot carrier immunity are improved.

This Ar-implantation can be readily integrated into the present CMOS process. It can be considered to be an easy, yet, effective way to improve the performance of the p$^+$ gate pMOSFET.

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