Characterization of Various Stress-Induced Oxide Traps in MOSFET's by Using a Subthreshold Transient Current Technique

Tahui Wang, *Senior Member, IEEE*, Lu-Ping Chiang, Nian-Kai Zous, Tse-En Chang, and Chimoon Huang

***Abstract*—An oxide trap characterization technique by measuring a subthreshold current transient is developed. This technique consists of two alternating phases, an oxide charge detrapping phase and a subthreshold current measurement phase. An analytical model relating a subthreshold current transient to oxide charge tunnel detrapping is derived. By taking advantage of a large difference between interface trap and oxide trap time-constants, this transient technique allows the characterization of oxide traps separately in the presence of interface traps. Oxide traps created by three different stress methods, channel Fowler–Nordheim (F–N) stress, hot electron stress and hot hole stress, are characterized. By varying the gate bias in the detrapping phase and the drain bias in the measurement phase, the field dependence of oxide charge detrapping and the spatial distribution of oxide traps in the channel direction can be obtained. Our results show that 1) the subthreshold current transient follows a power-law time-dependence at a small charge detrapping field, 2) while the hot hole stress generated oxide traps have a largest density, their spatial distribution in the channel is narrowest as compared to the other two stresses, and 3) the hot hole stress created oxide charges exhibit a shortest effective detrapping time-constant.**

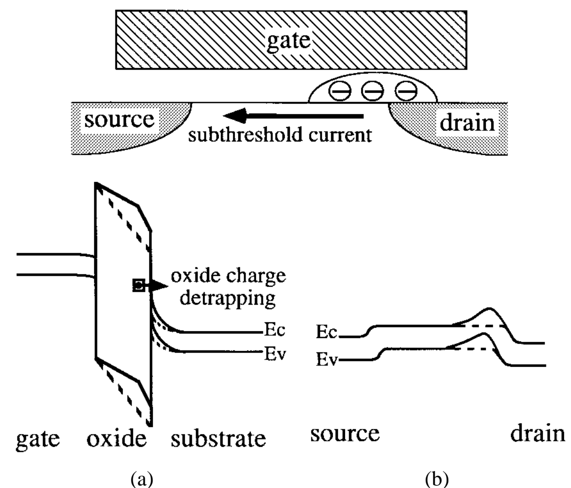

Fig. 1. (a) Illustration of trapped electron tunneling through a trapezoidal barrier in the detrapping phase and (b) surface potential barrier lowering in the subthreshold current measurement phase due to oxide electron detrapping. The solid line and the dashed line represent the band diagrams before and after oxide electron detrapping, respectively.

I. Introduction

OXIDE trap creation due to bias stress in program/erase cycles has been recognized as a major reliability concern in the flash EEPROM technology [1]–[3]. Various reliability issues such as stress induced leakage current (SILC) [4] and programming current degradation [5] are related to oxide trap generation. Previous studies have shown that stress generated oxide traps can be easily charged and discharged [6]. Device instabilities resulting from oxide charge trapping/detrapping such as time-dependent gate current [7], subthreshold current [8] and GIDL current [9], [10] at a DC bias have been reported. Previously, stress induced oxide traps were usually characterized by monitoring a threshold voltage shift. Since both interface trap and oxide trap have the same charge effect on threshold voltage, the presence of interface charge may complicate the characterization and interpretation of oxide trap effects. Recently, a modified charge pumping (CP) technique has been developed to circumvent this difficulty [11]. Although the CP method is able to measure oxide traps as well as interface traps simultaneously, a precise determination of oxide trap density requires the knowledge about the interface trap polarities (donor-like or acceptor-like) [12].

Despite the same charge effect on threshold voltage, interface traps and oxide traps are distinguished by a large difference in their time-constants. By taking advantage of the time-constant separation, we proposed a transient GIDL technique to monitor oxide trap discharging [9], [10]. The unique advantage of this technique is to allow a direct and continuous observation of charge exchange between oxide traps and the Si substrate. However, since band-to-band tunneling is confined to a certain range of substrate doping in the n-type drain [13], the GIDL method cannot be utilized to probe oxide traps in the channel region or to profile an oxide trap spatial distribution.

Unlike GIDL current, subthreshold current flows through the entire channel (Fig. 1) and potentially can be used to detect traps in the channel region. Bourcerie *et al.* reported a subthreshold current transient arising from the variation of oxide trapped charge [8]. In their measurement, the device must be biased in the subthreshold region in oxide charge detrapping. Due to a small positive oxide field in the subthreshold region,

Manuscript received July 15, 1997; revised March 30, 1998. The review of this paper was arranged by Editor J. M. Vasi. This work was supported by the National Science Council, R.O.C., under Contract NSC86-2215-E009-035.

T. Wang, L.-P. Chiang, and N.-K. Zous are with the Department of Electronics Engineering, Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

T. E. Chang was with National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. He is now in military service.

C. Huang is with the Technology Development Department, Macronix Co., Hsinchu 300, Taiwan, R.O.C.

Publisher Item Identifier S 0018-9383(98)05395-7.

0018–9383/98$10.00 © 1998 IEEE

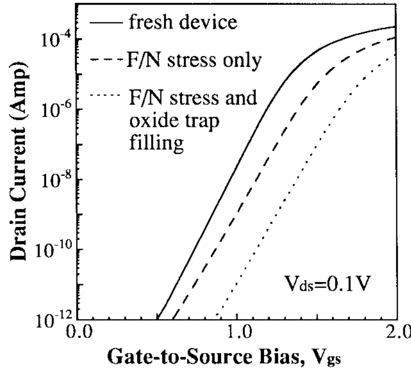

Fig. 2. The I_{ds}–V_{gs} characteristics before and after F–N stress. Stress condition: $V_{gs} = 9.5$ V for 800 s. Filling condition: $V_{gs} = 2.5$ V and $V_{bs} = -7$ V for 100 s.

only trapped oxide electrons near the poly-gate can be removed via tunneling. In this work, we propose a transient oxide trap characterization technique including two alternating phases; One is an oxide charge detrapping phase and the other is the subthreshold current measurement phase. The principle of this technique is illustrated in Fig. 1. The band diagrams in the detrapping phase and in the measurement phase are drawn in Fig. 1(a) and (b). In the detrapping phase, an applied negative gate bias causes trapped oxide electrons to tunnel to the Si substrate. As a result of negative charge detrapping, not only the surface field in the vertical direction but also the potential barrier in the lateral direction reduces [dashed lines in Fig. 1(a) and (b)]. Consequently, the subthreshold current increases after each detrapping phase. By monitoring the evolution of the subthreshold current with cumulative detrapping time, the escaping oxide charge density can be deduced. Furthermore, by varying the gate bias in the detrapping phase and the drain bias in the measurement phase, the detrapping oxide field and the position of the maximum surface barrier are modulated, respectively. Thus, the field dependence of oxide charge detrapping and the spatial distribution of oxide traps can be obtained by using this technique.

In measurement, a conventional source/drain n-MOSFET with 100 Å gate oxide, 0.6 μm gate length, and 20 μm gate width was used. Three bias stress conditions which may occur in flash EEPROM operation are studied: 1) channel Fowler–Nordheim (F–N) stress; 2) hot electron (HE) stress; and 3) hot hole (HH) stress. The stress biases are $V_{gs} = 9.5$ V and $V_{ds} = 0$ V for the F–N stress, $V_{gs} = 6.5$ V and $V_{ds} = 5$ V for the HE stress, and $V_{gs} = -5$ V and $V_{ds} = 5$ V for the HH stress. After stress, substrate hot electron injection at $V_{gs} = 2.5$ V and $V_{bs} = -7$ V was performed to fill the generated oxide traps with electrons. A gate current about several picoamperes was measured in trap filling. The step of oxide trap filling is important since only the charged traps can be detected by an electrical measurement such as subthreshold current measurement. The effect of oxide trap filling is exemplified in Fig. 2 where the solid line is the pre-stress I_{ds}–V_{gs}, the dashed line is the I_{ds}–V_{gs} measured immediately after the F–N stress and the dotted line represents the result after the oxide trap filling. The trap filling effect is demonstrated by the rightward shift of the I_{ds}–V_{gs} curve.

II. Modeling of a Subthreshold Current Transient

The dependence of subthreshold current on a gate bias is expressed as follows [14]:

$$I_d = I_o \exp(S(V_{gs} - V_{fb})) \tag{1}$$

where V_{fb} is flat-band voltage and S is the slope of the subthreshold current. The relationship between S and temperature is approximated by [14]

$$S = q/nkT \tag{2}$$

where the parameter n can be evaluated directly from the I_{ds}–V_{gs} in a measured device.

The stress generated oxide charges are assumed to have a distribution $Q_{ox}(x)$ in the vertical direction and the corresponding detrapping time-constant is $\tau(x)$. x is the distance from the trapped charge to the Si/SiO$_2$ surface. The oxide charge detrapping rate is

$$\frac{dQ_{ox}(x,t)}{dt} = -\frac{Q_{ox}(x,t)}{\tau(x)} \tag{3}$$

and

$$Q_{ox}(x,t) = Q_{ox}(x,0)\exp(-t/\tau(x)). \tag{4}$$

As a result, the change of flat-band voltage due to oxide charge detrapping is

$$V_{fb}(t) = V_{fb}(0) + \int_0^{t_{ox}} \frac{t_{ox} - x}{\epsilon_{ox}} \times Q_{ox}(x,0)(1 - \exp(-t/\tau(x)))\,dx \tag{5}$$

where t_{ox} is the gate oxide thickness. Substituting (2) and (5) into (1), we arrive at

$$\ln(I_d(t)) = \ln(I_d(0)) - \int_0^{t_{ox}} \frac{q}{nkT}\frac{t_{ox} - x}{\epsilon_{ox}} \times Q_{ox}(x,0)(1 - \exp(-t/\tau(x)))\,dx \tag{6}$$

where the integral term stands for the magnitude of a subthreshold current transient and is inversely proportional to temperature. Since subthreshold current exhibits an exponential dependence on oxide charge, a small change of oxide charge can result in a significant variation of a subthreshold current. The escaping oxide charge Q_{eff} in the measurement period therefore can be evaluated from the evolution of a subthreshold transient as follows:

$$\begin{aligned} Q_{eff} &= \int_0^{t_{ox}} \frac{t_{ox} - x}{t_{ox}}(Q_{ox}(x,0) - Q_{ox}(x,t)) \\ &= -(nkT\epsilon_{ox}/qt_{ox})\ln(I_d(t)/I_d(0)) \end{aligned} \tag{7}$$

where Q_{eff} is defined as the equivalent areal oxide charge density at the Si/SiO$_2$ surface. It should be pointed out that in case both interface traps and oxide traps are present, (6) still holds except that the parameter n should be replaced by the interface trap degraded n.

The relationship between the trap time-constant τ and the trap position x is determined by an oxide field and the trap energy. For example, if the oxide field is large and the trap energy is relatively small, trapped electrons escape through

a triangular barrier. By assuming a single trap energy and neglecting a local distortion of the electric field due to the trapped charge, the electron tunneling time is given by [15]

$$\tau = \tau_o \exp\left(\frac{4\sqrt{2m^*}}{3\hbar q E_{\rm ox}} E_t^{3/2}\right) \tag{8}$$

where τ_o is the tunneling characteristic time, E_t is the electron trap energy measured from the conduction band, $E_{\rm ox}$ is the oxide field, and other variables have their usual definitions. In this case, the trap time-constant τ is independent of x and the subthreshold current transient becomes a double exponential function of time, i.e.,

$$\ln(I_d(t)) = \ln(I_d(0)) - \frac{q t_{\rm ox}}{nkT\epsilon_{\rm ox}} Q_{\rm eff}(1 - \exp(-t/\tau)). \tag{9}$$

On the other side, if the trap energy is large and the oxide field is small, trapped oxide electrons tunnel to the Si substrate through a trapezoidal barrier. $\tau(x)$ is then given by [15]

$$\tau(x) = \tau_o \exp\left(\frac{4\sqrt{2m^*}}{3\hbar q E_{\rm ox}}\left[E_t^{3/2} - (E_t - qE_{\rm ox}x)^{3/2}\right]\right) \simeq \tau_o \exp(\alpha x) \tag{10}$$

with

$$\alpha = 2\left(2m^* E_t/\hbar^2\right)^{1/2}.$$

Following the derivation in [10], the time-dependence of a subthreshold current transient is obtained in the following:

$$\ln(I_d(t)) = \ln(I_d(0)) - \int_0^{t_{\rm ox}} \frac{q}{nkT}\frac{t_{\rm ox}-x}{\epsilon_{\rm ox}} Q_{\rm ox}(x,0) \times \left(1 - \exp\left(-\frac{t}{\tau_o}\exp(-\alpha x)\right)\right) dx \simeq \ln(I_d(0)) - \frac{q t_{\rm ox}}{nkT\epsilon_{\rm ox}} \int_0^{\alpha^{-1}\ln(t/\tau_o)} \frac{t_{\rm ox}-x}{t_{\rm ox}} \times Q(x,0)\, dx. \tag{11}$$

By neglecting the term $\frac{t_{\rm ox}-x}{t_{\rm ox}}$ and assuming a uniform oxide charge distribution, it can be shown that the subthreshold current transient follows a power law time-dependence

$$I_d(t) \propto t^p \quad \text{with } p = -\frac{q t_{\rm ox} Q_{\rm ox}}{nkT\alpha\epsilon_{\rm ox}}. \tag{12}$$

The power factor p is positive for electron detrapping. It should be mentioned that by taking into account the second-order field effect in (10), the power factor becomes slightly dependent on oxide field and increases with it.

III. Results and Discussions

A. Time-Dependence of a Subthreshold Transient

Fig. 3 shows the measured pre-stress and post-stress (after filling) subthreshold currents in three measurement/detrapping cycles. The biases are $V_{\rm gs} = 1.2$ V and $V_{\rm ds} = 0.1$ V in the measurement phase and $V_{\rm gs} = -7$ V and $V_{\rm ds} = 0$ V in the detrapping phase. The corresponding oxide field in the detrapping phase is about 6.0 MV/cm. Notably, the pre-stress

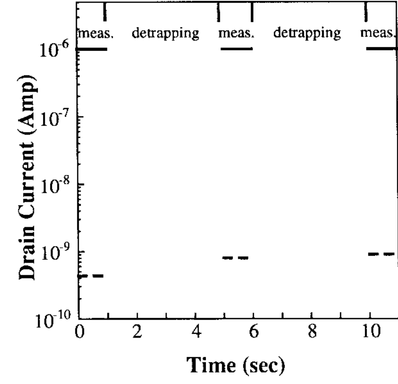

Fig. 3. Pre-stress (solid line) and post-stress (dashed line) subthreshold currents in three measurement/detrapping cycles. The voltages are $V_{\rm gs} = 1.2$ V and $V_{\rm ds} = 0.1$ V in the measurement phase and $V_{\rm gs} = -7$ V and $V_{\rm ds} = 0$ V in the detrapping phase.

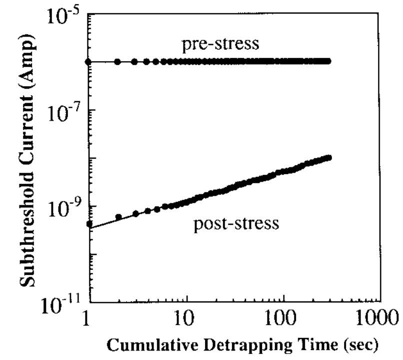

Fig. 4. Pre-stress and post-stress subthreshold currents versus cumulative detrapping time. Full circles represent the measurement data points.

subthreshold current (solid line) does not change with time. After stress, the subthreshold current (dashed line) remains almost constant during a measurement phase and is enhanced significantly after each detrapping phase. The evolution of the subthreshold current with cumulative detrapping time is plotted on a log-log scale in Fig. 4. Because interface traps have time-constants several orders shorter than those of oxide traps, the observed transient on a time scale of tens of seconds is certainly due to oxide trap discharging. The stress induced subthreshold current transient follows approximately a straight line in Fig. 4. This observed characteristic agrees with (12) and confirms that oxide charge detrapping is through a trapezoidal barrier at the present detrapping gate bias. The power factor p in Fig. 4 is about 0.55. By using $n = 1.6$, $m^* = 0.3m_o$ [16], $E_t = 3.1$ eV [17], the extracted oxide charge volumetric density is about $4 \times 10^{18} q/\text{cm}^3$.

B. Field and Temperature Effects

To analyze the field effect on oxide charge detrapping, the gate bias in the detrapping phase is adjusted from −4 V to −7 V in Fig. 5. The measured device was F–N stressed for 2000 s. As the negative gate bias (or oxide field) increases in Fig. 5, the time needed for the current to reach the same level becomes shorter. In other words, the effective detrapping time is a decreasing function of an oxide field. Such field dependence also provides evidence that field enhanced tunneling is

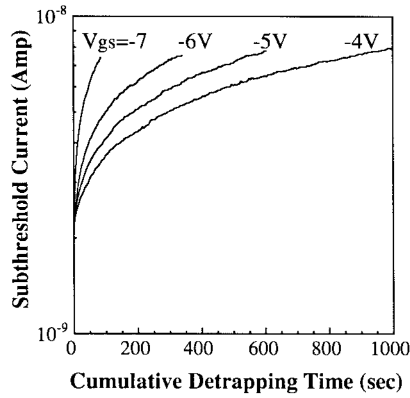

Fig. 5. Oxide charge detrapping induced subthreshold current transients in a F–N stressed device with various detrapping gate biases. The stress time is 2000 s. The measurement biases are $V_{gs} = 1.65$ V and $V_{ds} = 0.1$ V.

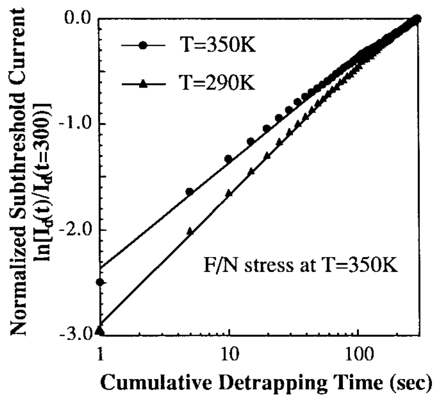

Fig. 6. Subthreshold current transients measured at $T = 290$ K and $T = 350$ K. The device was F–N stressed at $T = 350$ K for 2000 s. The symbols are the measured data points.

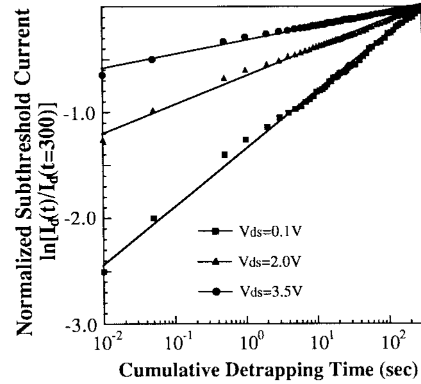

Fig. 7. Subthreshold current transients with $V_{ds} = 0.1$ V, 2.0 V, and 3.5 V in the measurement phase. The device was HE stressed for 10^4 s.

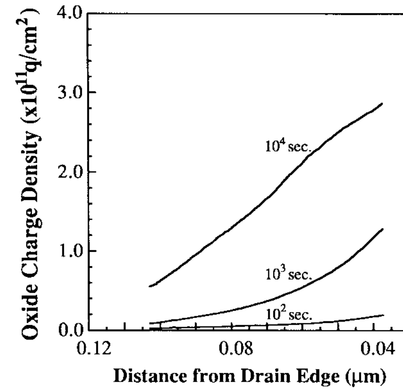

Fig. 8. Lateral profiling of the escaping oxide charge density in the measurement period. q is the elementary charge. The detrapping condition is $V_{gs} = -7$ V for 300 s. The stress times are 10^2 s, 10^3 s, and 10^4 s, respectively.

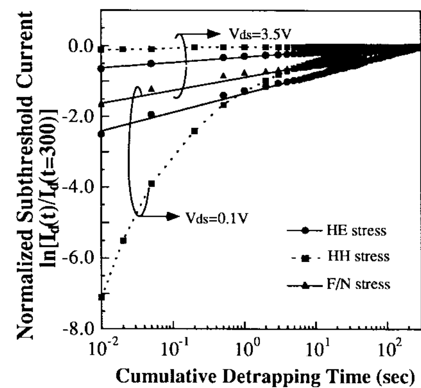

Fig. 9. Comparison of the HE stress, HH stress and F–N stress induced subthreshold current transients at $V_{ds} = 0.1$ V and 3.5 V. The sequence of the transient magnitude is HH > HE > F–N at $V_{ds} = 0.1$ V and F–N > HE > HH at $V_{ds} = 3.5$ V. The stress time is 10^4 s for the HE stress, 300 s for the HH stress and 400 s for the F–N stress.

a major mechanism in oxide charge detrapping. With respect to the temperature effect, the subthreshold current transients at two different temperatures $T = 290$ K and 350 K were measured in Fig. 6. The same detrapping gate bias $V_{gs} = -7$ V was applied. The slope of the measured transients is inversely proportional to temperature, as shown in (12).

C. Lateral Profiling of Oxide Traps

Lateral profiling of the stress generated oxide traps in the channel is achieved by varying the drain bias in the measurement phase. As the drain bias increases, the drain depletion region gradually extends from the drain edge toward the source. Fig. 7 shows the measured transients in a HE stressed n-MOSFET at various drain biases. Due to the nature of localized trap generation by the HE stress, the oxide trap induced transient diminishes as the drain depletion extends over the entire trap region. Fig. 8 shows the lateral distributions of oxide charge at different stress times. In the figure, the escaping oxide charge density in the measurement period is calculated from (7). The relationship between an applied drain bias and the width of the drain depletion region is estimated from an analytical model in [18]. As a first-order approximation, the drain induced barrier lowering (DIBL) effect [19] was neglected in the calculation of the oxide charge density.

The subthreshold transients by the F–N stress, HE stress and HH stress are compared and are shown in Fig. 9. Before the transient measurement, all of the stressed devices were subject to the substrate hot electron injection for oxide trap filling. Therefore, only the acceptor-like oxide traps are measured for

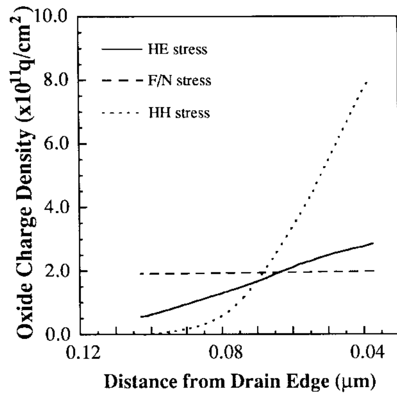

Fig. 10. Lateral profiling of the HE stress, HH stress and F–N stress created electron trap distributions. q is the elementary charge.

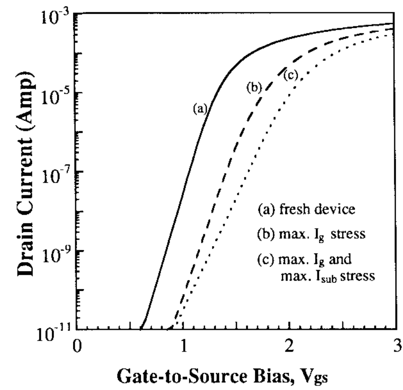

Fig. 11. The $I_{\rm ds}$–$V_{\rm gs}$ subthreshold current characteristics in three test devices. $I_{\rm sub}$ stress: $V_{\rm gs} = 2.5$ V and $V_{\rm ds} = 5$ V for 5000 s. I_g stress: $V_{\rm gs} = 6.5$ V and $V_{\rm ds} = 5$ V for 10^4 s.

the donor-like oxide traps are not charged when filled with electrons. In the figure, the F–N stress transients at $V_{\rm ds} = 0.1$ V and $V_{\rm ds} = 3.5$ V are identical. Among the three stresses the HH stress transient shows a largest magnitude at $V_{\rm ds} = 0.1$ V and a smallest magnitude at $V_{\rm ds} = 3.5$ V. This result implies that the HH stress generated oxide traps have a largest density whereas their spatial distribution in the channel is narrowest as compared to the other two stresses (Fig. 10). There are two reasons for the feature in Fig. 10; First, the lateral field distribution in the channel is more restricted in the HH stress than in the HE stress from a two-dimensional simulation, which consequently gives rise to a narrower oxide trap region in the channel. Second, the hole injection has a higher energy threshold than the electron injection because of a larger Si/SiO_2 interface barrier for holes. In addition, Fig. 9 reveals that the two hot carrier stress induced transients at $V_{\rm ds} = 0.1$ V exhibit a crossover around $t = 1.0$ s. The crossover can be realized due to a smaller effective detrapping time of the HH stress generated oxide traps. Our result is consistent with the findings by Weber *et al.* that the hole stress induced electron traps are located closer to the Si/SiO_2 surface [20] and thus the HH stress induced traps have a shorter detrapping time-constant. Moreover, a strong nonlinearity is observed in the HH stress transient in Fig. 9. This characteristic can be possibly explained by a strongly nonuniform oxide charge distribution in the vertical direction caused by the HH stress [20].

D. Coexistence of Interface Traps and Oxide Traps

The feasibility of using this oxide trap technique in the presence of interface traps is examined. Two hot electron stress methods are utilized, maximum I_g stress and maximum $I_{\rm sub}$ stress. It was reported that the traps created by the maximum I_g stress are mostly oxide traps while interface trap generation is dominant by the maximum $I_{\rm sub}$ stress [21]. Fig. 11 shows the $I_{\rm ds}$–$V_{\rm gs}$ characteristics in three test devices, (a) a fresh device, (b) a maximum I_g stressed device, and (c) a maximum I_g then maximum $I_{\rm sub}$ stressed device. Interface trap generation is evidenced by the degradation of the subthreshold slope after the maximum $I_{\rm sub}$ stress. The corresponding subthreshold transients in the three devices are plotted in Fig. 12. The device (c) shows a less pronounced transient effect than the device (b) due to a degraded subthreshold slope. Although the

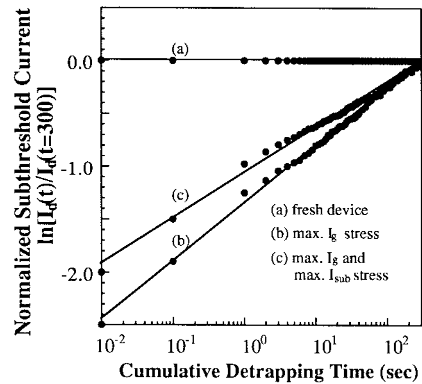

Fig. 12. Oxide charge detrapping induced subthreshold current transients in the three test devices.

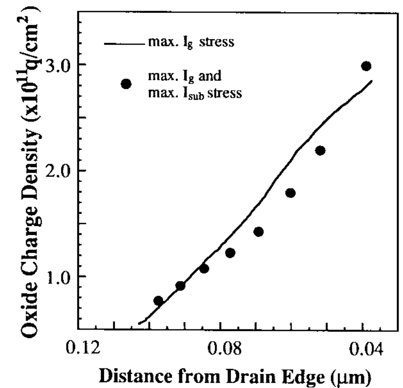

Fig. 13. Measured oxide trap distributions in the max. I_g stressed device and in the max. I_g and then max. $I_{\rm sub}$ stressed device.

transient magnitudes in the devices (b) and (c) are different, the extracted oxide trap densities and distributions in the two devices agree with each other reasonably well in Fig. 13. In other words, the oxide trap characterization result by this technique is not affected by the existence of interface traps.

IV. Conclusion

We have proposed a transient oxide trap characterization technique. This technique is found to be extremely sensitive to oxide charge variation. By taking advantage of the time-

constant separation between interface traps and oxide traps, this transient technique allows the oxide trap characterization separately in the presence of interface traps. The obtained time-dependence of a subthreshold current transient confirms that oxide charge detrapping is through a trapezoidal barrier tunneling. Oxide charge creation under various stress conditions has been studied. As compared to the HE stress and the F–N stress, the HH stress generated oxide charges can be characterized by a shorter effective detrapping time-constant and a more restricted spatial distribution in the channel.

REFERENCES

[1] C. T. Wang, *Hot Carrier Design Considerations for MOS Device and Circuits*, Van Nostrand Reinhold, New York, 1992.

[2] R. Moazzami and C. Hu, "Stress-induced current in thin SiO_2 films," in *IEDM Tech. Dig.*, pp. 139–142, 1992.

[3] S. Haddad, C. Chang, B. Swaminathan, and J. Lien, "Degradation due to hole trapping in flash memory cells," *IEEE Elect. Device Lett.*, vol. 10, pp. 117–119, 1990.

[4] K. Naruke, S. Taguchi, and M. Wada, "Stress induced leakage current limiting to scale down EEPROM tunnel oxide thickness," in *IEDM Tech. Dig.*, 1988, pp. 424–427.

[5] S. Yamada, Y. Hiura, T. Yamane, K. Amemiya, Y. Ohshima, and K. Yoshikawa, "Degradation mechanism of flash EEPROM programming after program/erase cycles," in *IEDM Tech. Dig.*, 1993, pp. 23–26.

[6] J.-C. Marchetaux, M. Bourcerie, A. Boudou, and D. Vuillaume, "Application of the floating gate technique to the study of the n-MOSFET gate current evolution due to hot carrier aging," *IEEE Elect. Device Lett.*, vol. 11, pp. 406–408, 1990.

[7] M. Kato, N. Miyamoto, H. Kume, A. Satoh, T. Adachi, M. Ushiyama, and K. Kimura, "Read-disturb degradation mechanisms due to electron detrapping in the tunnel oxide for low-voltage flash memorues," in *IEDM Tech. Dig.*, 1994, pp. 45–48.

[8] M. Bourcerie, B. S. Doyle, J. C. Soret, and A. Boudou, "Relaxable damage in hot-carrier stressing of n-MOSFET transistor-oxide traps in the near interface region of the gate oxide," *IEEE Trans. Electron Devices*, vol. 37, pp. 708–717, 1990.

[9] T. Wang, T. E. Chang, L. P. Chiang, and C. Huang, "A new technique to extract oxide trap time-constants in MOSFET's," *IEEE Elect. Device Lett.*, vol. 17, pp. 398–400, 1996.

[10] T. Wang, T. E. Chang, L. P. Chiang, C. H. Wang, N. K. Zous, and C. Huang, "Investigation of oxide charge trapping and detrapping in a MOSFET by using a GIDL current technique," *IEEE Trans. Electron Devices*, vol. 45, pp. 1511–1517, July 1998.

[11] W. Chen and T. P. Ma, "A new technique for measuring lateral distribution of oxide charge and interface trap near MOSFET junctions," *IEEE Elect. Device Lett.*, vol. 12, pp. 393–395, 1991.

[12] W. Chen, A. Balasinski, and T. P. Ma, "Lateral profiling of oxide charge and interface traps near MOSFET junctions," *IEEE Trans. Electron Devices*, vol. 40, pp. 187–196, 1993.

[13] S. M. Sze, *High-Speed Semiconductor Devices*. New York: Wiley, 1990, ch. 3.

[14] B. El-Kareh and R. J. Bombard, *Introduction to VLSI Silicon Devices*. Boston, MA: Kluwer, 1986, p. 461.

[15] I. Lundsorm and C. Svensson, "Tunneling to traps in insulator," *J. Appl. Phys.*, vol. 43, pp. 5045–5047, 1972.

[16] B. Brar, G. D. Wilk, and A. C. Seabaugh, "Direct extraction of the electron tunneling effective mass in ultra-thin SiO_2," *Appl. Phys. Lett.*, vol. 69, pp. 2728–2730, 1996.

[17] T. L. Tewksbury, III and H. S. Lee, "Characterization, modeling and minimization of transient threshold shifts in MOSFET's," *IEEE J. Solid-State Circuits*, vol. 29, pp. 239–252, 1994.

[18] S. K. Lai, "Two-carrier nature of interface trap generation in hole trapping and radiation damage," *Appl. Phys. Lett.*, vol. 39, pp. 58–60, 1981.

[19] R. Troutman, "VLSI limitations from drain-induced barrier lowering," *IEEE Trans. Electron Devices*, vol. 26, pp. 461–469, 1979.

[20] W. Weber, M. Brox, R. Thewes, and N. S. Saks, "Hot-hole-induced negative oxide charge in n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 42, pp. 1473–1480, 1995.

[21] B. Doyle, M. Bourcerie, J.-C. Marchetaux, and A. Boudou, "Interface trap creation and charge trapping in the medium-to-high gate voltage range ($V_d/2 \leq V_g \leq V_d$) during hot-carrier stressing of n-MOS transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 744–754, 1990.

Tahui Wang (M'86–SM'94) was born in Taoyuan, Taiwan, R.O.C., on May 3, 1958. He received the B.S. degree from National Taiwan University, Taipei, in 1980, and the Ph.D. degree in electrical engineering from the University of Illinois, Urbana-Champaign, in 1985.

From 1985 to 1987, he was with Hewlett-Packard Laboratories, Palo Alto, CA, where he was engaged in the development of GaAs HEMT devices and circuits. Since 1987, he has been with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, where he is currently a Professor. His research interests include hot carrier phenomena characterization and reliability physics in VLSI devices.

Dr. Wang was granted the Best Teacher Award by the Ministry of Education, R.O.C., in 1991. He served as technical committee member of the International Reliability Physics Symposium.

Lu-Ping Chiang received the B.S. degree from Tatung Institute of Technology, Taipei, Taiwan, R.O.C, in 1994, and the M.S. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1996, where he is currently pursuing the Ph.D. degree. His thesis research includes characterization and modeling of flash EEPROM reliability.

Nian-Kai Zous received the B.S. degree in electronics engineering in 1996 from National Chaio-Tung University, Hsinchu, Taiwain, R.O.C., where he is currently pursuing the Ph.D. degree. His research interest includes thin oxide reliability and hot carrier effects in deep submicron MOSFET's.

Tse-En Chang was born in Yun-Lin, Taiwan, R.O.C., on October 17, 1969. He received the B.S. and the Ph.D. degrees in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1992 and 1997, respectively. His research interest is in the modeling and physics of MOSFET reliability.

Currently, he is in military service as a Lieutenant.

Chimoon Huang received the B.S. degree from National Ocean University, Keelung, Taiwan, R.O.C., in 1986, and the Ph.D. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1994.

Currently, he is a Project Manager at the Technology Development Department, Macronix International Co., Hsinchu, and is engaged in the development of high-density flash EEPROM and embedded flash EEPROM. He is also with the Department of Electrical Engineering, National Lien-Ho College of Technology and Commerce as an Adjunct Associate Professor. His research interests include the hot carrier effects in Si MOSFET's, thin dielectric, and the technology development of nonvolatile memory devices.