High-Performance CMOS Buffered Gate Modulation Input (BGMI) Readout Circuits for IR FPA

Chih-Cheng Hsieh, Chung-Yu Wu, *Fellow, IEEE,* Tai-Ping Sun, Far-Wen Jih, and Ya-Tung Cherng, *Member, IEEE*

***Abstract*— A new CMOS current readout structure for the infrared (IR) focal-plane-array (FPA), called the buffered gate modulation input (BGMI) circuit, is proposed in this paper. Using the technique of unbalanced current mirror, the new BGMI circuit can achieve high charge sensitivity with adaptive current gain control and good immunity from threshold-voltage variations. Moreover, the readout dynamic range can be significantly increased by using the threshold-voltage-independent current-mode background suppression technique. To further improve the readout performance, switch current integration techniques, shared-buffer biasing technique, and dynamic charging output stage with the correlated double sampling circuit are also incorporated into the BGMI circuit. An experimental 128 × 128 BGMI readout chip has been designed and fabricated in 0.8 μm double-poly-double-metal (DPDM) n-well CMOS technology. The measurement results of the fabricated readout chip under 77K and 5 V supply voltage have successfully verified both readout function and performance improvement. The fabricated chip has the maximum charge capacity of 9.5 × 10^7 electrons, the transimpedance of 2.5 × 10^9 Ω at 10 nA background current, and the active power dissipation of 40 mW. The uniformity of background suppression currents can be as high as 99%. Thus, high injection efficiency, high charge sensitivity, large dynamic range, large storage capacity, and low noise can be achieved in the BGMI circuit with the pixel size of 50 × 50 μm^2. These advantageous characteristics make the BGMI circuit suitable for various IR FPA readout applications with a wide range of background currents.**

***Index Terms*—Detector, fixed pattern noise, infrared imaging, IR focal-plane-array, readout circuits.**

I. Introduction

In the infrared (IR) imaging systems with the focal-plane-array (FPA), there are various design requirements and constraints on readout interface circuits, such as high charge storage capacity, low noise, large dynamic range, low power dissipation, good detector bias control, small array size, and small pixel pitch. As the cell number in the FPA becomes larger, the pixel size and pitch should be scaled down to accommodate more detector cells within a reasonably small array size. However, the small pixel size limits the complexity of the input stage in the readout circuit and the capacitance value of the integration capacitor, which may degrade the readout performance. Thus, many efforts have been devoted to the development of new techniques and circuits to improve readout performance under various design constraints [1]–[6]. Among them, both background suppression [1]–[3] and adaptive gain control techniques [4], [5] can significantly improve the effective charge storage capacity, dynamic range, and noise performance.

Generally, the background suppression technique can be realized by using two types of circuits, namely charge-domain background suppression circuit [2] and current-memory based background suppression circuit [3]. The charge-domain circuit integrates both desired signal and background current prior to the background suppression. Thus, it cannot alleviate the problem of storage capacity limit. On the other hand, the current-memory suppression circuit needs complex in-pixel feedthrough reduction circuit and calibration cycle. Thus, it is not suitable for large format FPA applications.

It is well known that the gate modulation input (GMI) circuit [2], [4], [5] can yield very low input-referred noise and high charge detection sensitivity due to the adaptive high current-mode gain which is approximately inversely proportional to the square root of the detector output current. But the GMI circuit is susceptible to both voltage bias noise and fixed pattern noise (FPN) due to threshold-voltage variations. This degrades the readout performance of the GMI circuit.

In this paper, a new current readout structure for the IR FPA, called the buffered gate modulation input (BGMI) circuit, is proposed to solve the above mentioned problems and improve the readout performance. Based on the switch current integration (SCI) [6], [7] readout structure, the BGMI circuit integrates the shared-buffer detector biasing technique [8] with a GMI-like current-gain configuration to form the unit-cell input stage. The current gain is realized by a new unbalanced current mirror configuration. The resultant current gain is immune from process-dependent threshold-voltage variations and inversely proportional to the square root of the detector output current. Thus, adaptive gain control and gain uniformity can be achieved. A current-mode background suppression circuit is also implemented in the off-FPA shared integration capacitor unit to suppress the background current before integration. Moreover, the dynamic charging output stage with the correlated double sampling (CDS) circuit is included to decrease the power dissipation of the output stage and reduce noise. It has been shown from both simulation and experimental results that the proposed BGMI readout circuit can achieve high readout performance in a small pixel size through the use of BGMI technique with adaptive current gain,

Manuscript received May 30, 1997; revised February 28, 1998. This work was supported by the Chung Shang Institute of Science and Technology, Taiwan, R.O.C., under Contract CS86-0210-D009-002.

C.-C. Hsieh and C.-Y. Wu are with the Integrated Circuits & Systems Laboratory, Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Taiwan 300, Republic of China.

T.-P. Sun, F.-W. Jih, and Y.-T. Cherng are with the Chung Shang Institute of Science and Technology, Lung-Tan, Taiwan, Republic of China.

Publisher Item Identifier S 0018-9200(98)05536-X.

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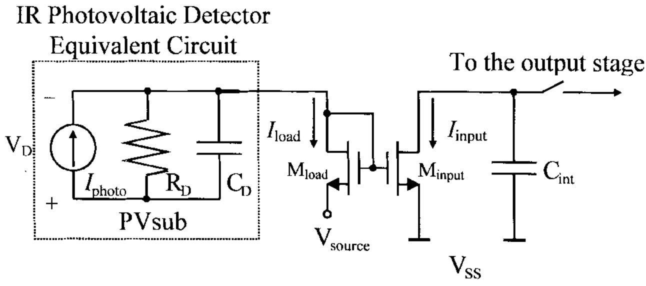

Fig. 1. The gate modulation input (GMI) circuit.

the off-FPA current-mode background suppression, and the previously proposed switch current integration (SCI) structure.

The circuit structure, readout strategy, and circuit performance of the proposed new BGMI readout structure are described in Section II. In Section III, both simulation results and experimental results of the fabricated BGMI readout chip are presented. Finally, a conclusion is given.

II. Circuit Design

The proposed BGMI readout chip consists of the BGMI circuits in the cell array, the shared integration cells with the current-mode background suppression circuits, one two-to-one switch, and one common dynamic charging output stage with the correlated-double sampling (CDS) circuit. In the following subsections, the GMI stage is reviewed first. Then the circuit design and operation of BGMI circuit, current-mode background suppression circuit, and dynamic charging output stage with the CDS circuit will be described. Finally, the BGMI chip operation will be presented.

A. Review on the Gate Modulation Input (GMI) Stage

In the GMI circuit as shown in Fig. 1, a source-degenerated current mirror configuration $M_{\rm load}$ and $M_{\rm input}$ with the source bias $V_{\rm source}$ is used to provide a tunable current gain for IR photovoltaic (PV) detectors. The effective injection efficiency (or current gain) $A_{I.{\rm GMI}}$ which is the current ratio between $\Delta I_{\rm input}$ and $\Delta I_{\rm photo}$ [4], the injection efficiency $\eta_{inj.{\rm DI}}$, and the detector bias V_D of the GMI circuit can be expressed as

$$A_{I.{\rm GMI}} = \frac{\Delta I_{\rm input}}{\Delta I_{\rm photo}} = \frac{g_{m.{\rm input}}}{g_{m.{\rm load}}}\eta_{inj.{\rm DI}} \tag{1}$$

$$\eta_{inj.{\rm DI}} = \frac{g_{m.{\rm load}}R_D}{1+g_{m.{\rm load}}R_D} \tag{2}$$

$$V_D = {\rm PV}_{\rm sub} - V_{{\rm GS}.M{\rm load}} - V_{\rm source} \tag{3}$$

where $g_{m.{\rm input}}$ ($g_{m.{\rm load}}$) is the transconductance of the input (load) MOSFET $M_{\rm input}$ ($M_{\rm load}$) under the input background current, R_D is the detector shunt resistance [9], ${\rm PV}_{\rm sub}$ is the detector N-node bias for N-on-P type PV detectors, $V_{\rm GS.Mload}$ is the gate-to-source voltage of $M_{\rm load}$ under the input background current, and $V_{\rm source}$ is the external adjustable source node voltage.

For the understanding of physical behavior and design guidelines of the GMI circuit, a simplified I–V model of long-channel MOS devices in the saturation region is used to further characterize the GMI parameters in (1)–(3) analytically in terms of MOS device parameters. The same derivation method can be applied if more accurate MOS device I–V model is used. Using the simplified long-channel MOS I–V model, the detector output current $I_{\rm load}$ and $V_{\rm GS.Mload}$ can be expressed as [10]

$$I_{\rm load} = K_{\rm load}(V_{\rm GS.Mload} - V_T)^2 \tag{4}$$

$$V_{\rm GS.Mload} = \sqrt{\frac{I_{\rm load}}{K_{\rm load}}} + V_T \tag{5}$$

where $K_{\rm load}$ is the transconductance parameter of $M_{\rm load}$, and V_T is the threshold voltage of $M_{\rm load}$. In the p-well CMOS process, the substrate of $M_{\rm load}$ can be connected to its source. Thus, $M_{\rm load}$ has no body effect. In the n-well CMOS process, $M_{\rm load}$ has the body effect which increases V_T. From (3) and (5), the detector bias V_D can be expressed as

$$V_D = {\rm PV}_{\rm sub} - \sqrt{\frac{I_{\rm load}}{K_{\rm load}}} + V_T - V_{\rm source}. \tag{6}$$

It can be seen from (6) that the detector bias V_D is sensitive to the threshold voltage and $V_{\rm source}$ variations as well as the possible noise source from $V_{\rm source}$. Since the detector shunt resistance R_D is sensitive to the detector bias V_D, the injection efficiency in (2) is also sensitive to threshold voltage variations and variations and noise of $V_{\rm source}$. To obtain a stable and high injection efficiency, a larger R_D and a strict control on threshold voltage uniformity as well as noise and stability of $V_{\rm source}$ are required.

Using (4) and (5), and the relation $V_{\rm G.Minput} = V_{\rm GS.Mload} + V_{\rm source}$, the output mirrored current $I_{\rm input}$ can be represented as

$$\sqrt{I_{\rm input}} = \sqrt{K_{\rm input}}\left(\sqrt{\frac{I_{\rm load}}{K_{\rm load}}} + V_{\rm source} + \Delta V_{Tm}\right) \tag{7}$$

where ΔV_{Tm} is the threshold-voltage mismatch between $M_{\rm input}$ and $M_{\rm load}$. Using (2), (7), and the relation $g_m = 2\sqrt{KI}$, the current gain $A_{I,{\rm GMI}}$ in (1) can be rewritten as

$$A_{I.{\rm GMI}} = \frac{\sqrt{K_{\rm input}K_{\rm load}}\left[\sqrt{\frac{I_{\rm load}}{K_{\rm load}}} + V_{\rm source} + \Delta V_{Tm}\right]R_D}{1+\sqrt{K_{\rm load}}\sqrt{I_{\rm load}}R_D}. \tag{8}$$

As may be seen from (8), the value of the current gain $A_{I.{\rm GMI}}$ is roughly inversely proportional to the square root of the detector output current $I_{\rm load}$ in certain range of $I_{\rm load}$ where $\sqrt{K_{\rm load}}\sqrt{I_{\rm load}}R_D \gg 1$ and $\sqrt{I_{\rm load}/K_{\rm load}} \ll V_{\rm source}$. This means that an adaptively controlled current gain exists in some range of $I_{\rm load}$. Moreover, the current gain also depends on $V_{\rm source}$. Thus, the current gain can be adjusted by $V_{\rm source}$. In the range of $I_{\rm load}$ where $\sqrt{K_{\rm load}}\sqrt{I_{\rm load}}R_D \gg 1$, R_D in (8) can be cancelled. In this range, if $V_{\rm source}$ is much larger than ΔV_{Tm} under good local matching between $M_{\rm input}$ and $M_{\rm load}$, the current-gain variations among cells can be reduced. Thus, strict global matching of the current mirror is not required in this range of $I_{\rm load}$. However, this range of $I_{\rm load}$ is not large enough as will be shown later. Moreover, when realizing the GMI circuit in the n-well CMOS process, $M_{\rm load}$ has the body

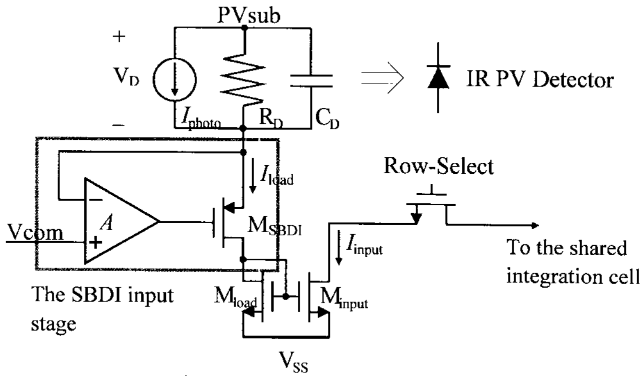

Fig. 2. The buffered gate modulation input (BGMI) circuit with the SBDI input stage and the current gain configuration in the GMI circuit.

effect which makes ΔV_{Tm} much larger and the device local match much more difficult.

It can be seen from (8) and (1) that the GMI circuit, like the DI readout, needs a large detector shunt resistance R_D to achieve a high injection efficiency and thus a high current gain. As seen from (6), R_D is sensitive to $V_{\rm source}$ and threshold voltage variations of $M_{\rm input}$ due to V_D. Thus, the current gain is also sensitive to V_T of $M_{\rm input}$ in the case that R_D cannot be cancelled in (8). Due to this sensitivity, the threshold-voltage variation of $M_{\rm input}$ causes the current gain to vary from one cell to another. This makes the GMI circuit susceptible to the fixed-pattern noise. Moreover, the GMI circuit is susceptible to the noise from $V_{\rm source}$. To obtain a large total dynamic range in the GMI circuit, the current gain should be kept high and uniform. This requires strict requirements on MOSFET threshold-voltage uniformity and extremely low-noise $V_{\rm source}$, which are difficult to control. Since $V_{\rm source}$ is in the range of several hundred millivolts with respect to $V_{\rm SS}$, and the adjustment range is in the order of several tens of millivolts, both stability and adjustment are very critical.

B. Buffered Gate Modulation Input (BGMI) Stage

In the proposed buffered gate modulation input (BGMI) circuit, the input stage of the share-buffered direct-injection (SBDI) [8] circuit is connected to a GMI-like current-gain configuration as shown in Fig. 2. Through the SBDI input stage and the current mirror, the output current $I_{\rm input}$ of the current mirror is sent to the shared integration cell through the row select switch. The effective current gain $A_{I.\rm BGMI}$ of the BGMI circuit, the injection efficiency $\eta_{inj.\rm SBDI}$, and V_D of the BGMI circuit are

$$A_{I.\rm BGMI} = \frac{\Delta I_{\rm input}}{\Delta I_{\rm photo}} = \frac{g_{m.\rm input}}{g_{m.\rm load}} \eta_{inj.\rm SBDI} \quad (9)$$

$$\eta_{inj.\rm SBDI} = \frac{(1+A) g_{m.\rm SBDI} R_D}{1 + (1+A) g_{m.\rm SBDI} R_D} \quad (10)$$

$$V_D = {\rm PV_{sub}} - V_{\rm com} \quad (11)$$

where A is the gain of the amplifier A, $V_{\rm com}$ is the common input bias, and $g_{m.\rm SBDI}$ is the tranconductance of the device $M_{\rm SBDI}$ which is designed to have no body effect in the n-well CMOS process. As may be seen from (10), high injection efficiency can be achieved with a smaller R_D as compared to that in the GMI circuit. Furthermore, the detector bias V_D in (11) is independent of the MOS threshold voltage and any source bias voltage. Thus, unlike the GMI circuit, the threshold nonuniformity and the source bias variation have no effect on the detector bias and R_D. The stable detector bias and R_D lead to a stable injection efficiency.

As seen from (9), the current gain is proportional to the transconductance ratio between $M_{\rm input}$ and $M_{\rm load}$. To increase the current gain, $g_{m.\rm input}$ should be larger than $g_{m.\rm load}$. To achieve this without any external bias voltage, shorter channel length is used in $M_{\rm input}$, whereas narrower channel width is used in $M_{\rm load}$. Due to both short-channel and narrow-channel effects [11] and [12], the threshold voltage of $M_{\rm load}$ is inherently greater than that of $M_{\rm input}$. For example, if the channel widths/lengths of $M_{\rm input}$ and $M_{\rm load}$ are 16 μm/8 μm and 3 μm/16 μm, respectively, the inherent threshold difference ΔV_{Ti} is about 30 mV under 77K operational environment. With ΔV_{Ti}, $I_{\rm input}$ can be expressed similarly to (7) as

$$\sqrt{I_{\rm input}} = \sqrt{K_{\rm input}} \left(\sqrt{\frac{I_{\rm load}}{K_{\rm load}}} + \Delta V_{Ti} + \Delta V_{Tm} \right). \quad (12)$$

If good local match between $M_{\rm load}$ and $M_{\rm input}$ is achieved, ΔV_{Tm} is smaller than ΔV_{Ti}. Since ΔV_{Ti} can be controlled by choosing the suitable difference of device geometries between $M_{\rm load}$ and $M_{\rm input}$, it is very stable under different operating voltages or currents. Moreover, since the geometry deviations are small and the mating of device parameters is good between $M_{\rm load}$ and $M_{\rm input}$ in the advanced CMOS process, the uniformity of ΔV_{Ti} among cells is good. Thus, the current gain in the BGMI circuit can be stable without the difficulties in adjusting and stabilizing the external bias voltage and keeping it in low noise.

The transconductance parameter $K_{\rm SBDI}$ of $M_{\rm SBDI}$ is designed to be the same as $K_{\rm load}$. Using (9) and (12), and the relation $g_{m.\rm SBDI} = 2\sqrt{K_{\rm SBDI} I_{\rm load}} = 2\sqrt{K_{\rm load} I_{\rm load}} = g_{m.\rm load}$, $A_{I,\rm GMI}$ in (9) can be rewritten as

$$A_{I,\rm BGMI} = \frac{\sqrt{K_{\rm input} K_{\rm load}} \left[\sqrt{\frac{I_{\rm load}}{K_{\rm load}}} + \Delta V_{Ti} + \Delta V_{Tm} \right] R_D}{\frac{1}{1+A} + \sqrt{K_{\rm load}} \sqrt{I_{\rm load}} R_D}. \quad (13)$$

Since ΔV_{Tm} is small and R_D is independent of threshold voltage and bias voltage variations, the current gain of the BGMI circuit is immune to global threshold voltage variations and external bias voltage variations.

As may be seen from (13), for sufficiently large value of A, $A_{I.\rm BGMI}$ is inversely proportional to $I_{\rm load}$ in the range of $I_{\rm load}$ where $\sqrt{K_{\rm load}} \sqrt{I_{\rm load}} R_D \gg 1/(1+A)$ and $\sqrt{I_{\rm load}/K_{\rm load}} \ll \Delta V_{Ti}$. Since these conditions can be more easily satisfied, the range of $I_{\rm load}$ in the BGMI circuit is larger than that in the GMI circuit. The high, stable, and adaptive front-stage current

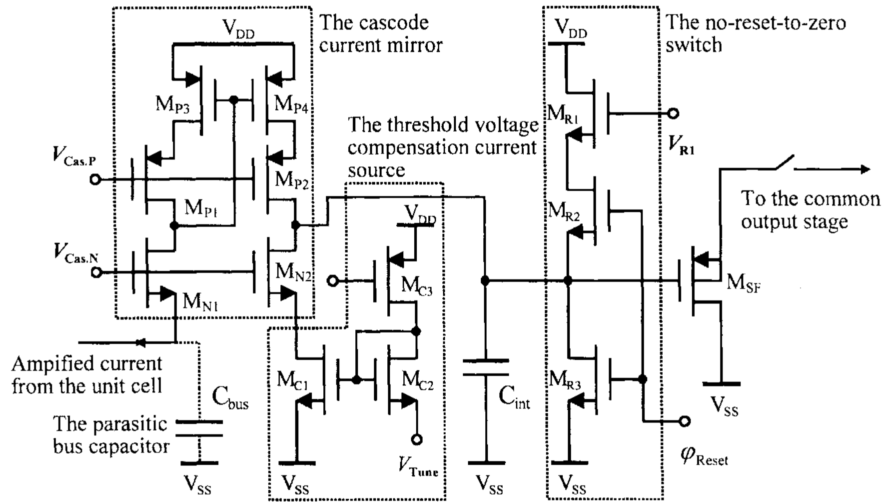

Fig. 3. The shared integration cell with current-mode background suppression.

gain in the BGMI circuit makes the noise contribution of the stages after the current mirror extremely low. It results in a low input referred noise.

In the above analysis of the current gains in both GMI and BGMI circuits, the channel length modulation effect is not considered. This effect degrades the gains and makes them source-drain voltage dependent. But the BGMI circuit has less degradation than the GMI circuit. In the design of both GMI and BGMI circuits, it is suggested that long channel length is used to avoid this effect.

C. The Current-Mode Background Suppression Circuit

In the GMI circuit, the amplified signal current and background current are integrated directly and thus a large amount of charges must be accommodated within an unit cell, implying the requirement of a large integration capacitor. This is a problem in a large IR FPA system. A current-mode background suppression circuit with the SCI structure is proposed to solve this problem. This results in higher dynamic range and better readout performance.

The off-FPA shared integration cell with the proposed current-mode background suppression circuit is shown in Fig. 3. The switched current from the unit cell is mirrored through a cascode current mirror [13] with the current ratio of 1. The use of cascode current mirror can reduce the effect of input voltage difference across the nonuniform parasitic bus capacitance $C_{\rm bus}$ and increase the current-mirror accuracy during integration. The drain voltage of $M_{\rm P3}$ ($M_{\rm P4}$) is controlled by both cascode device $M_{\rm P1}$ ($M_{\rm P2}$) and voltage $V_{\rm Cas.P}$ to keep the current mirror in the saturation region during integration. For the same reason, the cascode device $M_{\rm N1}$ ($M_{\rm N2}$) and the voltage $V_{\rm Cas.N}$ are used to control the drain voltage of $M_{\rm C1}$. After the cascode current mirror, the amplified current from the cell is subtracted by a dc tunable background current before integrated on the capacitor C_{int}. Thus, the current-mode background suppression is achieved. To generate the dc current, the threshold-voltage compensated current source [14] composed of $M_{\rm C1}$, $M_{\rm C2}$, $M_{\rm C3}$ is used. The drain current $I_{\rm MC1}$ flowing in device $M_{\rm C1}$ can be expressed as

$$I_{MC1} = K_{MC1}\left(V_{\rm tune} + V{\rm th}_{MC2} - V{\rm th}_{MC1} - \sqrt{\frac{I_{MC2}}{K_{MC2}}}\right)^2 \quad (14)$$

where K_{MC1} (K_{MC2}) is the transconductance parameter of the MOS device $M_{\rm C1}$ ($M_{\rm C2}$), $V{\rm th}_{MC1}$ ($V{\rm th}_{MC2}$) is the threshold voltage of $M_{\rm C1}$ ($M_{\rm C2}$), I_{MC2} is the biasing current controlled by the device $M_{\rm C3}$, and $V_{\rm tune}$ is a tunable dc bias. As seen from (14), this current source can generate a dc current nearly independent of MOS threshold voltages if small biasing current I_{MC2} and large transconductance parameter K_{MC2} are used. Thus, the pedestal removal of IR FPA readout with good immunity from threshold-voltage nonuniformity can be achieved. Thus, the spatial noise due to nonuniform background suppression can be reduced. The suppression current is adjustable through the voltage $V_{\rm tune}$.

A no-reset-to-zero circuit realized by $M_{\rm R1}$, $M_{\rm R2}$, and $M_{\rm R3}$ is used to keep $M_{\rm C1}$ in the saturation region. In the reset phase with $\phi_{\rm Reset}$, the integration node is reset to $V_{\rm Rst}$ instead of zero to maintain the saturation drain voltage $V_{\rm dsat}$ of $M_{\rm C1}$. The reset level $V_{\rm Rst}$ is equal to the drain-source voltage drop on $M_{\rm R3}$, which is dependent upon V_{DD}, $V_{\rm R1}$ and the dimensions of $M_{\rm R1}$, $M_{\rm R2}$, and $M_{\rm R3}$. For $V_{DD} = 5$ V and $V_{\rm R1} = 3$ V, $V_{\rm Rst} = 0.5$ V. If the integration node is reset to zero, $M_{\rm C1}$ is forced to the linear region with reduced current. Thus, it takes some recovery time when the next row is switched in. This leads to the signal integration error.

Although this current-mode background suppression circuit consumes additional power due to the small dc bias current through $M_{\rm C2}$, it is still acceptable in the case of the SCI readout structure where only one background suppression current source per row is needed. For example, in a 128×128 array readout system, only 128 suppression current sources are needed and they consume less than 4 mW additional power at 50 nA background flux.

In the shared integration cell, the off-FPA shared integration capacitor has no pixel-size limitation. Thus, it can be large to

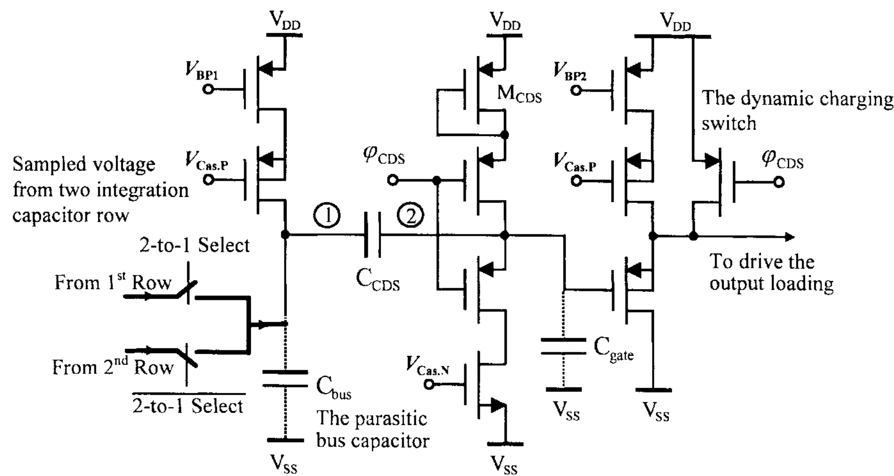

Fig. 4. The common output stage with CDS and dynamic charging circuits.

increase the storage capacity. The integrated signal voltage is sampled serially to the common output stage through the P-type source follower $M_{\rm SF}$ as a buffer.

D. The Dynamic Charging Output Stage with CDS

As shown in Fig. 4, the output stage is composed of correlated-double sampling (CDS) stage and PMOS source follower with the dynamic charging device. All PMOS source followers use the cascode current sources as loads to improve the readout performance. The voltage signal from the shared integration cell is correlated-double-sampled to reduce the $1/f$ noise of source follower and bus line. In the first sample phase with $\phi_{\rm CDS}$ low, the voltage at the node 1 is $V_{\rm sig} + V_{T.M_{\rm SF}} + V_{\rm Rst}$, and the node 2 is reset to a dc level about $V_{DD} - V_{T.M_{\rm CDS}}$ instead of V_{DD}, where $V_{\rm sig}$ is the integrated signal voltage, $V_{\rm Rst}$ is the reset level controlled by $V_{\rm R1}$, and $V_{T.M_{\rm SF}}$ ($V_{T.M_{\rm CDS}}$) is the threshold voltage of PMOS device $M_{\rm SF}$ ($M_{\rm CDS}$). The reset level at the node 2 is designed to have a dc level offset from V_{DD} for the following PMOS source follower with the dynamic charging structure. This can increase the maximum output swing of the source follower. In the second sample phase with $\phi_{\rm CDS}$, the integration capacitor is reset to $V_{\rm Rst}$ and the voltage at the node 1 becomes $V_{\rm Rst} + V_{T.M_{\rm SF}}$. Because the voltage on the capacitor $C_{\rm CDS}$ remains the same, the voltage at the node 2 becomes $V_{DD} - V_{T.M_{\rm CDS}} - V_{\rm sig}$. This realizes the CDS function.

Since the noise of PMOS devices is less than that of NMOS devices, the noise performance can be improved by using the two cascaded PMOS source-followers called the P-P type cascaded SF as shown in Fig. 4 instead of the PMOS source follower cascaded by the NMOS source follower called the P-N type cascaded SF. Moreover, the body effect of NMOS source followers fabricated in the n-well process degrades the maximum output excursion in the P-N type cascaded SF.

In the output stage, the dynamic charging switch is turned on in the reset-to-high phase with $\phi_{\rm CDS}$ low and the output node is precharged to V_{DD}. When $\phi_{\rm CDS}$ is high, the switch is off and the integrated signal is sent to the output through the PMOS source follower. This can overcome the speed bottleneck of the output stage while maintaining low power dissipation of the output stage. The control clock can be shared with the CDS reset clock $\phi_{\rm CDS}$.

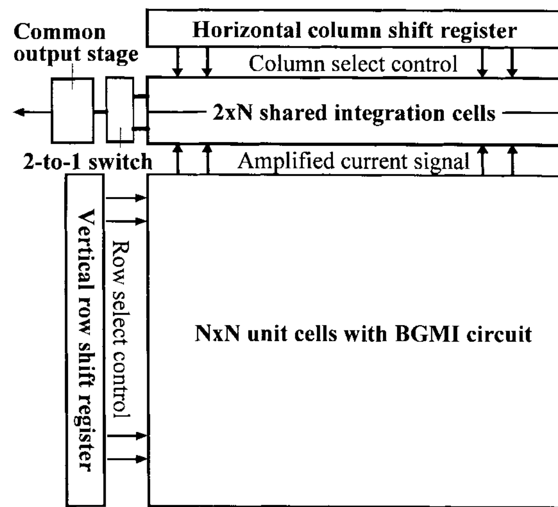

Fig. 5. The block diagram of the buffered gate modulation input (BGMI) readout chip.

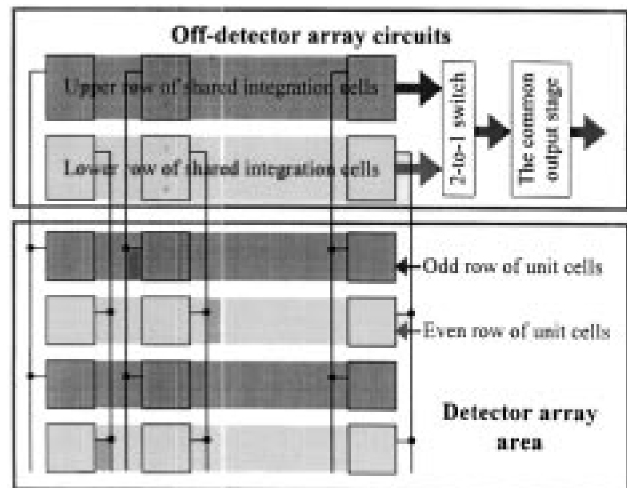

Fig. 6. The connection of odd-even blocks and data selection of the output stage.

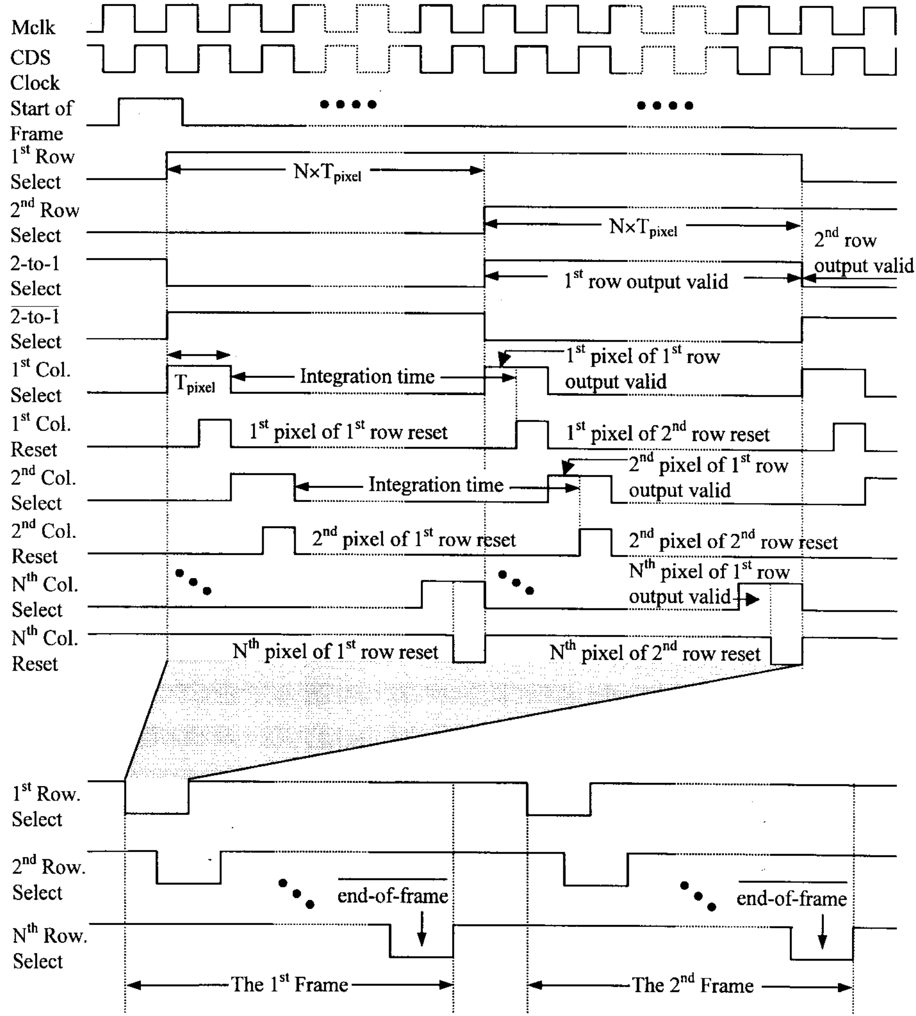

Fig. 7. The clock timing waveforms of master clock ($Mclk$), CDS Clock ($\phi_{\rm CDS}$), output selection clock (2-to-1 Select), row select (R-Sel), column select (C-Sel), column reset ($\phi_{\rm CDS}$), and signal end-of-frame.

The transimpedance of the IR readout circuit is

$$Z_{\rm Total} = \left(\frac{A_1 T_{int}}{C_{int}}\right) A_V \tag{15}$$

where T_{int} is the integration time, and A_V is the total voltage gain through the readout circuit due to source-follower gains and charge sharing between CDS capacitor $C_{\rm CDS}$ and gate capacitance $C_{\rm gate}$. Thus, A_V is less than 1. But the current gain A_I in the BGMI circuit may be orders of magnitude higher as compared to the DI, BDI, or CTIA [5] readout. This leads to the same high transimpedance.

E. The BGMI Chip Operation

Fig. 5 shows the block diagram of the proposed BGMI readout chip which is composed of $N \times N$ cell array with BGMI circuits, $2 \times N$ shared integration cells with the current-mode background suppression circuit, one two-to-one switch, and one common output stage. There are two rows of $1 \times N$ share integration cells in this chip. All the odd (even) rows of $N \times N$ unit cells are connected through the switch to the upper (lower) row of shared integration cells as shown in Fig. 6. This design of two-row integration-cells is used to achieve the no-dead-time data readout operation. The circuit operation is explained as follows.

The clock timing waveforms of master clock $Mclk$, CDS clock $\phi_{\rm CDS}$, column start signal, row select R-Sel, column select C-Sel, 2-to-1 selection clock, and column reset clock $\phi_{\rm Reset}$ are shown in Fig. 7 where all the clock signal have high level of 5 V and low level of 0 V. The readout operation of the BGMI chip is described below. When R-Sel of the first row is high and C-Sel of the first column is high, the unit-cell input stage of the first row is switched to the upper row of shared integration cells and the first pixel in the first row of unit cells is selected and reset to perform the readout current integration with the integration time indicated in Fig. 7. After the row-processing time $N \times T_{\rm pixel}$, where N is the column number and $T_{\rm pixel}$ is the pixel processing time, R-Sel of the second row is high and the unit cells of the second row are switched to the lower row of integration cells, whereas the first pixel in the second row of unit cells is selected and reset for integration. At the same time, the *2-to-1 select* clock is high and the first pixel in the upper row of integration cells is sampled to the output stage. Then the second pixel of the upper row is read out in series. The integration time T_{int} is controlled by the

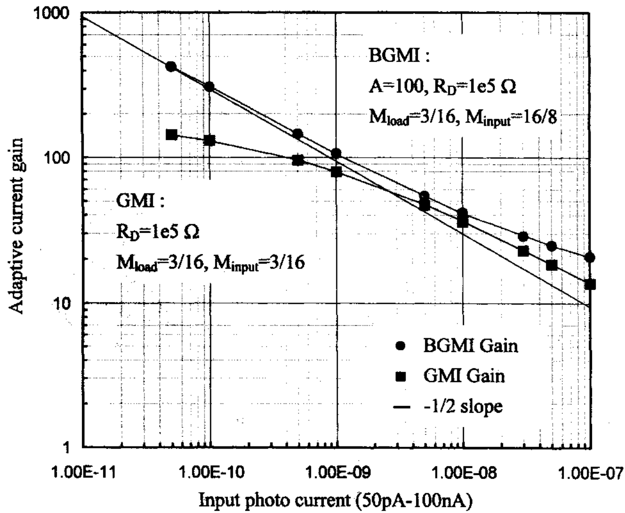

Fig. 8. The adaptive gain control property of both BGMI and GMI circuit.

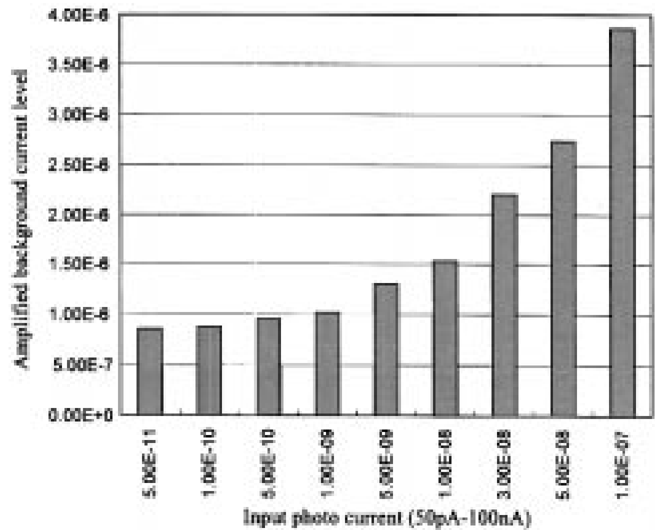

Fig. 9. The amplified background current level of the BGMI with different input photo current from 50 pA to 100 nA.

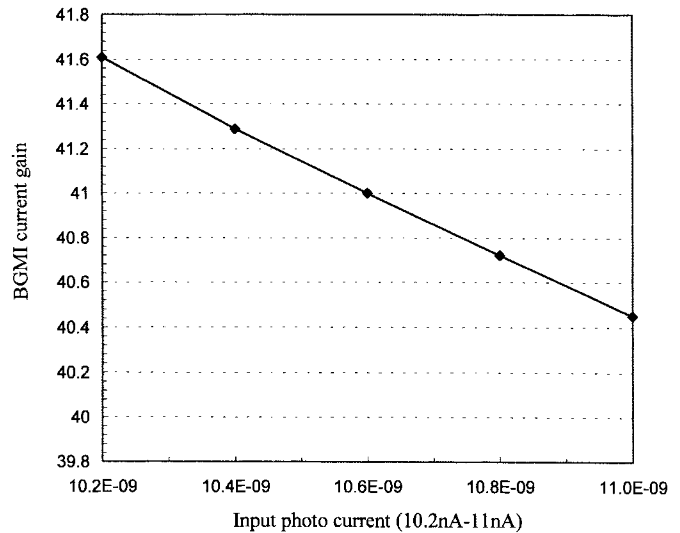

Fig. 10. The optimized current gain at 10 nanoamps background current.

column number N and the reset signal. The integration time is defined as the low level time interval between two column reset signals of ϕ_{Reset} as shown in Fig. 7. The integration capacitor is reset immediately after it is sampled. After all pixels in the upper row of integration cells have been read out, the *2-to-1 select bar* is high and the columns of lower row of integration cell are sampled to the common output stage serially. This alternative data sample of odd–even rows can achieve a continuous no-dead-time readout. The integration time is limited to about $N \times T_{\text{pixel}}$ and defined by the frame rate. When the Nth row is selected, the row select signal is used to form the end-of-frame signal which indicates the first frame has been read out. Then the second frame is ready to be read out.

III. Simulation and Experimental Results

The simulations are performed at 77K by using the SPICE low-temperature device parameters of 0.8 μm double-poly double-metal (DPDM) CMOS process. The simulated adaptive current gains versus the input photo current I_{photo} in both BGMI and GMI circuits are shown in Fig. 8. As may be seen from Fig. 8, the gain of BGMI circuit can be changed from 20 to more than 400 for a large range of the background current level from 100 nA to 50 pA. Moreover, the current gain is nearly inversely proportional to the square root of input photo current in the range of small I_{photo}. It is also shown in Fig. 8 that the adaptive gain of GMI is degraded by the limited injection efficiency at low input current level with the detector shunt resistance of 100 kΩ. As the input photo current becomes large, the constant terms of the numerator in the gain of BGMI in (13) become much less significant than the term $\sqrt{I_{\text{load}}/K_{\text{load}}}$. It causes the deviation from the $-1/2$ slope line as shown in Fig. 8.

The amplified background current level is shown in Fig. 9 where the maximum background suppression current is about 4 μA with 100 nA input photo current. The additional power dissipation of 128 $\times$ 128 BGMI readout due to the current-mode background suppression circuit is less than 6 mW with 100 nA background flux. Under the charge capacity consideration, the design of BGMI circuit is optimized at 10 nA background current with 10% signal level and the total current gain is about 40 as shown in Fig. 10.

Both integration voltage waveforms $V(C_{int})$ on the integration capacitor during the integration time $T_{int} = 128$ μs and output waveforms V_{output} in the common output stage with different input current are simulated and shown in Fig. 11. In the simulation, the total input currents are 10.2, 10.4, 10.6, 10.8, and 11 nA; the integration capacitance is 2 pF; and the background suppression current is 0.4 μA. As may be seen from Fig. 11, the maximum output excursion can reach 2 V under 5 V power supply, which is due to the proper design by using the P-P type cascade source-followers. The simulation readout speed can reach 1 MHz under 40 mW power dissipation at 40 pF output loading and 5 V supply with 128 $\times$ 128 format. The maximum readout speed can be as high as 2 MHz to fit different system requirements.

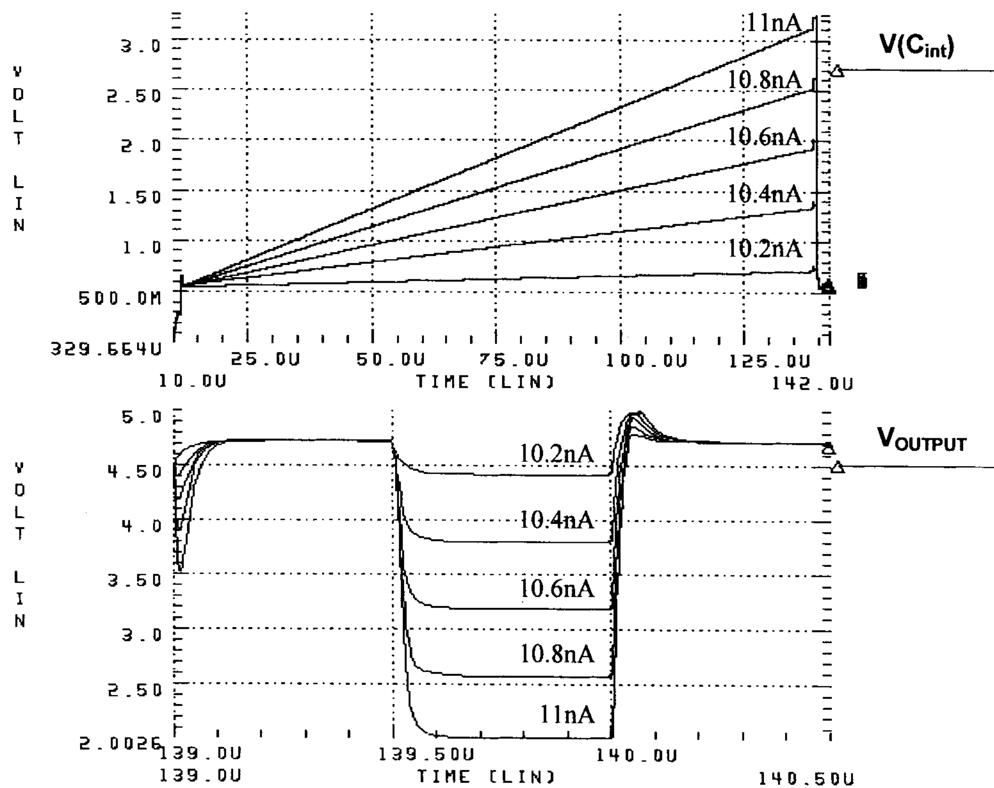

Fig. 11. The simulated waveforms of $V(C_{int})$ on integration capacitor and V_{output} in the common output stage with input currents from 10.2 to 11 nA with a 0.2 nA step.

Since both SBDI and current mirror are used in the BGMI readout circuit, the input referred noise can be reduced effectively as the BDI readout circuit [8]. Under 2 MHz readout speed and 4 pF integration capacitor, the noise charges of the BGMI circuit is estimated as 10^4 electrons. The total dynamic range can be over 70 dB.

An experimental 128 × 128 BGMI readout chip has been designed and fabricated by using 0.8 μm double-poly double-metal (DPDM) n-well CMOS technology. The photograph of the experimental readout chip is shown in Fig. 12. The layout arrangement is based on the previously proposed SCI structure [6] with two rows of shared integration cells. The 2 × 128 shared integration cells are placed at the top of the chip. The integration capacitor is 2 pF and can be extended to 4 pF by a MOS switch. Thus this chip can handle a wide range of input photo flux from picoamps to hundreds of nanoamps. Some noise shielding techniques for mixed-mode IC's such as the separation of the analog and digital power supplies, the different analog and digital ground lines, the independent substrate bias line, and the lowpass filters of input pads have been adopted in the BGMI readout chip design.

The experimental 128 × 128 BGMI chip is designed to work under 5 V power supply and 77K environment. The chip is packaged properly in a vacuum dewar and tested under cryogenic environment with liquid hydrogen as cooling source. All power supplies and voltage biases are provided from a separate board. The maximum charge capacity can achieve 9.5 $\times 10^7$ electrons by designing a 4 pF integration capacitance.

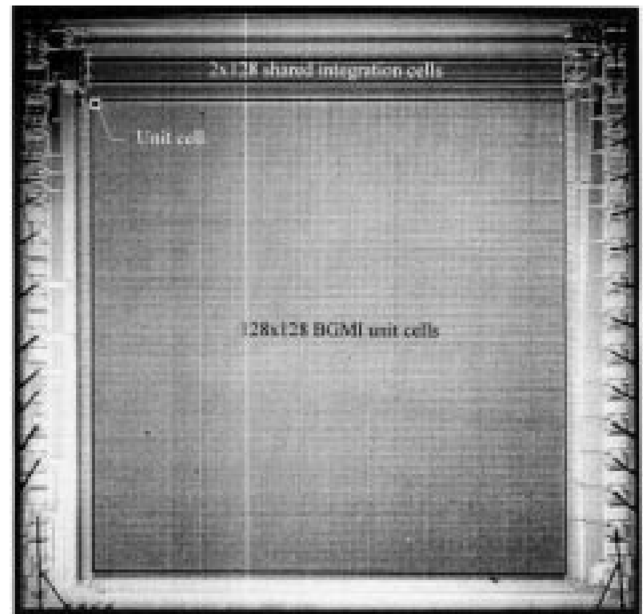

Fig. 12. The photograph of the fabricated 128 × 128 BGMI chip.

On-chip testing current sources are used to simulate the photocurrents of IR detectors.

In Fig. 13, the waveforms of the output voltage V_{output} in two frame cycles are measured with 128 end-of-row signals and one end-of-frame signal in each frame cycle. The measured no-dead-time data readout waveforms of V_{output} during the Nth row selection period with the end-of-row signal are

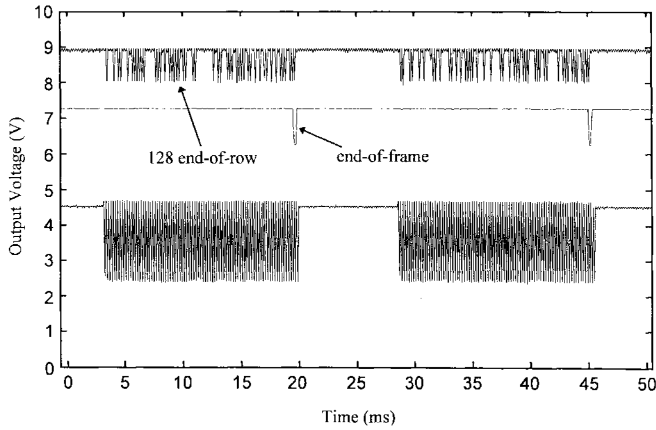

Fig. 13. The measured $V_{\rm output}$ waveforms of the fabricated 128 $\times$ 128 BGMI readout chip at 77K during the two-frame period with the 128 end-of-row signals and one end-of-frame signal in each frame period.

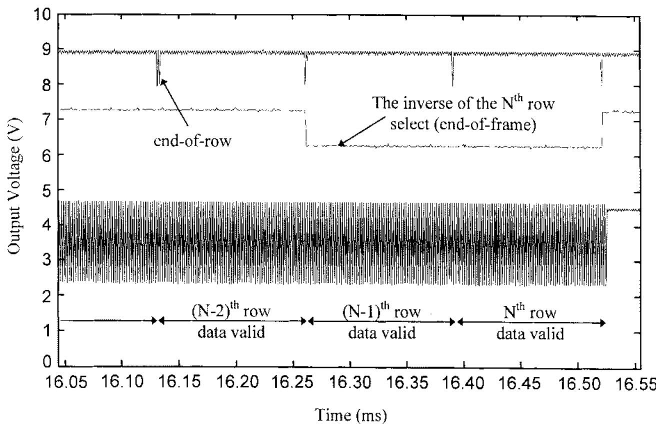

Fig. 14. The measured no-dead-time readout $V_{\rm output}$ waveforms of the fabricated 128 $\times$ 128 BGMI readout chip at 77K during the Nth row selection period with the end-of-row signal.

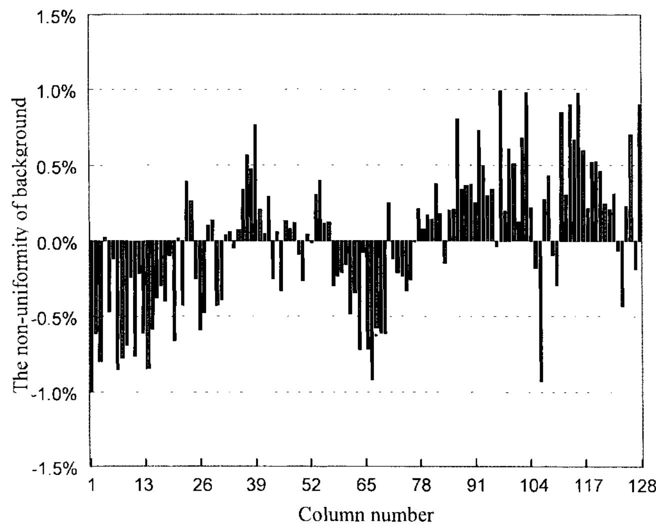

Fig. 15. The measured nonuniformity of background suppression currents in the fabricated 128 $\times$ 128 BGMI readout chip at 77K with the suppression level 1.5 μA.

shown in Fig. 14. Fig. 15 shows the measured nonuniformity of background suppression currents in the fabricated 128 $\times$ 128 BGMI readout chip at 77K with the suppression level 1.5

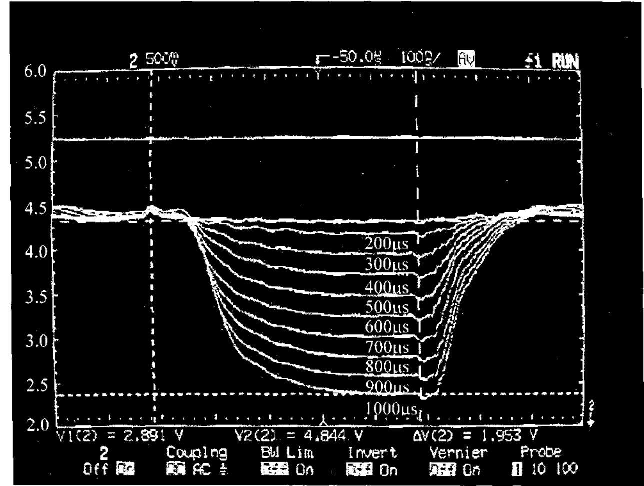

Fig. 16. The measured $V_{\rm output}$ waveforms of a single pixel on the readout chip at 77K for different integration times from 300 to 1000 μs.

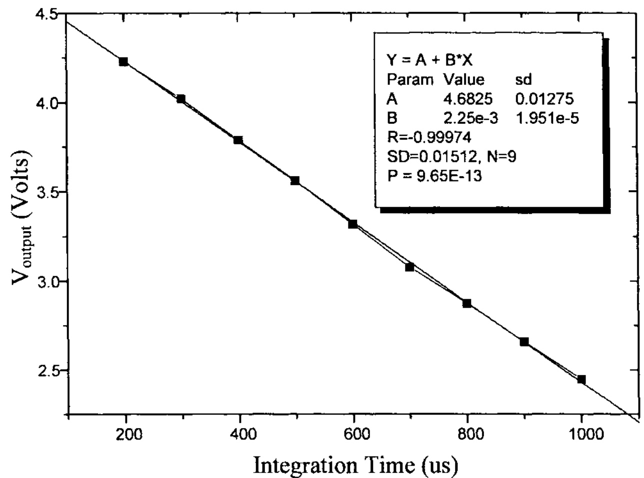

Fig. 17. The measured linearity of the 128 $\times$ 128 BGMI readout chip at 77K.

μA. It can be seen from Fig. 15 that the deviation is within 1%. Since the background current to be suppressed is large, the required $V_{\rm Tune}$ should be large enough. Large $V_{\rm Tune}$ leads to good current uniformity.

The measured $V_{\rm output}$ waveforms of a single pixel under different integration times from 200 to 1000 μs are shown in Fig. 16. The maximum output swing is 2 V as shown in Fig. 16. Fig. 17 shows the measured $V_{\rm output}$ versus the integration time from 200 to 1000 μs. It is seen from Fig. 17 that the linearity performance of the BGMI readout chip is better than 99%. The measured performance parameters of the fabricated BGMI readout chip are summarized in Table I. The readout speed is 1 MHz and can achieve 2 MHz to fit different system requirements. The transimpedance can be as high as 2.5×10^9 Ω with an adaptive current gain 40 at 10 nA background current. The total active chip power dissipation is below 40 mW at 77K.

IV. Conclusions

In this paper, the high-performance buffered gate modulation input (BGMI) circuit for IR FPA image readout has

TABLE I
TEST RESULTS AND OPERATION CONDITIONS FOR THE FABRICATED 128 × 128 BUFFERED GATE MODULATION INPUT (BGMI) READOUT CHIP

Parameter	Results
Operating temperature	77° K
Power supply	0-5 Volts
Pixel pitch	50x50 μm^2
Maximum output swing	2 Volts
Maximum charge capacity	9.5x10^7 e$^-$
Maximum readout speed	2M Hz
Background suppression uniformity	99%
Linearity	99 %
Transimpedance (at 10nA background)	2.5x10^9 ohms
Active power dissipation	40m Watts
Adaptive gain control	yes
Technology	0.8μm DPDM n-well CMOS

been proposed and analyzed. By using the proposed BGMI circuit with current-mode background suppression, shared-buffer techniques, GMI-like current-gain configuration, and other design techniques in the readout circuit of IR FPA, good injection efficiency, stable detector bias, good threshold-voltage immunity, high charge detection sensitivity, and large dynamic range can be achieved in 50×50 μm^2 pixel size. The good readout performance and adaptive gain control make it suitable for IR FPA readout applications with large background level range. The function and performance of the proposed new BGMI readout structure has been verified by both SPICE simulation results and measurement results on an 128×128 experimental chip.

ACKNOWLEDGMENT

The authors would like to thank the Chung Shang Institute of Science and Technology and the Chip Implementation Center of National Science Council, R.O.C., for their valuable discussions, suggestions, and support.

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Chih-Cheng Hsieh was born in Taichung, Taiwan, in 1967. He received the B.S. and Ph.D. degrees in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1990 and 1997, respectively.

His research interests include analog integrated circuits and system design and infrared readout integrated circuits design.

Chung-Yu Wu (M'76–SM'96–F'98) was born in Chiayi, Taiwan, in 1950. He received the M.S. and Ph.D. degrees in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1976 and 1980, respectively.

From 1980 to 1984, he was an Associate Professor at National Chiao-Tung University. During 1984–1986, he was a Visiting Associate Professor in the Department of Electrical Engineering, Portland State University, Portland, OR. Since 1987, he has been a Professor at the National Chiao-Tung University. From 1991 to 1995, he was rotated to serve as Director of the Division of Engineering and Applied Science in the National Science Council. Currently, he is the Centennial Honorary Chair Professor at the National Chaio-Tung University. He has published more than 200 technical papers on several topics, including digital integrated circuits, analog integrated circuits, computer-aided design, neural networks, ESD protection circuits, special semiconductor devices, and process technologies. He also has 18 patents, including nine U.S. patents. His current research interests focus on low-voltage low-power mixed-mode integrated circuit design, hardware implementation of visual and auditory neural systems, and RF integrated circuit design.

Dr. Wu is a member of Eta Kappa Nu and Phi Tau Phi. He was awarded the Outstanding Research Award by the National Science Council in 1989 and 1995, the Outstanding Engineering Professor by the Chinese Engineer Association in 1996, and the Tung-Yuan Science and Technology Award by the Tung-Yuan in 1997.

Tai-Ping Sun was born in Taiwan in 1950. He received the B.S. degree in electrical engineering from Chung Cheng Institute of Technology, Taiwan, in 1974, the M.S. degree in material science engineering from National Tsing Hua University, Taiwan, in 1977, and the Ph.D. degree in electrical engineering from National Taiwan University in 1990.

From 1977 to 1997, he worked at the Institute of Science and Technology, R.O.C., on the development of infrared devices, circuits, and systems. He joined the Department of Management Information System, Chung-Yu College of Business Administration, in 1997 as a Professor. His research interests have been in infrared detector and system, analog/digital mixed-mode integrated circuit design, and special semiconductor sensors and their applications.

Far-Wen Jih was born on February 25, 1961, in Taiwan. He received the B.S. and M.S. degrees in from the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1983 and 1985, respectively.

He is currently a Deputy Director of Opto-Electronics Devices Section of Materials R&D Center, Chung-Shang Institute of Science & Technology, Taiwan. His research interests include infrared device measurement technology, image readout IC design, and thermal image systems.

Ya-Tung Cherng (M'95) received the B.S. degree in physics from Chung Cheng Institute of Technology and the M.S. degree in solid state science from Syracuse University, Syracuse, NY. He received the Ph.D. degree in materials science and engineering from the University of Utah, Salt Lake City, in 1988.

He joined the Materials R&D Center (MRDC), Chung Shan Institute (CSIST), Taiwan, in 1974. He is currently Director of Opto-Electronic Device Section of MRDC, CSIST, where he is responsible for infrared sensor and image system developments. He has been involved in the IR sensor and E-O system design, analysis, and testing for more than 20 years. His professional interests are in compound semiconductors, sensor process and characterization, and E-O system design and testing.