Investigation of Oxide Charge Trapping and Detrapping in a MOSFET by Using a GIDL Current Technique

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***Abstract*— We proposed a new measurement technique to investigate oxide charge trapping and detrapping in a hot carrier stressed n-MOSFET by measuring a GIDL current transient. This measurement technique is based on the concept that in a MOSFET the Si surface field and thus GIDL current vary with oxide trapped charge. By monitoring the temporal evolution of GIDL current, the oxide charge trapping/detrapping characteristics can be obtained. An analytical model accounting for the time-dependence of an oxide charge detrapping induced GIDL current transient was derived. A specially designed measurement consisting of oxide trap creation, oxide trap filling with electrons or holes and oxide charge detrapping was performed. Two hot carrier stress methods, channel hot electron injection and band-to-band tunneling induced hot hole injection, were employed in this work. Both electron detrapping and hole detrapping induced GIDL current transients were observed in the same device. The time-dependence of the transients indicates that oxide charge detrapping is mainly achieved via field enhanced tunneling. In addition, we used this technique to characterize oxide trap growth in the two hot carrier stress conditions. The result reveals that the hot hole stress is about 10^4 times more efficient in trap generation than the hot electron stress in terms of injected charge.**

***Index Terms*—GIDL, hot carrier, oxide trap, transient.**

I. Introduction

OXIDE trap creation due to hot carrier stress has been recognized as a major reliability issue in submicron CMOS and flash EEPROM technologies [1]–[4]. For example, threshold voltage shift, stress induced oxide leakage current [3], [4], and oxide wearout are all related to oxide trap generation. Previous studies have shown that the stress generated oxide traps can be easily charged and discharged [5], [6] and the trap occupation factor is closely related to a device bias history [7]. Various device instabilities resulting from oxide charge trapping/detrapping have been reported such as time-dependent gate current [6], [8], subthreshold current [9], and GIDL current [10] at a DC bias. In the past, physics and characteristics of oxide charge trapping/detrapping mechanisms have been extensively studied. Threshold voltage shift measurement was widely adopted to monitor the variation of oxide trapped charge. However, this approach may not be appropriate for hot carrier stress generated oxide traps since part of the traps are located deep in the n^+ drain region and the threshold voltage method can hardly detect these traps. In addition, a threshold voltage shift is a resultant effect of both trapped charges at the Si/SiO_2 surface and in bulk oxide. One cannot distinguish oxide charge from interface charge by using the threshold voltage method. Furthermore, threshold voltage is only linearly dependent on trapped charge and thus may not be sufficiently sensitive to oxide charge variation.

In this work, we have developed a transient GIDL technique to investigate oxide charge trapping and detrapping [11], [12]. The unique feature of this technique is to allow a direct and continuous observation of charge exchange between gate oxide and neighboring silicon. Because interface traps and oxide traps have a wide separation in time-constants by several orders of magnitude, charge detrapping from oxide traps can be differentiated in this method by appropriately choosing a time scale. As compared to the threshold voltage method, this new technique not only can probe oxide traps in the n^+ drain region for band-to-band tunneling takes place in a certain range of substrate doping (about 5×10^{18} cm^{-3} [13]), but also provides a better measurement resolution due to an exponential dependence of GIDL current on oxide charge. Moreover, since the threshold voltage in a n-MOSFET is not affected by localized positive oxide charge, this technique has an advantage over the threshold voltage method in characterizing oxide traps created by hot hole stress, which are usually found in flash EEPROM operation [14].

The concept of the GIDL technique is illustrated in Fig. 1. In the figure, a hot carrier stressed n-MOSFET is biased in a GIDL condition, i.e., a negative gate bias and a positive drain bias. The band diagrams before and after oxide charge detrapping are represented by the solid line and the dashed line, respectively. Here, negative oxide charge is assumed in the figure. Due to an increased band-to-band tunneling distance after negative charge detrapping, the GIDL current is reduced. Therefore, by monitoring the temporal evolution of GIDL current, we can deduce escaping charge density and the associated charge detrapping rate.

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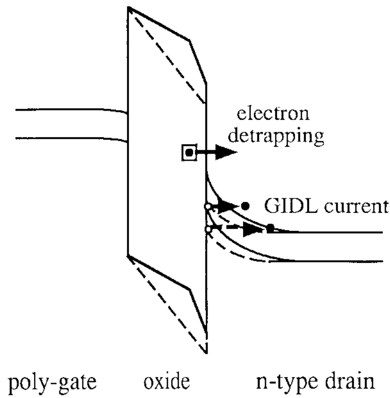


Fig. 1. Illustration of oxide charge detrapping induced GIDL current variation. The band diagrams before and after negative oxide charge detrapping are shown by the solid line and the dashed line, respectively.

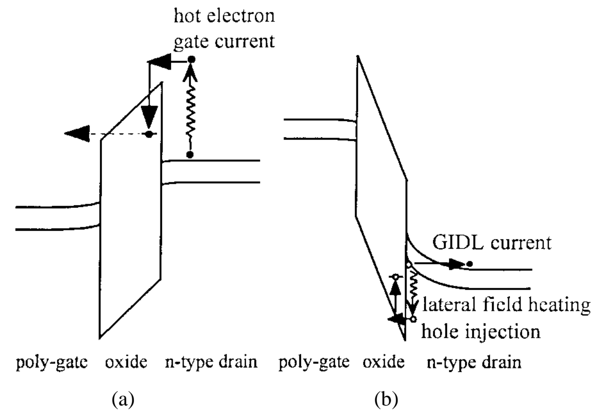


Fig. 2. Illustration of channel hot carrier injection and oxide trap filling: (a) electron filling: channel hot electron injection and (b) hole filling: band-to-band tunneling induced hot hole injection.

II. Method of Measurement

The measurement technique consists of three major steps, oxide trap creation, oxide trap filling and oxide charge detrapping. The sample device is a conventional S/D n-MOSFET with a gate length of 0.6 μm and a gate width of 25 μm. The oxide thickness is around 100 Å. The device was stressed by channel hot electron injection, $V_{\rm ds} = 5$ V and $V_{\rm gs} = 8$ V, for 2500 s and subsequently by band-to-band tunneling induced hot hole injection, $V_{\rm ds} = 6$ V and $V_{\rm gs} = -5$ V, for 300 s. After the stress, oxide trap generation was almost saturated and the generated oxide traps have two different polarities, i.e., electron traps and hole traps. The generated oxide traps were then filled with electrons or holes. This step is important since only charged traps can be detected by an electrical measurement.

The procedure of electron trap filling is illustrated in Fig. 2(a), where the device is biased in a weak channel hot electron injection condition. A small hot electron gate current is used to fill oxide traps by electron thermal capture. Two conflicting mechanisms should be considered with respect to the effectiveness of the filling. One is trap filling by capture of injected electrons [solid line in Fig. 2(a)]. The other is trap emptying due to trapped electron field emission to the gate [dashed line in Fig. 2(a)]. The latter mechanism becomes increasingly important at a higher oxide field and may decrease electron occupation of the traps. Mechanisms of hole filling are shown in Fig. 2(b). A GIDL bias with a large $V_{\rm ds}$ is applied. By lateral field heating, the band-to-band tunneling generated holes can gain much energy and inject into gate oxide.

The band diagram of oxide electron detrapping near the Si/SiO_2 surface is shown in Fig. 3(a). The oxide traps are prefilled with electrons and a GIDL bias is applied. A modest $V_{\rm ds}$ is used to minimize lateral field heating and possibly hot hole injection. In general, oxide charge detrapping may occur by means of four mechanisms, thermal emission, field emission, photoemission, or impact ionization. Photoemission is not considered as there are no radiation sources during measurement. The charge detrapping by impact ionization was found to be insignificant in thin gate oxide (<500 Å) devices [15]. Thermal emission only prevails for traps with shallow energy levels, for example, $E_t < 1.0$ eV [16] at a weak oxide field. In our measurement condition, a relatively strong oxide field in the vertical direction exists due to a large drain-to-gate bias ($V_{\rm dg}$). Thus, trapped electron field emission to the n-type drain should be the dominant mechanism. As a result of electron detrapping, both the oxide field and the silicon surface field decrease and the GIDL current decays with time.

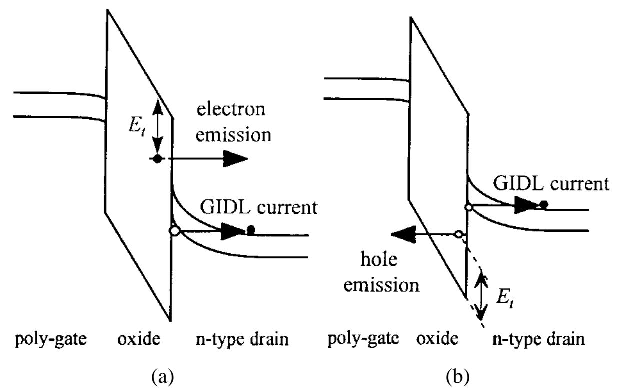


Fig. 3. Schematic band diagrams of oxide charge detrapping: (a) electron detrapping and (b) hole detrapping. A modest $V_{\rm ds}$ was used to minimize lateral field heating.

In order to compare both the electron and hole detrapping characteristics, the same GIDL bias is applied in hole detrapping in Fig. 3(b) except that the oxide traps are pre-filled with holes. The schematic band diagram for hole detrapping is drawn in Fig. 3(b). Under this condition, the vertical oxide field causes trapped hole emission to the n^+ poly gate. As a consequence, the GIDL current increases with time.

III. Modeling of GIDL Transient

The dependence of GIDL current on a silicon surface field E_s is expressed below [17]

$$I_d = AE_s \exp(-B/E_s) \tag{1}$$

where the parameters A and B are defined in [17]. A surface field change ΔE_s resulting from hot carrier stress created oxide charge is

$$\Delta E_s = \int_0^{t_{\rm ox}} \frac{t_{\rm ox} - x}{\epsilon_{\rm Si} t_{\rm ox}} Q(x)\, dx \equiv \frac{Q_{\rm eff}}{\epsilon_{\rm Si}} \tag{2}$$

where $t_{\rm ox}$ is the gate oxide thickness, $\epsilon_{\rm Si}$ is the silicon dielectric constant and $Q(x)$ is the oxide charge volumetric concentration. $Q_{\rm eff}$ is defined as the equivalent areal density considered at the Si/SiO$_2$ surface. Assuming that ΔE_s is small compared with E_s and using Taylor's expansion in (1), the GIDL current variation after stress is shown in the following:

$$\begin{aligned} I_d(\text{post-stress}) &= A[E_s + \Delta E_s] \exp\left(-\frac{B}{E_s+\Delta E_s}\right) \\ &= AE_s[1+\Delta E_s/E_s] \exp(-B/E_s) \\ &\quad \cdot \exp\left(\frac{B}{E_s^2}\Delta E_s\right) \\ &\simeq I_d(\text{pre-stress}) \exp\left(\frac{BQ_{\rm eff}}{\epsilon_{\rm Si}E_s^2}\right). \end{aligned} \tag{3}$$

Therefore, the stress created oxide charge $Q_{\rm eff}$ can be evaluated from the measured pre-stress and post-stress GIDL currents as follows:

$$Q_{\rm eff} = \frac{\epsilon_{\rm Si}E_s^2}{B} \ln\left[\frac{I_d(\text{pre-stress})}{I_d(\text{post-stress})}\right]. \tag{4}$$

It is noteworthy that 1) the GIDL current is more sensitive to oxide charge near the Si/SiO$_2$ surface for the term $(t_{\rm ox} - x)$ in (2) and 2) the GIDL current I_d exhibits an exponential dependence on oxide charge $Q_{\rm eff}$. A small variation of trapped charge can give rise to a significant change of the GIDL current.

In oxide charge detrapping, assuming that the trap time-constant is $\tau(x)$, the oxide charge detrapping rate is

$$\frac{dQ(x,t)}{dt} = -\frac{Q(x,t)}{\tau(x)}. \tag{5}$$

Solving (5), we have

$$Q(x,t) = Q(x,0)\exp[-t/\tau(x)] \tag{6}$$

and

$$\begin{aligned} \Delta Q_{\rm eff}(t) &\equiv Q_{\rm eff}(0) - Q_{\rm eff}(t) \\ &= \int_0^{t_{\rm ox}} \frac{t_{\rm ox}-x}{t_{\rm ox}} Q(x,0)\{1-\exp[-t/\tau(x)]\}\,dx. \end{aligned} \tag{7}$$

Substituting (7) into (3), the time-dependence of the GIDL current evolution in the detrapping process is derived

$$\ln[I_d(t)] = \ln[I_d(0)] + (B/\epsilon_{\rm Si}E_s^2)\Delta Q_{\rm eff}(t). \tag{8}$$

At a small oxide field, oxide charge can escape via a trapezoidal barrier tunneling. By assuming a single trap energy E_t and neglecting local distortion of the electric field due to the trapped charge, $\tau(x)$ is given by [18]

$$\tau(x) = \tau_o \exp\left\{\frac{4\sqrt{2m^*}}{3\hbar qE_{\rm ox}}\left[E_t^{3/2} - (E_t - qE_{\rm ox}x)^{3/2}\right]\right\} \tag{9}$$

where $E_{\rm ox}$ is the oxide field, m^* is the charge tunneling effective mass and other variables have their usual definitions. Substituting (7) and (9) into (8), it can be shown in the Appendix that the GIDL transient at a small detrapping oxide field follows a power-law time-dependence, i.e.,

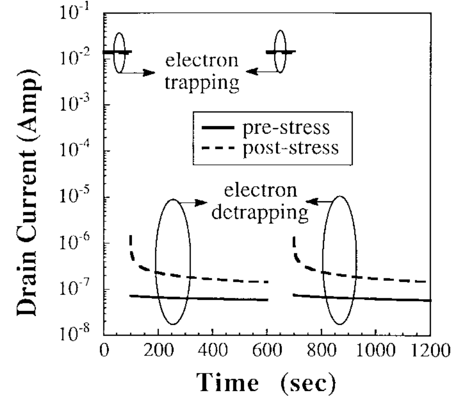


Fig. 4. Temporal evolutions of pre-stress and post-stress drain currents in the electron trapping and detrapping phases. Trapping phase: $V_{\rm ds} = 3.5$ V and $V_{\rm gs} = 6$ V, detrapping phase: $V_{\rm ds} = 3$ V and $V_{\rm gs} = -4$ V. The trapping/detrapping cycle repeats two times.

$$I_d(t) \propto t^n \quad \text{with} \quad n \simeq \frac{B\overline{Q}}{\alpha\epsilon_{\rm Si}E_s^2} \tag{10}$$

where $\alpha = 2(2m^*E_t/\hbar^2)^{1/2}$ and $\overline{Q}$ denotes an average oxide charge concentration. The power factor n is positive for hole detrapping and negative for electron detrapping.

IV. Results and Discussions

A. Oxide Charge Trapping and Detrapping

Fig. 4 shows the measured pre-stress (solid lines) and post-stress (dashed lines) drain currents in the electron trapping (filling) and detrapping phases. The bias conditions were $V_{\rm ds} = 3.5$ V and $V_{\rm gs} = 6$ V in the trapping phase and $V_{\rm ds} = 3$ V and $V_{\rm gs} = -4$ V in the detrapping phase. Apparently, the pre-stress GIDL current remains almost unchanged with time. In contrast, the post-stress GIDL current is greatly enhanced and its transient behavior becomes particularly pronounced. The transient phenomenon can be explained by two possible mechanisms, oxide electron emission or channel hot hole injection induced hole-trapped electron recombination. As pointed out previously, a modest $V_{\rm ds}$ of 3 V was used. Lateral field enhanced hot hole injection is unlikely to happen and the observed transient should be attributed to oxide electron emission. This result is different from the conclusion by Cheng *et al.*, at a large $V_{\rm ds}$ [10] that the GIDL current transient is mainly caused by hot hole injection. It should be noted that the measured transient sustains for tens of seconds. While interface traps have time-constants on an order of microseconds, the observed transient on the scale of tens of seconds is certainly due to oxide trap discharging only. In Fig. 4, the electron trapping/detrapping cycle repeats two times. No noticeable difference in the pre-stress drain current was observed between the two cycles, which implies negligible stress effect in the measurement itself. Here, an electron filling time of 100 s is sufficient since the drain current in the detrapping phase is nearly unchanged when the filling time is prolonged.

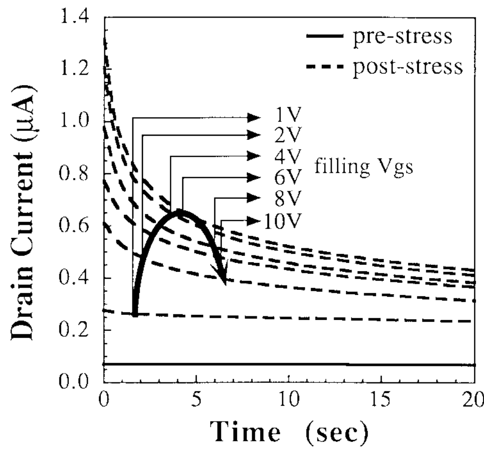


Fig. 5. Dependence of the GIDL transient on an electron filling bias. Electron filling bias: $V_{\rm ds} = 3.5$ V and $V_{\rm gs} = 1$–10 V. GIDL measurement bias: $V_{\rm ds} = 3$ V and $V_{\rm gs} = -4$ V.

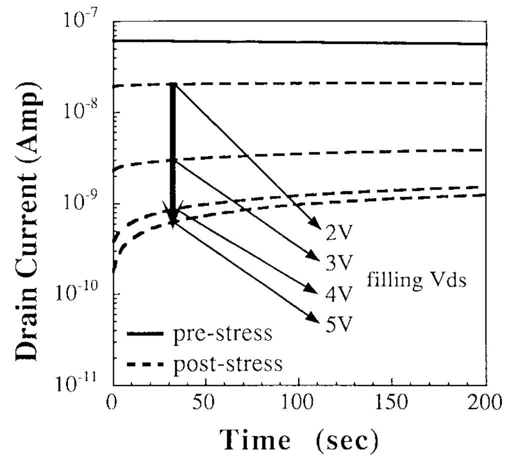


Fig. 7. Dependence of the GIDL transient on a hole filling bias. Hole filling bias: $V_{\rm dg} = 11$ V and $V_{\rm ds} = 2$–5 V. GIDL measurement bias: $V_{\rm ds} = 3$ V and $V_{\rm gs} = -4$ V.

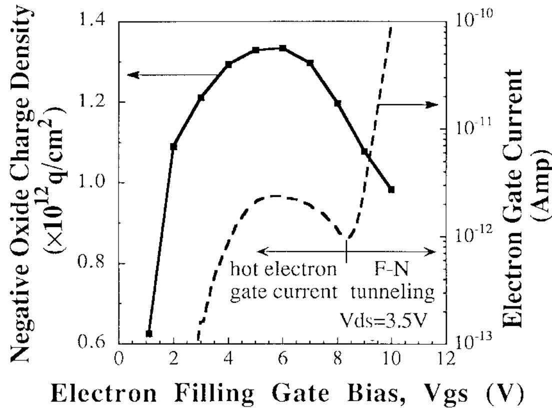


Fig. 6. Extracted negative oxide charge density versus a filling gate bias. q is the elementary charge. The dashed curve is the measured electron injection current in electron filling.

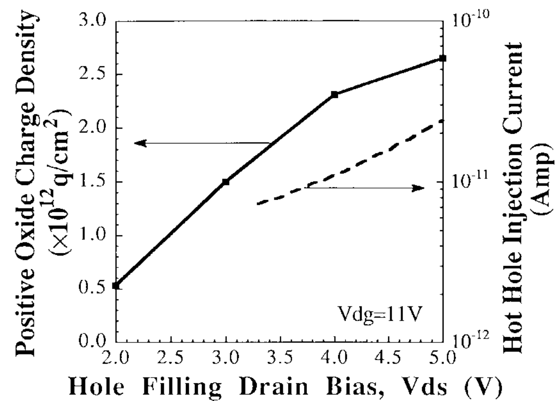


Fig. 8. Extracted positive oxide charge density versus the drain bias in hole filling. $V_{\rm dg}$ was fixed at 11 V in hole filling. q is the elementary charge. The dashed curve is the measured hole injection current in hole filling.

Furthermore, the bias effect on oxide charge trapping (oxide trap filling) was examined. In Fig. 5, we varied the gate bias in the electron filling phase and measured the corresponding GIDL transients in the detrapping phase. The result reveals that the GIDL transients exhibit a "turn-around" feature; i.e., the transient magnitude first increases with the filling gate bias and then decreases with it. The boldface arrow in Fig. 5 highlights the turn-around feature. The extracted negative oxide charge density [based on (4)] versus the filling gate bias is plotted in Fig. 6. Also shown in the figure is the measured electron gate current (dashed line). In calculation, E_s is evaluated from a two-dimensional device simulation [19] and the GIDL parameter B is about 30 MV/cm. The trapped electron density increases with the gate bias until $V_{\rm gs} \simeq 6$ V. Above that, the trap occupation factor declines due to the onset of field-enhanced electron emission from oxide traps to the gate. The maximum trapped electron density was found to be about 1.4×10^{12} cm^{-2} at $V_{\rm gs} = 6$ V.

Fig. 7 shows the oxide hole detrapping induced GIDL current transients at $V_{\rm ds} = 3$ V and $V_{\rm gs} = -4$ V with various hole filling biases. In hole filling, the drain-to-gate bias was fixed at 11 V while the drain bias was varied from 2–5 V. The extracted positive oxide charge density and the corresponding hole injection current are plotted against the filling drain bias in Fig. 8. The strong dependence of the trapped hole density and the hole injection current on the drain bias confirms that the hole injection process is related to lateral field heating. It is also worthwhile to discuss the hole current measurement in Fig. 8. As shown in the inset of Fig. 9, the measured gate current in hole filling is actually composed of two components, electron Fowler–Nordheim (FN) tunneling current (I_e) and band-to-band tunneling hole current (I_h). In Fig. 9, the gate current was measured with $V_{\rm dg} = 11$ V and $V_{\rm ds}$ from 0 to 6 V. The decline of the gate current in the low drain bias region can be explained by a decrease of the gate-to-substrate bias and consequently a decrease of the I_e. Above $V_{\rm ds} = 3$ V, the gate current is dictated by the I_h, which rises with $V_{\rm ds}$ as a result of a larger lateral field. Detailed numerical simulation and characterization of the I_e and the I_h can be found in [20].

B. Time and Field Dependences of GIDL Transient

The time-dependence of the GIDL transient at a small detrapping field was investigated in Fig. 10. In the figure, the temporal evolution of the GIDL current is plotted on a

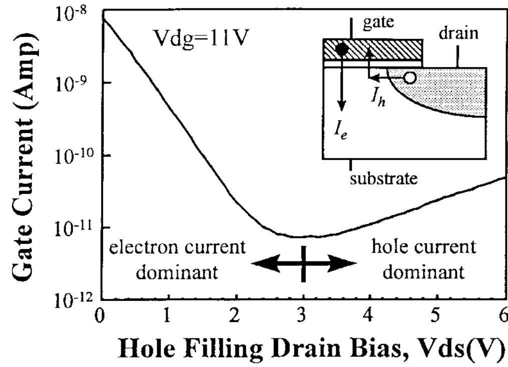


Fig. 9. Measurement of the gate current in hole filling, $V_{\rm dg} = 11$ V. The inset shows that the gate current is composed of two components, electron F–N tunneling current I_e and band-to-band tunneling induced hot hole current I_h.

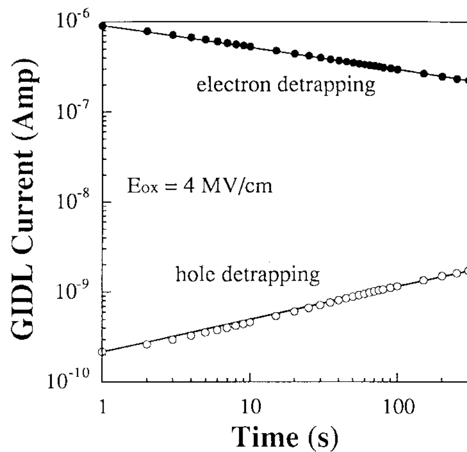
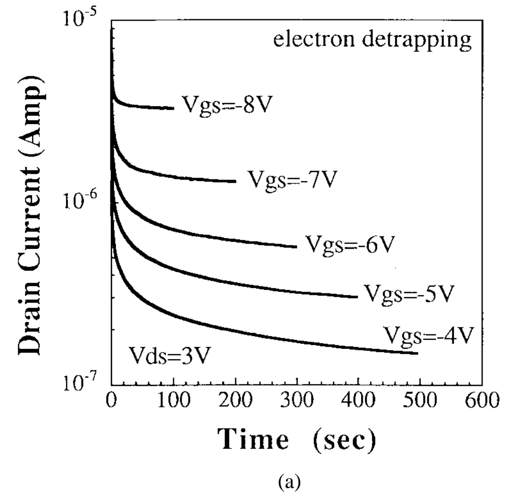
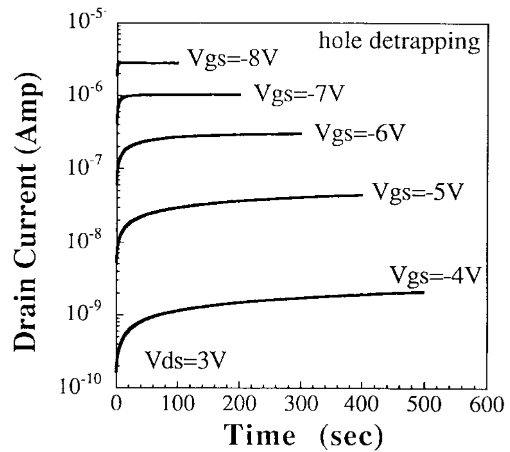


Fig. 10. The oxide charge detrapping induced GIDL current transients plotted against time on a log–log scale. The circles represent measured data points and the solid lines are the fitting curves. The oxide field in measurement is about 4 MV/cm.



(a)



(b)

Fig. 11. Dependence of the GIDL transient on a detrapping gate bias: (a) electron detrapping and (b) hole detrapping. GIDL measurement bias: $V_{\rm ds} = 3$ V and $V_{\rm gs} = -4$ to -8 V. Electron filling bias: $V_{\rm ds} = 3.5$ V and $V_{\rm gs} = 6$ V. Hole filling bias: $V_{\rm ds} = 5$ V and $V_{\rm gs} = -6$ V.

$\log(I_d) - \log(t)$ scale. The oxide field in measurement is about 4 MV/cm. Apparently, both the electron detrapping and hole detrapping induced GIDL transients follow a straight line. This characteristic agrees with the model prediction (10) and confirms that oxide charge detrapping is through field-enhanced tunneling. In addition, we noticed that the hole detrapping transient exhibits a larger slope in Fig. 10, which is realized due to a larger hole trap density in the stressed device [by comparing Fig. (6) and Fig. (8)].

By varying the gate bias in the detrapping phase, we can adjust the detrapping oxide field in the GIDL measurement. The field dependence of the GIDL transients is shown in Fig. 11. The gate bias was from -4 to -8 V and the drain bias was 3 V in the measurement. The GIDL transient magnitude, either due to electron detrapping [Fig. 11(a)] or due to hole detrapping [Fig. 11(b)], decreases as the negative gate bias (or oxide field) increases. These findings are in qualitative agreement with (8) for the oxide field is in the denominator.

Furthermore, Fig. 11 shows that as the negative gate bias increases, the time needed for the GIDL current to reach its steady state becomes shorter. In other words, the charge detrapping rate is an increasing function of an oxide field. Such field dependence also provides evidence that oxide charge detrapping is through tunneling.

C. Oxide Trap Growth Rate

The oxide trap growth characteristics by the two hot carrier stress methods was explored using this GIDL technique. The GIDL transients at different stress times were measured in Fig. 12 (hot electron stress) and in Fig. 13 (hot hole stress). Before each GIDL measurement, electron filling was performed at $V_{\rm ds} = 3.5$ V and $V_{\rm gs} = 6$ V. Therefore, only the acceptor-like oxide traps can be measured since the donor-like oxide traps are not charged when filled with electrons. The extracted oxide trap density, $N_{\rm ox} = |Q_{\rm ox}|/q$, versus injected charge is plotted in Fig. 14. The obtained growth rates follow the power–law relationship ($N_{\rm ox} = AxQ_{\rm inj}^n$) quite well [21]. The power factor n is about 0.16 for the hot electron stress and 0.11 for the hot hole stress. Moreover, our result shows that the hot hole stress is about 10^4 times more efficient in oxide trap generation than the hot electron stress in terms of injected charge.

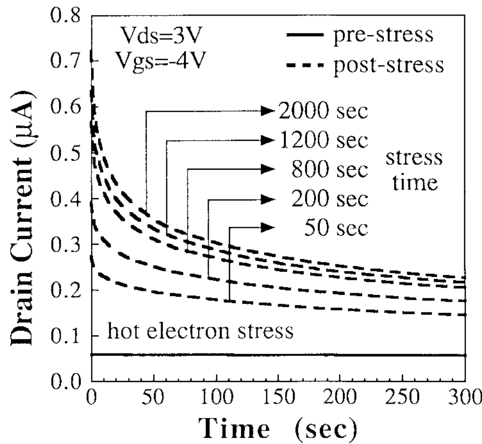


Fig. 12. Electron detrapping induced GIDL transients at different hot electron stress times. Stress bias: $V_{\rm ds} = 5$ V and $V_{\rm gs} = 8$ V. Electron filling bias: $V_{\rm ds} = 3.5$ V and $V_{\rm gs} = 6$ V.

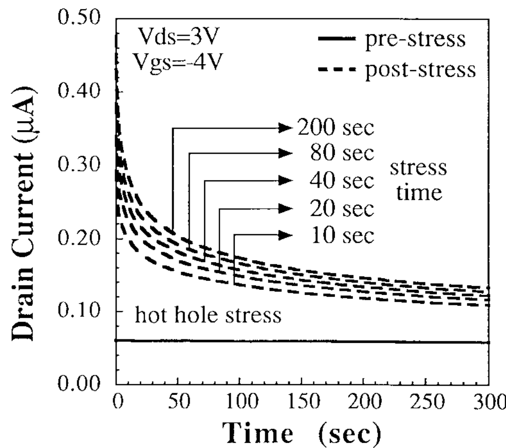


Fig. 13. Electron detrapping induced GIDL transients at different hot hole stress times. Stress bias: $V_{\rm ds} = 5$ V and $V_{\rm gs} = -5$ V. Electron filling bias: $V_{\rm ds} = 3.5$ V and $V_{\rm gs} = 6$ V.

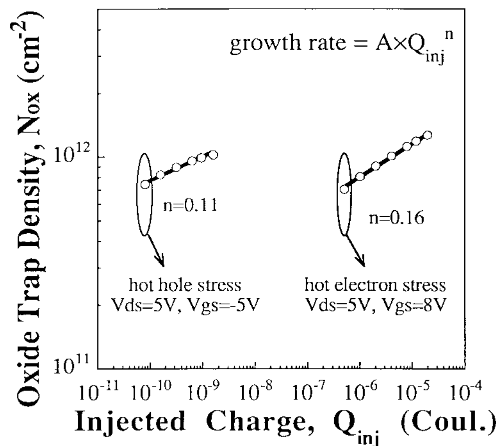


Fig. 14. The growth rates of the acceptor-like oxide traps by two hot carrier stress methods. The full circles are measured result and the solid lines are calculated from the power law, $N_{\rm ox} = AxQ_{\rm inj}^n$.

V. Conclusion

We have demonstrated a GIDL technique for oxide trap characterization in a MOSFET. The theoretical basis of this technique has been developed. This technique is shown to be very sensitive to oxide charge variation. Various oxide charge trapping and detrapping processes were characterized. Both electron detrapping and hole detrapping induced GIDL transients were observed. A power–law dependence of the transients at a small oxide has been shown. Finally, we have shown the possibility of using this technique to probe oxide trap growth characteristics under various hot carrier stress conditions.

Appendix

At a small oxide field, (9) can be reduced to $\tau(x) \simeq \tau_o \exp(\alpha x)$ with $\alpha = 2(2m^* E_t/\hbar^2)^{1/2}$. Then, (8) becomes

$$\ln[I_d(t)] = \ln[I_d(0)] + (B/\epsilon_{\rm Si} E_s^2) \int_0^{t_{\rm ox}} \frac{t_{\rm ox} - x}{t_{\rm ox}} Q(x, 0) \cdot \left\{1 - \exp\left[-\frac{t}{\tau_o} \exp(-\alpha x)\right]\right\} dx. \tag{A1}$$

Since the double exponential function $\exp[-(t/\tau_o)\exp(-\alpha x)]$ in the integrand changes abruptly from 0 to 1 around $x = \alpha^{-1}\ln(t/\tau_o)$, it can be reasonably approximated by a step-function as follows:

$$\exp\left[-\frac{t}{\tau_o}\exp(-\alpha x)\right] = \begin{cases} 0 & \text{for } x \le \alpha^{-1}\ln(t/\tau_o) \\ 1 & \text{for } x \ge \alpha^{-1}\ln(t/\tau_o). \end{cases} \tag{A2}$$

This step function approximation is actually the same as the tunneling front model used in [22], [23]. Therefore, (A1) can be further simplified

$$\begin{aligned} \ln[I_d(t)] &= \ln[I_d(0)] + (B/\epsilon_{\rm Si} E_s^2) \int_0^{\alpha^{-1}\ln(t/\tau_o)} \frac{t_{\rm ox} - x}{t_{\rm ox}} \cdot Q(x, 0)\, dx \\ &= \ln[I_d(0)] + (B/\epsilon_{\rm Si} E_s^2)\, \overline{\frac{t_{\rm ox} - x}{t_{\rm ox}} Q(x, 0)} \cdot [\alpha^{-1}\ln(t/\tau_o)] \end{aligned} \tag{A3}$$

where $\overline{(t_{\rm ox} - x)/t_{\rm ox} Q(x, 0)}$ represents an average oxide charge concentration in the stressed device. Note that the above expression holds for $t \gg \tau_o$. This condition is easily satisfied in measurement for τ_o is on an order of picoseconds [24]. By neglecting the term $\overline{(t_{\rm ox} - x)}/t_{\rm ox}$ a power–law dependence of the GIDL transient is readily obtained, i.e.,

$$I_d(t) \propto (t/\tau_o)^n$$

with the power factor n about $B\overline{Q}/\alpha\epsilon_{\rm Si} E_s^2$.

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