A Novel Process to Form Cobalt Silicided p^+ Poly-Si Gates by BF_2^+ Implantation into Bilayered CoSi/a-Si Films and Subsequent Anneal

W. K. Lai, *Student Member, IEEE*, H. W. Liu, M. H. Juang, N. C. Chen, and H. C. Cheng, *Member, IEEE*

***Abstract*—A novel process that implants BF_2^+ ions into thin bilayered CoSi/a-Si films has been shown to form cobalt silicided p^+ poly-Si gates with excellent gate oxide integrity and very small flatband shift. The effects of not only using the CoSi layer as an implantation barrier but also keeping the a-Si underlayer during the initial silicide formation both significantly suppress the boron penetration through thin gate oxide.**

I. Introduction

SURFACE-CHANNEL p-MOSFET's with p^+ poly-Si gates have been investigated [1] in place of the buried-channel devices with n^+ poly-Si gates due to superior short-channel behavior, better turn-off characteristics, lower threshold voltage operation, much less sensitivity to process tolerances [2], and improved hot-carrier reliability [3]. However, it has been reported that boron impurities from the B^+-doped poly-Si gate could readily diffuse through the gate oxide during high-temperature anneals [4]–[7]. This boron penetration can result in flat-band voltage $(V_{\rm fb})$ shift, increase of the subthreshold swing and leakage current, and deterioration of the gate oxide quality. Hence, different structures have been investigated, such as the as-deposited a-Si gate [8] in place of the poly-Si gate, the stacked a-Si (or poly-Si) gate structures [9]–[11], and various nitrided gate oxides [12]–[14], to retard the boron diffusion into underlying Si substrate.

In this letter, a novel process that forms the CoSi on the amorphous silicon layer and then implants BF_2^+ dopants into such a thin bilayer followed by an anneal is proposed to suppress the boron penetration and form a cobalt silicided poly-Si gate structure.

II. Experiments

(100) oriented, 3–5 Ω-cm, n-type Si wafers were used. Field oxides of 450 nm thickness were thermally grown for patterning the active region of metal-oxide-semiconductor (MOS) capacitors. Thin gate oxide of 8 nm thickness was grown at 900 °C in a dry O_2 ambient. Immediately, undoped a-Si and poly-Si of 100 nm thickness were deposited on respective samples by low-pressure chemical-vapor-deposition (LPCVD) at 550 and 620 °C, correspondingly. The gate electrode was patterned for the utilization of selective etching. Some specimens with poly-Si films, used as the control samples, were first BF_2^+-implanted at 40 keV to 5×10^{15} cm^{-2}. Then, thin Co films of about 13.5 nm thickness, which would form 45-nm $CoSi_2$ films, were deposited by an e-beam evaporation system for all the samples. Thin Mo films of 18 nm thickness were subsequently deposited to serve as a passivation layer for the first-step silicidation anneal. The anneal was performed at 450 °C for 60 s by rapid thermal annealing (RTA). Mo and the unreacted Co layer on field oxide were selectively removed in a 5:1:1 mixture of H_2O:H_2O_2:NH_4OH and a 6:1:1 mixture of H_2O:H_2O_2:HCl, correspondingly, at 55–60°C. After the self-aligned silicide process, the samples with bilayered CoSi/a-Si and CoSi/poly-Si films, except the control specimens, were BF_2^+-implanted at 55 keV to 5×10^{15} cm^{-2}. The second-step anneal was by RTA at temperatures ranging from 700 to 1000 °C (60 s for 700, 800, and 900 °C, and 30 s for 1000 °C). The resultant gate oxide integrity was characterized by current–voltage (I–V) and capacitance–voltage (C–V) measurements.

III. Results and Discussion

From the previous shallow-junction studies [16]–[17], the usage of CoSi as an implant barrier as well as a boron diffusion source could effectively reduce the boron diffusion. Hence, this process is supposed to retard the boron penetration through gate oxide. In addition, a-Si films are preserved during the initial silicide formation to further suppress the boron penetration [8]. The resulting sheet resistance of the polycide films decreases with increasing second-step annealing temperature and is still stable even at higher annealing temperature of 1000 °C.

Fig. 1 shows the quasi-static C–V curves for the samples with the poly-Si layer only, the bilayered CoSi/poly films, and the bilayered CoSi/a-Si films, respectively, annealed at 900 °C for 60 s. The C–V curve for the poly-Si samples is much distorted and shifted to the right as compared to the CoSi/poly and CoSi/a-Si ones, indicating a large amount of

Manuscript received January 28, 1998; revised April 1, 1998. This work was supported in part by the R.O.C. National Science Council under Contract NSC-87-2215-E-009-047.

W. K. Lai, H. W. Liu, and H. C. Cheng are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C.

M. H. Juang is with the Department of Electronics Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan, R.O.C.

N. C. Chen is with Holtek Microelectronics Inc., Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C.

Publisher Item Identifier S 0741-3106(98)04779-X.

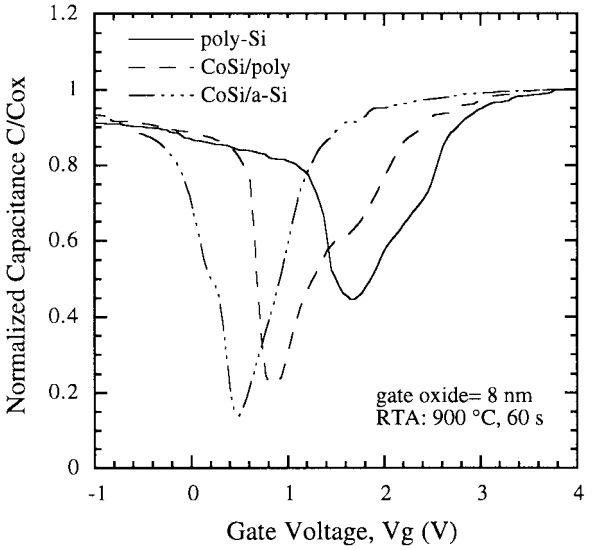

Fig. 1. Normalized quasi-static C–V curves for the specimens with poly-Si, CoSi/poly, and CoSi/a-Si films, respectively, annealed at 900 °C for 60 s.

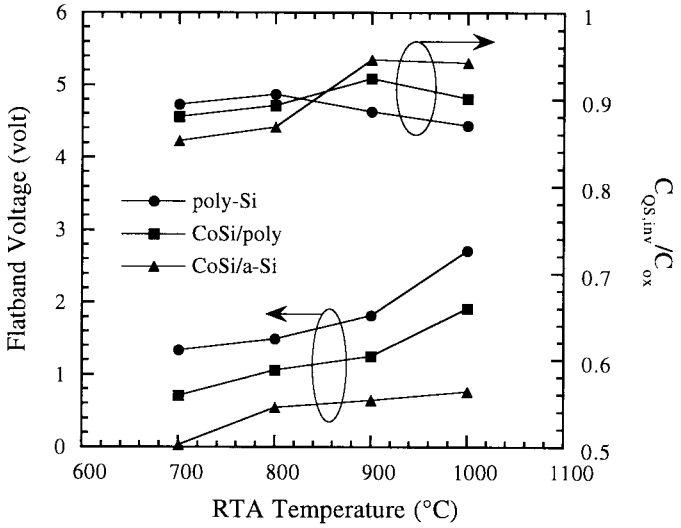

Fig. 2. Flat-band voltage $(V_{\rm fb})$ and polysilicon depletion effect, as monitored by normalized inversion capacitance $(C_{\rm QS,inv}/C_{\rm ox})$, on the specimens with poly-Si, CoSi/poly, and CoSi/a-Si films, respectively, as a function of post-implant anneal temperatures.

boron penetration has occurred [5]. In addition, a significant capacitance reduction for the poly-Si samples is found in the inverse bias region, which is caused by the gate depletion layer formation. The slightly distorted C–V curve is also observed in the CoSi/poly samples. On the other hand, such a dramatically distorted C-V curve in the poly-Si sample is not observed in the CoSi/poly and CoSi/a-Si specimens, reflecting the fact that the boron penetration is suppressed.

The implanted-dopant diffusion from the silicides into the underlying poly-Si layer should be sufficient to avoid possible polysilicon depletion effect after post-implant annealing. Boron penetration effect on $V_{\rm fb}$ and polysilicon depletion were investigated over a wide range of RTA temperatures, as shown in Fig. 2, where the poly-Si, the CoSi/poly, and the CoSi/a-Si samples were compared. Polysilicon depletion effect is monitored by plotting $C_{\rm QS,inv}/C_{\rm ox}$, where $C_{\rm QS,inv}$ (defined at $V_g - V_{\rm fb} = -2$ V) is the quasi-static inversion capacitance just prior to the deep inversion region [15] and $C_{\rm ox}$ (defined at $V_g - V_{\rm fb} = 3.2$ V) is the oxide capacitance. The $C_{\rm QS,inv}/C_{\rm ox}$ values in the CoSi/a-Si samples are much lower than the CoSi/poly ones at RTA temperatures below 800 °C. The undoped a-Si films of 100 nm thickness were deposited by LPCVD at about 550 °C. Since the first-step annealing for forming CoSi was only 450 °C, the silicide films were still amorphous after the CoSi formation. Moreover, the a-Si films have been reported to be capable of retarding the boron diffusion [8]. Therefore, the resultant doping concentration in the poly-Si layer may be inadequate and may cause the depletion effect after a low annealing temperature below 800 °C. Obviously, such a depletion phenomenon for the CoSi/a-Si specimens is greatly reduced when the annealing temperature is above 900 °C. In addition, large $V_{\rm fb}$ shifts were found in the poly-Si samples, especially at RTA temperatures above 900 °C, indicating severe boron penetration through thin gate oxide. However, the $V_{\rm fb}$ shifts were largely reduced in the CoSi/poly samples, which implied that the CoSi implantation

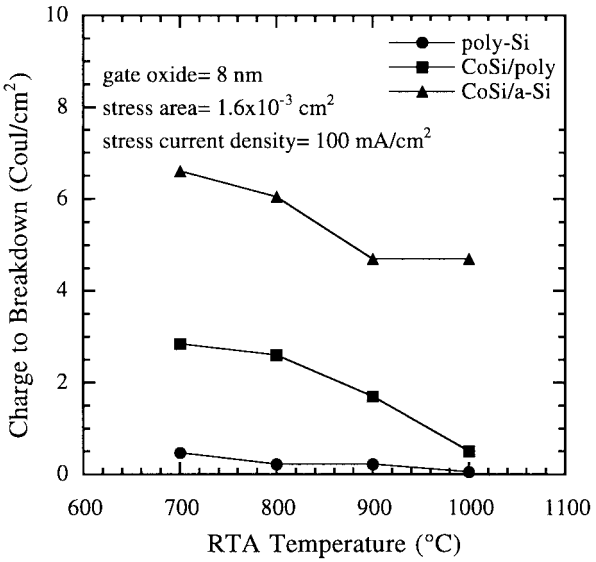

Fig. 3. Dependence of charge to breakdown $Q_{\rm bd}$ on RTA temperature for the poly-Si, CoSi/poly, and CoSi/a-Si samples, respectively.

barrier could effectively retard the boron penetration during subsequent post-implant annealing. Furthermore, the CoSi/a-Si samples exhibited significantly smaller $V_{\rm fb}$ shift, as compared to the CoSi/poly samples, attributable to considerably suppressed boron penetration. As a result, with the effective retardation of boron penetration from using CoSi as the implantation barrier, the a-Si layers could be further used to achieve even better results.

The dependences of charges to breakdown $(Q_{\rm bd})$ on RTA temperature were shown in Fig. 3. At least ten capacitors, with the area of 1.6×10^{-3} cm^2, for each sample were taken to evaluate the $Q_{\rm bd}$ measurements. The stress current density of 100 mA/cm^2 was used. The $Q_{\rm bd}$ value for the poly-Si samples

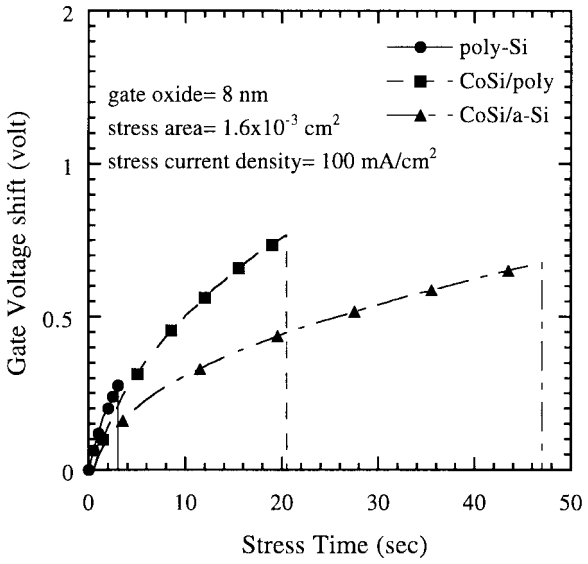

Fig. 4. Comparison of the gate voltage shift (ΔV_g) under the constant current (100 mA/cm^2) stress for the poly-Si, CoSi/poly, and CoSi/a-Si samples, respectively, annealed at 900 °C for 60 s.

was extremely low even at RTA 700 °C. It is attributed to the readily boron penetration caused by dopant implantation (40 keV) into such a thin poly-Si layer, i.e., 100 nm in thickness. However, the CoSi/poly samples could exhibit much better $Q_{\rm bd}$ value than the poly-Si samples, especially at RTA temperatures lower than 900°C. Furthermore, the CoSi/a-Si samples could achieve much better $Q_{\rm bd}$, implying the effectiveness of this process in preventing the boron penetration. In addition, Fig. 4 shows the gate voltage shifts (ΔV_g) during the constant current (100 mA/cm^2) stress for the poly-Si, CoSi/poly, and CoSi/a-Si samples, respectively, annealed at 900 °C. The electron trapping rate of gate oxide in the CoSi/a-Si samples is found to be much lower than those for the poly-Si and CoSi/poly ones, indicating the generation of less electron traps.

IV. Conclusion

In conclusion, the novel process that implants $BF_2{}^+$ dopants into thin bilayered CoSi/a-Si films and subsequent anneal has been used to form cobalt silicided p^+ poly-Si gates with excellent thin gate oxide integrity and very small $V_{\rm fb}$ shifts. Here, a low-temperature annealing to form the CoSi is required to keep the amorphous silicon underlayer, i.e., the CoSi/a-Si bilayer. Thus the usage of such bilayer films could significantly suppress the boron penetration, by combining both effects of the a-Si layer and the CoSi implantation barrier. As a result, the scheme shows good feasibility for further deep submicron dual gate CMOS technology.

Acknowledgment

The authors would thank the National Nano Device Laboratory (NDL) of R.O.C. NSC and the Semiconductor Research Center (SRC) of National Chiao Tung University for the technical support.

References

[1] G. J. Hu and R. H. Bruce, "Design tradeoffs between surface and buried-channel FET," *IEEE Trans. Electron Devices*, vol. ED-32, p. 584, 1985.
[2] K. Tanaka and M. Fukuma, "Design methodology for deep submicron CMOS," in *IEDM Tech. Dig.*, 1987, p. 628.
[3] F. Matsuoka, H. Iwai, H. Hayashida, K. Hama, Y. Toyoshima, and K. Maeguchi, "Analysis of hot-carrier-induced degradation mode on PMOSFET," *IEEE Trans. Electron Devices*, vol. 37, p. 1487, 1990.
[4] J. Y.-C. Sun, C. Wong, Y. Taur, and C.-H. Hsu, "Study of boron penetration through thin oxide with p^+-polysilicon gate," in *Proc. 1989 Symp. VLSI Technol.*, 1989, p. 17.
[5] J. R. Pfiester, F. K. Baker, T. C. Mele, H.-H. Tseng, P. J. Tobin, J. D. Hayden, J. W. Miller, C. D. Gunderson, and L. C. Parrillo, "The effects of boron penetration on p^+ polysilicon gates PMOS devices," *IEEE Trans. Electron Devices*, vol. 37, p. 1842, 1990.
[6] J. J. Sung and C.-Y. Lu, "A comprehensive study on p^+ polysilicon-gate MOSFET instability with fluorine incorporation," *IEEE Trans. Electron Devices*, vol. 37, p. 2312, 1990.
[7] C.-Y. Chang, C.-Y. Lin, J. W. Chou, C. C.-H. Hsu, H.-T. Pan, and J. Ko, "Anomalous reverse short-channel effect in p^+ polysilicon gated P-channel MOSFET," *IEEE Trans. Electron Device Lett.*, vol. 15, p. 437, 1994.
[8] C. Y. Lin, K. C. Juan, C. Y. Chang, F. M. Pan, P. F. Chou, S. F. Hung, and L. J. Chen, "A comprehensive study of suppression of boron penetration by amorphous-Si gate in p^+-gate PMOS devices," *IEEE Trans. Electron Devices*, vol. 42, p. 2080, 1995.
[9] C. Y. Lin, C. Y. Chang, and C. C. H. Hsu, "Suppression of boron penetration in BF_2-implanted p-type gate MOSFET by trapping of fluorines in amorphous gate," *IEEE Trans. Electron Devices*, vol. 42, p. 1503, 1995.
[10] S. L. Wu, C. L. Lee, and T. F. Lei, "Suppression of boron penetration induced Si/SiO_2 interface degradation by using a stacked-amorphous-silicon film as the gate structure for pMOSFET," *IEEE Trans. Electron Device Lett.*, vol. 5, p. 160, 1994.
[11] Y. H. Lin, C. S. Lai, C. L. Lee, T. F. Lei, and T. S. Chao, "Nitridation of the stacked poly-Si gate to suppress the boron penetration in pMOS," *IEEE Electron Device Lett.*, vol. 16, p. 248, 1995.
[12] Z. J. Ma, J. C. Chen, Z. H. Lin, J. K. Krick, Y. C. Cheng, C. Hu, and P. K. Ko, "Suppression of boron penetration in P^+ polysilicon gate P-MOSFET using low-temperature gate-oxide N_2O anneal," *IEEE Electron Device Lett.*, vol. 15, p. 109, 1994.
[13] L. K. Han, D. Wristers, J. Yang, M. Bhat, and D. L. Kwong, "Highly suppressed boron penetration in NO-nitrided SiO_2 for P^+-polysilicon gated MOS device applications," *IEEE Electron Device Lett.*, vol. 16, p. 319, 1995.
[14] G. Q. Lo and D. L. Kwong, "The use of ultrathin reoxidized nitrided gate oxide for suppression of boron penetration in $BF_2{}^+$-implanted polysilicon gated P-MOSFET," *IEEE Electron Device Lett.*, vol. 12, p. 175, 1991.
[15] S. W. Lee, C. Liang, C. S. Pan, W. Lin, and J. B. Mark, "A study on the physical mechanism in the recovery of gate capacitance to $C_{\rm ox}$ in implanted polysilicon MOS structures," *IEEE Electron Device Lett.*, vol. 13, p. 2, Jan. 1992.
[16] M. H. Juang, C. T. Lin, and H. C. Cheng, "Shallow junctions formed by $BF_2{}^+$ implantation into thin CoSi films and rapid thermal annealing," *J. Appl. Phys.*, vol. 76, p. 1323, 1995.
[17] H. C. Cheng, M. H. Juang, and L. M. Huang, "A silicidation-induced process consideration for forming scale-down silicided junction," *IEEE Electron Device Lett.*, vol. 15, p. 342, 1994.