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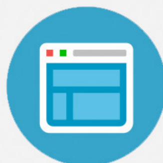
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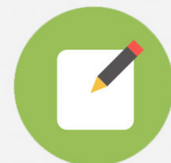

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Thermal stability of selective chemical vapor deposited tungsten contact and effects of *in situ* N_2 plasma treatment

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This work investigates the thermal stability of Al/W/p^+-n junction diodes, in which the W contact was filled using selective chemical vapor deposition to a thickness of about 450 nm and served as diffusion barrier between the Al and the Si substrate. The effects of *in situ* N_2 plasma treatment on the barrier effectiveness were also investigated. The Al/W(450 nm)/p^+-n junction diodes can sustain a 30 min furnace annealing up to 575 °C. With an *in situ* N_2 plasma treatment on the W surface caused a thin layer of WN_x to form on the W surface, and the nitrified layer of WN_x/W acting as barrier between the Al and the Si substrate effectively suppressed WAl_{12} formation at elevated temperatures, resulting in a significant barrier improvement. N_2 plasma treatment at 100 W for 300 s enabled the Al/WN_x/W(450 nm)/p^+-n junction diodes to sustain thermal annealing at temperatures up to 625 °C without degradation of electrical characteristics. © *1998 American Vacuum Society.* [S0734-211X(98)00304-7]

I. INTRODUCTION

Because Si is highly soluble in Al alloy and exhibits high diffusivity along Al grain boundaries, Al/Si contacts tend to fail due to Si dissolving in Al and Al spiking into Si substrates.[1,2] The Al–Si alloy also becomes supersaturated during cooling cycles and excess Si precipitates at the Al/Si interface, resulting in degradation of contact characteristics. Therefore, the introduction of a barrier layer between the Al metallization and the Si substrate is of fundamental importance in preventing junction spiking and avoiding contact degradation.[2]

Tungsten has been considered as a good contact barrier for protecting shallow junctions from aluminum spiking and achieving low contact resistance.[3–8] Tungsten nitride is also an effective diffusion barrier between Si and contact metals because it is chemically more stable than pure tungsten, and has a greater capacity for suppressing interdiffusion between Al and Si.[9–15] Generally, tungsten nitride is deposited by reactively sputtering a pure W target in Ar–N_2 mixed ambient.[9,10] It has been reported that reactively sputtered tungsten nitride far surpassed pure W metal as a diffusion barrier between Al and Si substrates.[9] However, it is difficult to deposit tungsten nitride with excellent barrier properties into contact holes of submicron dimension using sputtering techniques because of potential step coverage problems. In this respect, selective chemical vapor deposition of tungsten (selective CVD-W) is a most attractive technique for filling deep submicron contact holes in ultralarge scale integrated (ULSI) interconnect applications.[8]

It has been reported that a selective 73-nm-thick CVD-W film acted as an effective diffusion barrier between Al and Si substrate at 450 °C for 30 min; however, it failed at 520 °C.[6] It has also been reported that no discernible reaction took place at an Al/W interface at temperatures up to 500 °C with a W film deposited using CVD; however, reaction occurred at an Al/W interface with sputtered W even at 450 °C and a WAl_{12} compound formed.[4] Moreover, it was found that N_2 plasma treatment of a CVD-W surface before Al deposition prevents Al–W alloy formation and suppresses the increase of sheet resistance for the Al/W structure.[15] Although these studies have provided much valuable information for the application of thin CVD-W films (less than 100 nm) as diffusion barriers, nevertheless, little study has been made of the thermal stability of thicker CVD-W film.[8]

Generally, W plugs used in industry are 450 nm or more in thickness.[16] In this study, 100 and 450-nm-thick CVD-W films were selectively deposited to fill contact holes and acted as diffusion barriers between Al and Si substrates. The film resistivities of the selective CVD-W were found to be about 10 $\mu\Omega$ cm. This technique offers the advantage of producing a fully self-aligning contacts and barrier-formation processes. In addition, the resultant structures also possess more planar surfaces for subsequent metallization processing. To study the effects of N_2 plasma treatment, an *in situ* N_2 plasma treatment was performed on tungsten surfaces prior to Al metallization. After the treatment, thin WN_x layers formed on the surfaces of the W layers, which efficiently suppressed diffusion between W and Al during post-metallization thermal annealing. The results of this study might be useful in producing selective CVD-W-filled plugs for ULSI interconnection applications.

II. EXPERIMENT

To evaluate the barrier effectiveness of a selective CVD-W layer, various samples of Al/barrier/p^+-n junction diodes were prepared. The starting material was n type, ⟨100⟩-oriented Si wafers with 4–7 Ω cm nominal resistivity. After RCA standard cleaning, the wafers were thermally oxi-

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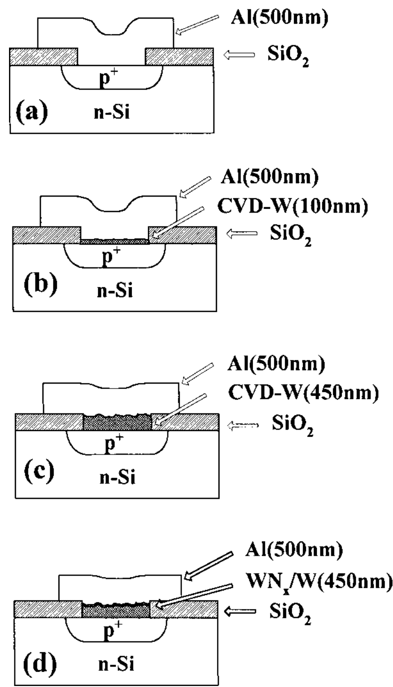

FIG. 1. Schematic cross sections of four differently metallized p^+-n junction diodes (a) Al/p^+-n, (b) Al/W(100 nm)/p^+-n, (c) Al/W(450 nm)/p^+-n, and (d) Al/WN_x/W(450 nm)/p^+-n.

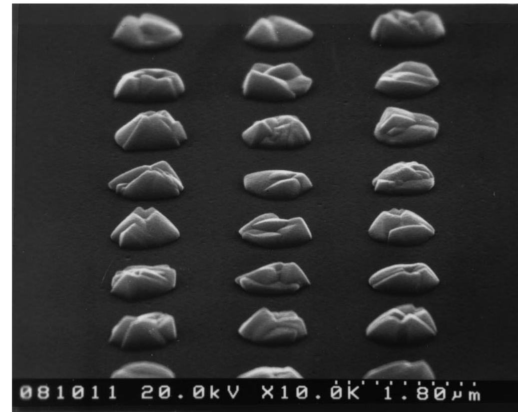

FIG. 2. SEM micrographs showing an overfilled 0.5 μm contact hole using selective CVD-W techniques.

dized to grow a 500 nm oxide layer. Diffusion areas with sizes of 500×500 and 1000×1000 μm^2 were defined on the oxide-covered wafers using conventional photolithographic techniques. The p^+-n junctions 300 nm deep were formed using BF_2^+ implantation at 30 keV to 3×10^{15} cm^{-2} followed by furnace annealing at 900 °C for 30 min in N_2 ambient.

After junction formation, the wafers were split into four groups for the preparation using various metallization structures: Al/p^+-n, Al/W(100 nm)/p^+-n, Al/W(450 nm)/p^+-n, and Al/WN_x/W(450 nm)/p^+-n. For the Al/W(100 nm)/p^+-n and Al/W(450 nm)/p^+-n diodes, the contact holes were selectively deposited with CVD-W layers of 100 and 450 nm, respectively, followed by Al metallization. For the Al/WN_x/W(450 nm)/p^+-n diodes, an *in situ* N_2 plasma treatment was performed on the selectively deposited CVD-W layers of 450 nm thickness before the Al metallization; thus, thin WN_x layers formed on the W surfaces. The schematic cross sections of these differently metallized p^+-n junction diodes are shown in Fig. 1. The contact holes in the Al/W(450 nm)/p^+-n and Al/WN_x/W(450 nm)/p^+-n diodes, were almost fully filled by selective CVD-W; this provided nearly planar surfaces for subsequent metallization processing.

Prior to selective CVD-W deposition, the wafers were dipped in dilute HF (50:1) for 30 s, followed by a rinse in deionized water for 3 min and a spin dry. The wafers were then loaded into a load-locked cold wall W-CVD system (ULVAC ERA-1000S) within 5 min and transferred to the deposition chamber without exposure to the atmosphere. The ERA-1000S is a fully automatic single wafer CVD system equipped with a cluster of multichambers, including a load/unload, buffer and two deposition chambers. This system employs a robot unit in the buffer chamber for wafer transfer in vacuum. The aluminum-alloy reactor was watercooled and was kept at a high vacuum base pressure by a turbopump. The base pressure of the CVD chamber was 1×10^{-6} Torr. In this study, W films were chemically vapor deposited using the SiH_4 reduction of WF_6 process under the following conditions: substrate temperature 300 °C, total gas pressure 100 mTorr, WF_6 flow rate 40 sccm, SiH_4 flow rate 10 sccm, and H_2 carrier gas flow rate 1000 sccm. After selective CVD-W deposition, one group of wafers was further treated with *in situ* N_2 plasma without breaking the vacuum under the following conditions: N_2 flow rate 80 sccm, total gas pressure 30 mTorr, treatment time 300 s, and plasma generation power ranging from 50 to 200 W. Finally, Al metallization was applied to all samples.

To investigate thermal stability of the differently metallized junction diodes, samples were thermally annealed in an N_2 flow furnace for 30 min at temperatures ranging from 350 to 650 °C. Electrical characteristics were measured using an HP-4145B semiconductor parameter analyzer. Unpatterned samples with various W/Si, Al/W/Si, and Al/WN_x/W/Si structures were also prepared for material analysis. Sheet resistance of the multilayer structures was measured using a four-point probe. X-ray diffraction (XRD) analysis was used for phase identification. Auger electron spectroscopy (AES) was used to observe WN_x formation following the N_2 plasma treatment. Scanning electron microscopy (SEM) was used to observe surface morphology as well as cross-sectional microstructure, and secondary ion mass spectroscopy (SIMS) was used for elemental depth profile measurement.

III. RESULTS AND DISCUSSION

A. Selective CVD-W and N_2 plasma treatment

Figure 2 shows overfilled 0.5 μm contact holes resulting from using a selective CVD-W technique. Excellent selectivity, good uniformity, and low resistivity W (about 10 $\mu\Omega$ cm) were obtained with a WF_6/SiH_4 flow rate of 40/10 sccm. Thus, this WF_6/SiH_4 flow rate was used to de-

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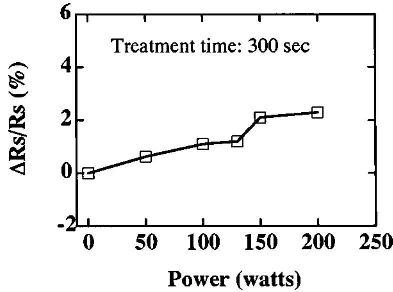

FIG. 3. Percentage change of sheet resistance vs N_2 plasma power in W(450 nm)/Si samples.

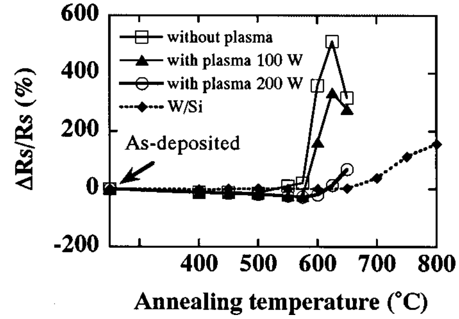

FIG. 5. Percentage change in sheet resistance plotted against annealing temperature for the W/Si sample as well as the Al/W/Si samples with and without N_2 plasma treatment on the W surface.

posit tungsten during barrier study in this work. Details of the CVD-W selectivity study were reported elsewhere[17] and are not discussed further in this article.

Post-deposition N_2 plasma treatment resulted in a sheet resistance change in the W/Si samples. Figure 3 shows the percentage change of sheet resistance versus N_2 plasma power for a W(450 nm)/Si sample. The sheet resistance increased slightly with increasing plasma power, presumably due to formation of thin WN_x layers on W surfaces, and the thicknesses of WN_x layers increased with N_2 plasma power. The measured AES depth profiles, as shown in Fig. 4, provide evidence for these presumptions. With N_2 plasma treatment at 100 W, a thin WN_x layer about 2 nm thick was formed on the W surfaces [Fig. 4(b)], while WN_x layer thicknesses were about 5 nm in the samples treated with N_2 plasma at 200 W [Fig. 4(c)]. Since metal nitride generally has a higher resistivity than corresponding pure metal, the presence of a thin WN_x layer on the W surface obviously resulted in a slight increase in sheet resistance in the W/Si samples.

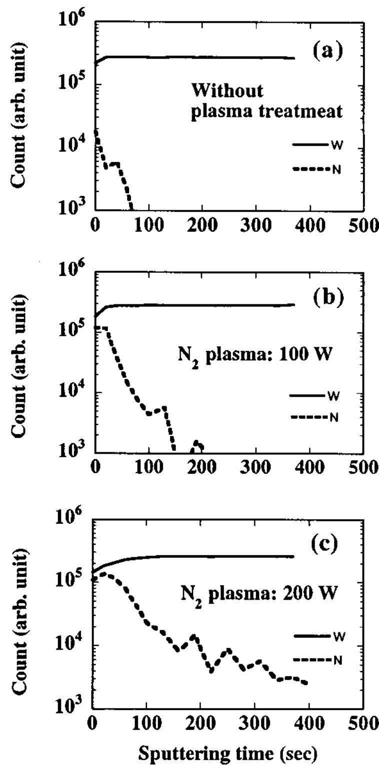

FIG. 4. AES depth profiles of W/Si samples (a) as-deposited, (b) after N_2 plasma treatment at 100 W, and (c) after N_2 plasma treatment at 200 W. The sputtering rate was about 0.1 nm/s.

B. Sheet resistance measurement and XRD analysis

Sheet resistance measurement and XRD analysis were used to evaluate the barrier capability of the W films. Figure 5 shows the percentage change in sheet resistance plotted against annealing temperature for the W/Si, Al/W/Si, and Al/WN_x/W/Si samples. The Al/W/Si samples whose W barriers did not receive N_2 plasma treatment showed increases in sheet resistance after annealing at 550 °C. With N_2 plasma treatment on the W surface, sheet resistance for the Al/WN_x/W/Si samples remained constant up to at least 575 °C. Although the WN_x layer was very thin, it showed an excellent barrier ability to suppress the reaction between Al and W, resulting in improved thermal stability for the Al/WN_x/W/Si structure.

The increase in sheet resistance for the Al/W/Si structure reflects the consumption of conductive aluminum due to WAl_{12} formation, as confirmed by the x-ray diffraction pattern shown in Fig. 6. The WAl_{12} compound appeared for the Al/W/Si sample annealed at 550 °C [Fig. 6(b)]. After annealing at 600 °C, phase signal intensity of the WAl_{12} increased and a part of it was converted into WAl_5 phase,[18] W_5Si_3 and WSi_2 signals both appeared as well [Fig. 6(c)]. Moreover, the Al signal disappeared while the α-W signal remained, implying that the 500 nm Al layer had been completely converted into WAl_{12} and WAl_5 but the 450 nm W layer was only partially consumed. The presence of W_5Si_3 and WSi_2 signals indicates that reactions took place at the W/Si interface during the 600 °C annealing.

The results of XRD analysis of Al/WN_x/W/Si samples treated with N_2 plasma at 200 W are illustrated in Fig. 7. No compound phase of W–Al or W–Si was observed after samples were annealed at temperatures up to 600 °C [Fig. 7(b)], which confirms the integrity of the multilayer structure. Apparently, N_2 plasma treatment has the effect of increasing the thermal stability of the Al/barrier/Si structure. After annealing at 650 °C, $W(Si, Al)_2$ and WSi_2 signals ap-

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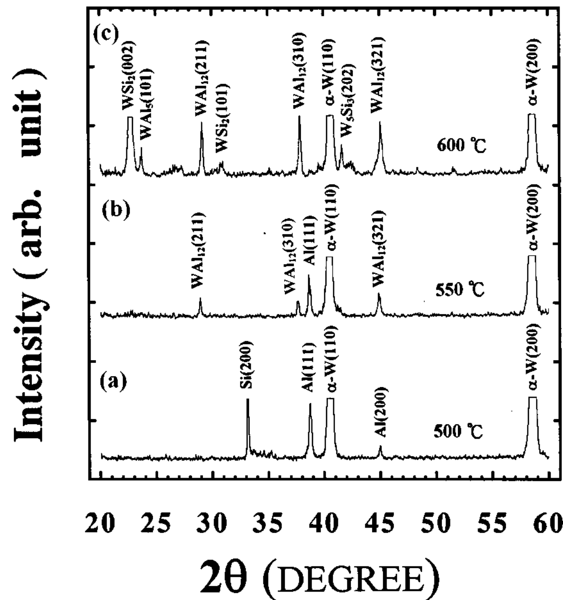

FIG. 6. XRD spectra for the Al/W(450 nm)/Si sample after annealing at (a) 500, (b) 550, and (c) 600 °C.

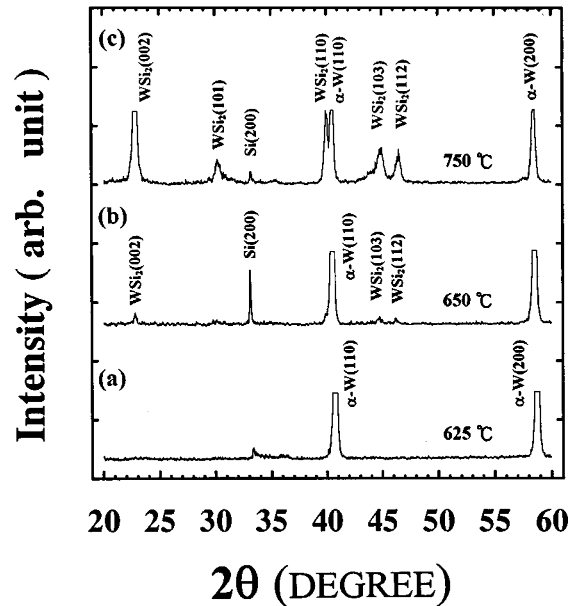

FIG. 8. XRD spectra for the W/Si sample after annealing at (a) 625, (b) 650, and (c) 750 °C.

peared and the Al signal remained, while no WAl_{12}-related signals were observed [Fig. 7(c)]. The W/Si samples without Al overlayers were also investigated for comparison. The increase in sheet resistance for the W/Si structure after annealing at temperatures above 700 °C (Fig. 5) presumably resulted from the consumption of conductive tungsten due to the formation of WSi_2, as confirmed by the XRD analysis results shown in Fig. 8. In fact, the XRD spectra show that weak WSi_2-phase signals began appearing at 650 °C, indicating reaction between W and the Si substrate. The WSi_2-signal intensity increased with increasing annealing temperature, but the α-W signal remained even after annealing at 750 °C. This indicates that the 450 nm W layer was only partially consumed after annealing at 750 °C. By comparing the XRD spectra of W/Si samples (Fig. 8) with those of Al/W/Si and $Al/WN_x/W/Si$ samples (Figs. 6 and 7), we found that the formation of WAl_{12} or $W(Si, Al)_2$ promoted the formation of WSi_2 for the Al/W/Si structure. Similar results have been reported in which the presence of an Al overlayer in the Al/W/Si structure led to a reduction in thermal stability of the underlying W/Si interface.[5] Comparative thermal stability results for the various layered structures are given in Table I.

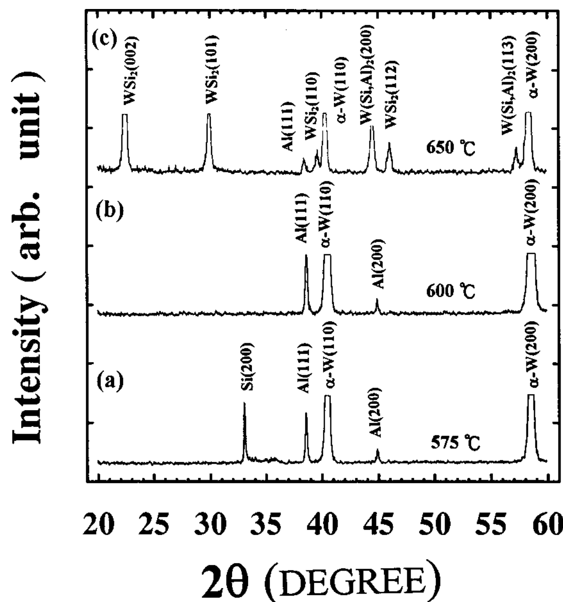

FIG. 7. XRD spectra for the $Al/WN_x/W(450\ nm)/Si$ sample after annealing at (a) 575, (b) 600, and (c) 650 °C. The W surface was treated with N_2 plasma at 200 W.

C. Electrical measurements

Barrier capability of the self-aligned selective CVD-W layers was investigated by evaluating the thermal stability of the $Al/W/p^+$-n junction diodes using electrical measurements. Figure 9 illustrates the distributions of reverse bias leakage current density measured at -5 V for the Al/p^+-n, $Al/W(100\ nm)/p^+$-n, and $Al/W(450\ nm)/p^+$-n junction diodes annealed at various temperatures; the diodes had a diffusion area of 500×500 or $1000\times1000\ \mu m^2$, and at least 30 diodes were measured in each case. Electrical characteristics of the Al/p^+-n diodes deteriorated after annealing at 400 °C [Fig. 9(a)], while the $Al/W(100\ nm)/p^+$-n diodes remained stable up to 500 °C [Fig. 9(b)]. Moreover, the $Al/W(450\ nm)/p^+$-n diodes were able to retain their integrity up to 575 °C [Fig. 9(c)]. It is clear that the thermal stability of the $Al/W/p^+$-n diodes can be improved further by using a thicker W film. Reaction of Al and W at elevated temperatures leads to the formation of WAl_{12}, and the barrier capability of a thin W film will be determined by the W consumption. For the $Al/W(450\ nm)/p^+$-n diodes, partial consumption of the thicker W layer due to the WAl_{12} forma-

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TABLE I. Comparative results of thermal stability for various layered structures.

Annealing temperature	W/Si	Al/W/Si	$Al/WN_x/W/Si$ (N_2 plasma 100 W)	$Al/WN_x/W/Si$ (N_2 plasma 200 W)
500 °C	X^a	X	X	X
550 °C	X	WAl_{12}	X	X
575 °C	X	WAl_{12}, WAl_5	X	X
600 °C	X	WAl_{12}, WAl_5, $W(Al,Si)_2$, WSi_2, W_5Si_3	WSi_2, $W(Al,Si)_2$	X
650 °C	WSi_2	WAl_5, $W(Al,Si)_2$, WSi_2	WSi_2, $W(Al,Si)_2$	WSi_2, $W(Al,Si)_2$

[a] "X" indicates no observation of compound phase.

tion did not deteriorate the integrity of W/Si interface; thus the diodes were stable even after annealing at 575 °C.

For comparison, junction diodes with W(450 nm)/ p^+-n structures, but without Al overlayers were also fabricated for thermal stability study. Figure 10 shows that the W(450 nm)/p^+-n diodes retained their integrity up to 700 °C and showed only slight degradation after annealing at 750 °C. This implies that degradation of the Al/ W(450 nm)/p^+-n diodes can be attributed to the presence of the Al overlayer.

The barrier capability of CVD-W layer can be effectively improved by *in situ* N_2 plasma treatment prior to Al metallization. Figure 11 shows the statistical distributions of reverse bias leakage current density for the variously annealed Al/WN_x/W(450 nm)/p^+-n junction diodes, in which the WN_x layer on the W surface was formed by N_2 plasma treatment. About half of the diodes whose W barriers were treated with N_2 plasma at 50 W survived thermal annealing at 600 °C, retaining a leakage current density of less than 100 nA/cm^2, as shown in Fig. 11(a); by contrast, none of the Al/W(450 nm)/p^+-n diodes survived the same thermal annealing at 600 °C [Fig. 9(c)]. Because the thickness of the WN_x layer increased with increasing N_2 plasma power (Fig. 4), further improvement of barrier capability can be obtained by increasing the N_2 plasma power. With N_2 plasma treatment at 100 W, the Al/WN_x/W(450 nm)/p^+-n diodes were able to retain their integrity up to 625 °C, as shown in Fig. 11(b). Increasing the N_2 plasma power to 200 W did not improve the thermal stability of the Al/WN_x/W(450 nm)/ Al/WN_x/W(450 nm)/p^+-n diodes, as shown in Fig. 11(c). Thermal stability temperatures for Al/WN_x/W(450 nm)/ p^+-n diodes as high as 650 °C were not achieved in this study, presumably because of closeness to the Al melting point of 660 °C, and the formation of WSi_2 at the W/Si interface (Fig. 7). Based on these experimental results, we conclude that selective CVD-W layers with post-deposition *in situ* N_2 plasma treatment form effective diffusion barrier between Al and Si substrate.

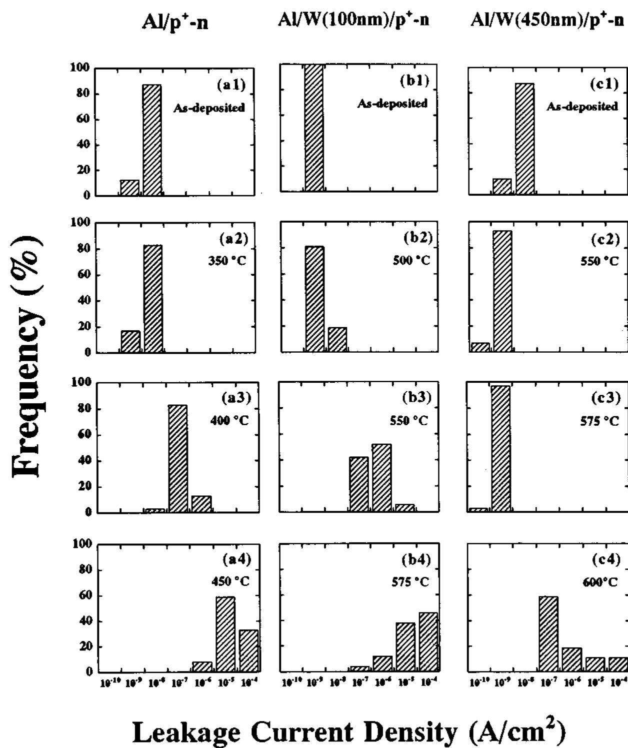

FIG. 9. Histograms showing the distributions of reverse bias leakage current density measured at -5 V for (a) Alp^+-n, (b) Al/W(100 nm)/p^+-n, and (c) Al/W(450 nm)/p^+-n junction diodes annealed at various temperatures.

D. SEM observation

Scanning electron microscopy (SEM) was used to investigate the surface and cross-sectional morphologies of the Al/barrier/p^+-n junction diodes. Figure 12 shows SEM micrographs of the Al/W(450 nm)/p^+-n junction diodes before and after thermal annealing. The as-deposited samples have rough Al surfaces because of the rough surfaces of the CVD-W underlayers [Fig. 12(a)]. Both the surface morphology and the W/Si interface remained unchanged after annealing at 500 °C [Fig. 12(b)]. After annealing at 600 °C, precipitates were found at the W/Si interface and protrusions

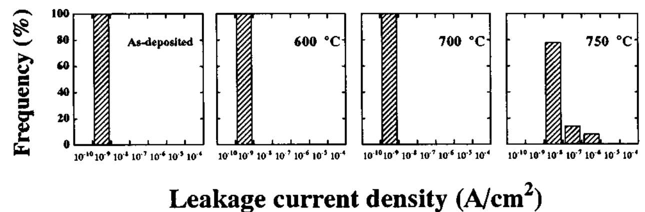

FIG. 10. Histograms showing the distributions of reverse bias leakage current density measured at -5 V for the W(450 nm)/p^+-n junction diodes annealed at various temperatures.

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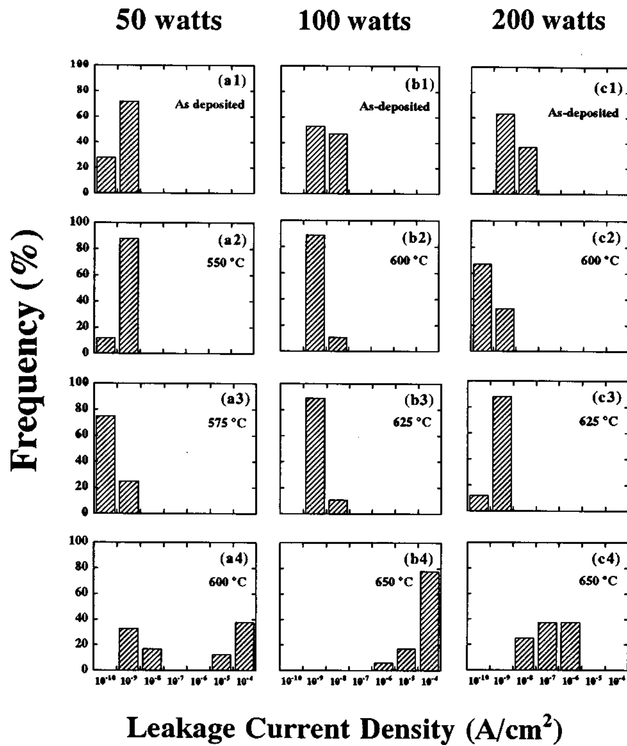

FIG. 11. Histograms showing the distributions of reverse bias leakage current density measured at -5 V for the Al/WN_x/W(450 nm)/p^+-n junction diodes annealed at various temperatures; the W layers of the junction diodes were treated with N_2 plasma at (a) 50, (b) 100, and (c) 200 W.

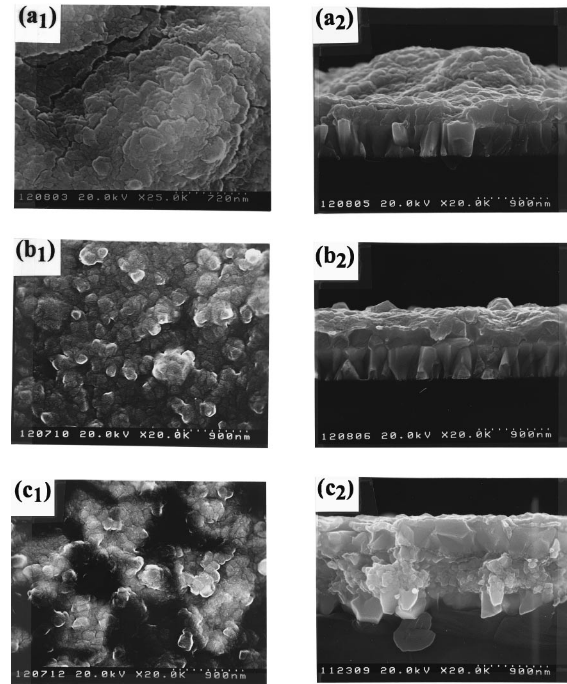

FIG. 13. Top-view (left) and cross-sectional view (right) SEM micrographs for (a) 600 °C annealed Al/WN_x/W(450 nm)/p^+-n diodes whose W barrier was treated with N_2 plasma at 50 W, (b) 600 °C annealed Al/WN_x/W(450 nm)/p^+-n diodes whose W barrier was treated with N_2 plasma at 100 W, and (c) 650 °C annealed Al/WN_x/W(450 nm)/p^+-n diodes whose W barrier was treated with N_2 plasma at 100 W.

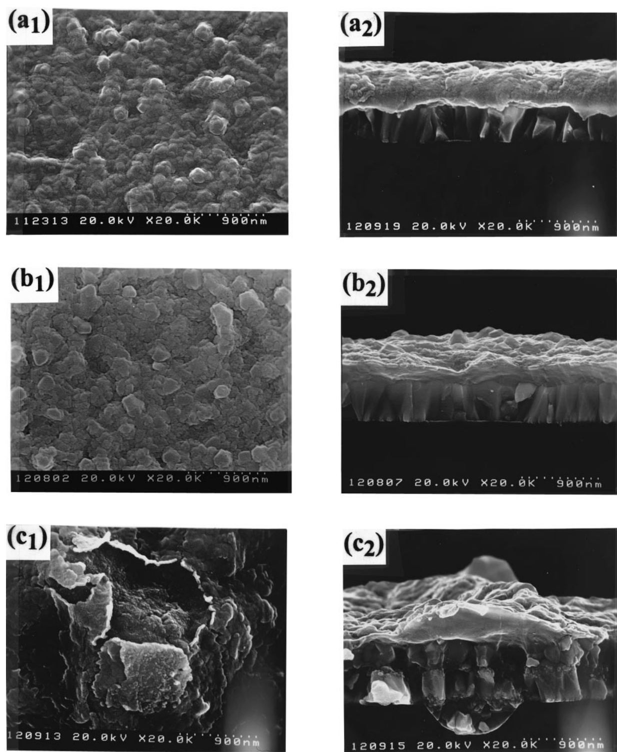

FIG. 12. Top-view (left) and cross-sectional view (right) SEM micrographs for the Al/W(450 nm)/p^+-n junction diodes (a) as-deposited, (b) annealed at 500 °C, and (c) annealed at 600 °C.

were observed on the surface, presumably due to WAl_{12} formation [Fig. 12(c)]. Assuming total conversion of the 500-nm-thick Al film into the WAl_{12}, only about 40 nm of W-layer thickness was consumed and the remaining 410 nm should be able to function as a barrier layer. However, nonuniform formation of WAl_{12} might lead to a highly localized thinning of the W layer; thus, either Al atoms or WAl_{12} compound can be very close to the W/Si interface. As a result, close proximity of Al atoms to the Si substrate can easily induce reaction between Al and Si during thermal annealing at 600 °C. Moreover, it is possible that the formation of WSi_2 and WAl_{12} introduces microcracks that cannot be observed by SEM but might provide fast diffusion paths for Al atoms to react with the Si substrate.

Figure 13 shows top-view and cross-sectional SEM micrographs of the thermally annealed Al/WN_x/W(450 nm)/p^+-n junction diodes. Instead of protrusions on the surface and large precipitates at the W/Si interfaces for the 600 °C annealed Al/W(450 nm)/p^+-n samples [Fig. 12(c)], surface cracks and small precipitates at the W/Si interface were found on the 50 W plasma-treated Al/WN_x/W(450 nm)/p^+-n diodes after annealing at 600 °C, as shown in Fig. 13(a). Figure 13(b) shows the 600 °C annealed Al/WN_x/W(450 nm)/p^+-n samples whose barriers were treated with N_2 plasma at 100 W; compared with the as-deposited Al/W(450 nm)/p^+-n shown in Fig. 12(a), no obvious difference is observable with respect to surface morphology and W/Si interface smoothness. The thin WN_x layer that formed

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TABLE II. Comparative thermal stability results for p^+-n junction diodes with different W-barrier layers as determined using various characterization techniques.

Barrier/metallization structures of p^+-n junction diodes	Leakage current	SEM	SIMS
Al/W(100 nm)/p^+-n	500 °C	500 °C	
Al/W(450 nm)/p^+-n	575 °C	575 °C	<600 °C
Al/WN_x/W(450 nm)/p^+-n (N_2 plasma at 100 W)	625 °C	625 °C	>600 °C
Al/WN_x/W(450 nm)/p^+-n (N_2 plasma at 200 W)	625 °C	625 °C	>600 °C
W(450 nm)/p^+-n	700 °C	WSi_2 formed at 700 °C	

on the W surface due to the N_2 plasma treatment, was able to suppress the WAl_{12} compound formation and kept the W/Si interface unchanged up to 600 °C. After annealing at 650 °C, all of the diodes failed, presumably due to the low melting point of Al (660 °C). Compound [WAl_{12}, and WAl_5, and $W(Si, Al)_2$] formation along with tungsten silicidation deteriorated the Al/WN_x/W(450 nm)/p^+-n diodes completely, as shown in Fig. 13(c). Comparative thermal stability results for the p^+-n junction diodes with different W-barrier layers determined using various characterization techniques are given in Table II.

E. SIMS analysis

SIMS depth profiles were used to examine elemental distributions in the multilayer structures. Figure 14 shows the SIMS depth profiles for the Al/W(450 nm)/Si and Al/WN_x/W(450 nm)/Si samples before and after thermal annealing at 600 °C. Without N_2 plasma treatment, the interdiffusion of Al, W, and Si led to severe deterioration of the Al/W (450 nm)/Si structure after 600 °C annealing, as shown in Fig. 14(b). The Al/WN_x/W(450 nm)/Si samples whose W barriers were treated with N_2 plasma at 200 W, had W and Si profiles that remained almost unchanged, while Al diffused only slightly into W layers, as shown in Fig. 14(d). This indicates that the thermal stability of the Al/W barrier/p^+-n diodes can be significantly improved using N_2 plasma treatment on the W surfaces.

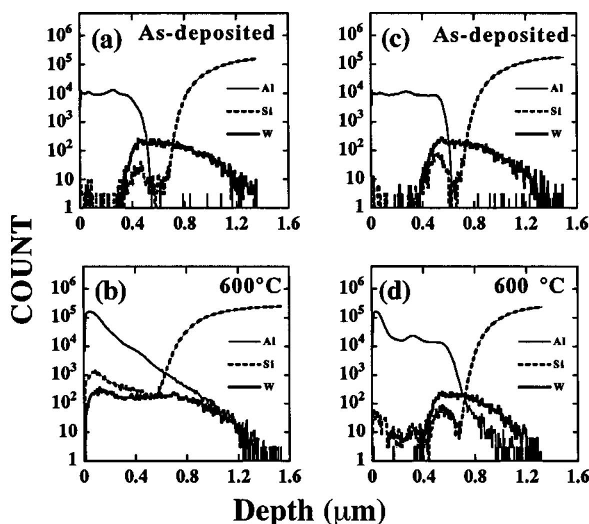

FIG. 14. SIMS depth profiles for Al/W(450 nm)/Si (a) as-deposited and (b) 600 °C annealed, and for Al/WN_x/W(450 nm)/Si (c) as-deposited and (d) 600 °C annealed.

IV. SUMMARY

The effect of *in situ* N_2 plasma treatment on the thermal stability of selective CVD-W contacted p^+-n junction diodes with Al metallization was systematically investigated. Without N_2 plasma treatment, the Al/W(100 nm)/p^+-n and Al/W(450 nm)/p^+-n junction diodes were able to sustain a 30 min furnace annealing up to 500 and 575 °C, respectively. With *in situ* N_2 plasma treatment on W surfaces at a power of 100 W, the Al/WN_x/W(450 nm)/p^+-n junction diodes were able to sustain thermal annealing up to 625 °C without degradation of their electrical characteristics. Reaction between Al and CVD-W at elevated temperatures resulted in formation of WAl_{12}, WAl_5, and $W(Si, Al)_2$, leading to acceleration of the reaction between W and Si substrates. The N_2 plasma treatment resulted in formation of a thin WN_x layer on the W surface, and the Al/WN_x/W/Si structure effectively suppressed W–Al compound formation, leading to improvement of thermal stability.

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