Barrier Properties of Very Thin Ta and TaN Layers Against Copper Diffusion

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ABSTRACT

Diffusion barrier properties of very thin sputtered Ta and reactively sputtered TaN films used as a barrier layer between Cu and Si substrates were investigated using electrical measurement and materials analysis. The Cu/Ta/p^+-n junction diodes with the Ta barrier of 5, 10, and 25 nm thicknesses were able to sustain a 30 min thermal annealing at temperatures up to 450, 500, and 550°C, respectively, without causing degradation to the device's electrical characteristics. The barrier capability of Ta layer can be effectively improved by incorporation of nitrogen in the Ta film using reactive sputtering technique. For the Cu/TaN/p^+-n junction diodes with the TaN barrier of 5, 10, and 25 nm thicknesses, thermal stability was able to reach 500, 600, and 700°C, respectively. We found that failure of the very thin Ta and TaN barriers was not related to Ta silicidation at the barrier/Si interface. Failure of the barrier layer is presumably due to Cu diffusion through the barrier layer during the process of thermal annealing via local defects, such as grain boundaries and stress-induced weak points.

Introduction

Copper (Cu) has attracted much attention in deep submicron mutlilevel interconnection applications because of its low bulk resistivity (1.68 μΩ cm), excellent electromigration resistance,[1,2] and acceptability of deposition by electroless as well as chemical vapor deposition (CVD).[3-5] Unfortunately, Cu diffuses fast in silicon, silicide, as well as oxide, and forms Cu-Si compounds at temperatures as low as 200°C, resulting in degradation of device characteristics.[6,7] Moreover, it has poor adhesion to interlevel dielectric and drifts through oxide under field acceleration.[8-10] Therefore, a diffusion barrier between Cu and its underlying layers is considered as a prerequisite for Cu to be useful in silicon integrated circuit applications.

Various materials have been studied as a diffusion barrier between Cu and Si substrate, as well as Cu and dielectric layer. Refractory metals have been recognized as an attractive class of materials because of their high thermal stability and good electrical conductivity.[11-13] Sputtering of nitride-based diffusion barriers, such as WN,[14] TiN,[15] TiWN,[16,17] and TaN,[18-25] to be used in Cu/barrier/Si and Cu/barrier/SiO_2 structures, has attracted extensive attention. Tantalum (Ta) forms no compound with copper; thus, Cu/Ta/Si, structure is expected to be stable at high temperatures.[18,19] In addition, because Ta has a low formation enthalpy (ΔH) with nitrogen, and tantalum nitride (TaN) has a high melting point of 3087°C as well as a more dense microstructure, Cu/TaN/Si structure is also expected to be thermally stable at elevated temperatures.[26] In this work, we investigate Ta and TaN as a diffusion barrier in Cu metallization system.

It was reported that a Ta film of 50 nm thickness acting as a diffusion barrier between a Cu and Si structure retained the integrity of the Cu/Ta/Si structure at temperatures up to 600°C for 30 min.[19] It was also reported that a TaN film of 100 nm thickness was able to act as an effective diffusion barrier between Cu and Si substrate at 750°C for 60 min.[23] Moreover, it was found that an Ar^+ ion bombardment during deposition of Ta resulted in a dense Ta film with low resistivity, and thus the barrier effectiveness of Ta film was significantly enhanced.[27] Although these studies have provided much valuable information for the application of Ta film as a diffusion barrier, nevertheless, little study has been made on the evaluation of barrier effectiveness with respect to the devices' electrical characteristics, which is believed to be more sensitive to barrier degradation than the material property.[14] Moreover, though a number of data are already published on the thermal stability of Ta and TaN films thicker than 30 nm using the characterization techniques of material analysis, no comparative study has been made on the thermal stability of ultrathin (less than 30 nm) Ta and TaN films using the electrical measurements as well as material analyses. As the device dimensions move to 0.25 μm and below, it becomes inappropriate to use a barrier thicker than 30 nm. The barrier thickness should be reduced to lower the resistance of the total line interconnect and/or via.

In this study, we investigated the thermal stability of ultrathin Ta and TaN barrier layers in a Cu metallization system. Properties of these barrier layers were evaluated by electrical measurement as well as material analyses. The results of this study might be useful for Cu metallization in ultralarge-scale integrated (ULSI) multilevel interconnects applications.

Experimental

The Cu/Ta/p^+-n and Cu/TaN/p^+-n junction diodes were fabricated for the study of Ta and TaN barrier capability. The starting materials were 4-in., (100)-oriented, n-type silicon wafers with 4-7 Ω cm nominal resistivity. After RCA standard cleaning, the wafers were thermally oxidized at 1050°C in steam atmosphere to grow a 500 nm oxide layer. Diffusion regions with areas 500 × 500 and 1000 × 1000 μm^2 were defined on the oxide-covered wafers using the conventional photolithographic technique. The p^+-n junctions with junction depths of 0.3 μm were formed by BF_2^+ implantation at 40 keV to a dose of 3×10^{15} cm^{-2} followed by furnace annealing at 900°C for 30 min in N_2 ambient.

After the junctions were formed, the wafers were prepared for Ta or TaN barrier layer deposition. In this study, a dc magnetron sputtering system with a base pressure of $1–2 \times 10^{-6}$ Torr and with no intentional substrate heating and bias was used. The Ta films were sputtered using a Ta target in Ar ambient at a pressure of 7.6 mTorr, while the TaN films were reactively sputtered using the same Ta target in an Ar/N_2 gas mixture at the same pressure of 7.6 mTorr. The flow rates of Ar and N_2 into the sputtering chamber were 24 and 6 sccm, respectively, for making the Ar/N_2 gas mixture.[28] Prior to each sputter deposition, the target was cleaned by presputtering with the shutter closed for 10 min. The Ta and TaN films were deposited at a sputtering power of 200 W to a thickness of 25, 10, and 5 nm separately. The deposition rates of Ta and TaN films were determined to be 2.94 and 2.07 nm/min, respectively. After the barrier layer deposition, Cu films of 200 nm thickness were deposited on the barrier metal using the same sputtering system without breaking the vacuum. Finally, Cu patterns were defined and etched using dilute (5 vol %) HNO_3, while Ta and Ta nitrides were etched using SF_6/N_2 plasma for the preparation of Cu/Ta/p^+-n and Cu/TaN/p^+-n diodes. For comparison, the thermal stability of Cu/p^+-n diodes without a barrier layer as well as Ta/p^+-n and TaN/p^+-n diodes without a Cu overlayer was also investi-

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gated. The schematic cross sections of these differently metallized p^+-n junction diodes are illustrated in Fig. 1.

To investigate thermal stability of the Cu/Ta/p^+-n and Cu/TaN/p^+-n diodes, the diodes were thermally annealed at various temperatures ranging from 200 to 800°C for 30 min in N_2 ambient. Leakage current was measured at a reverse bias of −5 V using an HP-4145B semiconductor parameter analyzer; the measured diodes have an active area of 500 × 500 or 1000 × 1000 μm, and at least 30 diodes were measured in each case. For material analysis, unpatterned samples of barrier/Si, Cu/barrier/Si, and Cu/barrier/SiO_2/Si structures were also prepared. These samples were processed in the same process run with the patterned samples of junction diodes except a number of thicker Ta and TaN samples of Ta/Si and TaN/Si specialized for X-ray diffraction (XRD) analysis. Sheet resistance of the multilayer structures was measured using a four-point probe. XRD analysis using a 30 keV copper Kα radiation was used for phase identification. Scanning electron microscopy (SEM) was employed to observe surface morphology and microstructure.

Results and Discussion

Electrical measurements.—Barrier capability of thin Ta and TaN films was investigated by evaluating the thermal stability of Cu/Ta/p^+-n and Cu/TaN/p^+-n junction diodes using electrical measurements. We analyzed the distributions of leakage current density for the annealed diodes and related the results of electrical measurements to other results obtained by sheet resistance measurement, XRD analysis, and SEM observation.

Cu/Ta/p^+-n junction diodes.—Figure 2 illustrates the statistical distributions of reverse bias leakage current density measured at −5 V for the Cu/Ta(25 nm)/p^+-n, Cu/Ta (10 nm)p^+-n, and Cu/Ta(5 nm)/p^+-n junction diodes annealed at various temperatures. The Cu/Ta(25 nm)/p^+-n diodes remained stable after annealing at temperatures up to 550°C but suffered moderate degradation in electrical characteristic at 600°C; annealing at 650°C resulted in severe degradation (Fig. 2a). For the Cu/Ta(10 nm)/p^+-n diodes, the diodes remained stable after annealing at temperatures up to 500°C, while a number of diodes suffered moderate degradation after annealing at 550°C; however, about 50% of the diodes survived even after annealing at 600°C (Fig. 2b). As for the Cu/Ta(5 nm)/p^+-n diodes, they started to show degradation after annealing at 500°C (Fig. 2c). This indicates that thermal stability of the Cu/Ta/p^+-n junction diodes may be severely degraded by reducing the Ta barrier layer thickness below 5 nm.

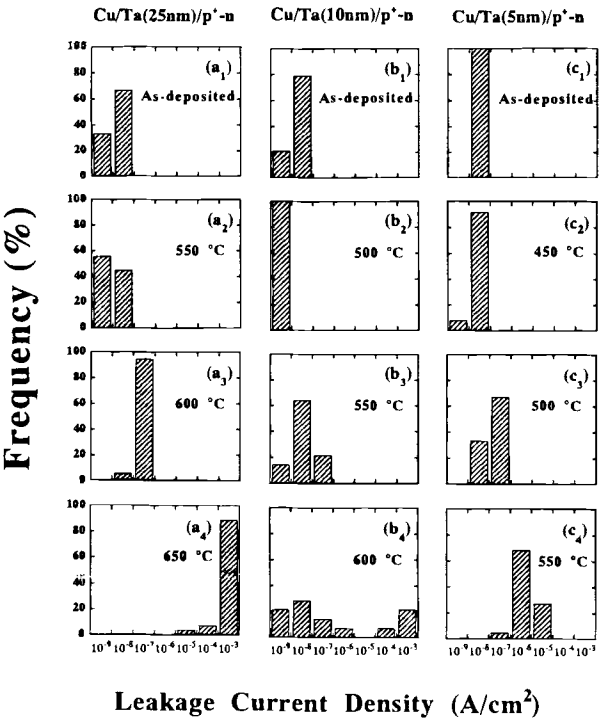


Fig. 2. Histograms showing the distributions of reverse bias leakage current density for (a) Cu/Ta(25 nm)/p^+-n, (b) Cu/Ta (10 nm)/p^+-n, and (c) Cu/Ta(5 nm)/p^+-n junction diodes annealed at various temperatures.

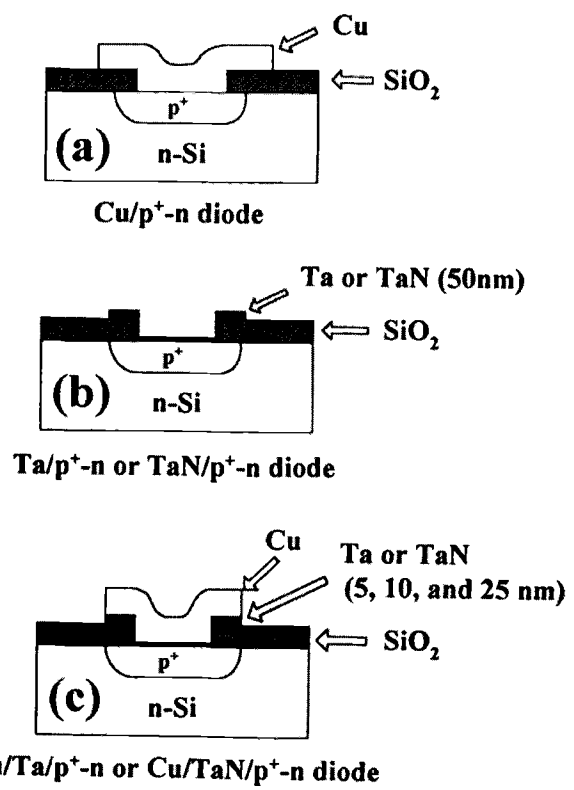


Fig. 1. Schematic cross sections of (a) Cu/p^+-n, (b) barrier/p^+-n, and (c) Cu/barrier/p^+-n junction diodes.

Cu/TaN/p^+-n junction diodes.—The barrier properties of Ta can be significantly improved by adding impurities, such as N and O, to the Ta film.[18,19] If solubility limit of the impurity is exceeded, solute atoms in the Ta grain are expected to be segregated to the grain boundaries, resulting in obstruction of the fast paths for copper diffusion. It was reported that the grain size and atomic density of reactively sputtering deposited Ta-N films, respectively, decreased and increased as the nitrogen concentration in the Ta–N films was increased; moreover, the bcc-Ta, Ta_2N, TaN, and Ta_5N_6 phase appeared in succession with the increase of the nitrogen content.[18] In addition, TaN is chemically inert to Si and Cu, and it has been reported that the contact system of Cu/TaN/Si is thermally very stable.[23] The superiority of TaN films in thermal stability over the pure Ta film was also reported.[20]

Figure 3 shows the statistical distributions of reverse bias leakage current density for the Cu/TaN/p^+-n junction diodes of different TaN barrier thickness annealed at various temperatures. For the diodes with a 25 nm thick TaN barrier, the devices remained stable after annealing at temperatures up to 700°C. After annealing at 750°C, though many devices failed, more than half of the tested diodes still survived (Fig. 3a). This feature of failure is probably related to the Cu diffusion through localized defects in the annealed TaN layer. For the diodes with a 10 nm thick TaN barrier, the devices suffered moderate degradation after annealing at 650°C and degraded severely after annealing at 700°C (Fig. 3b). For the Cu/TaN(5 nm)/p^+-n diodes, the 5 nm TaN film was proved to be an effective barrier against Cu diffusion at temperatures up to 500°C. As the annealing temperature was raised to 550°C, the diodes started to show degradation (Fig. 3c). Comparative results

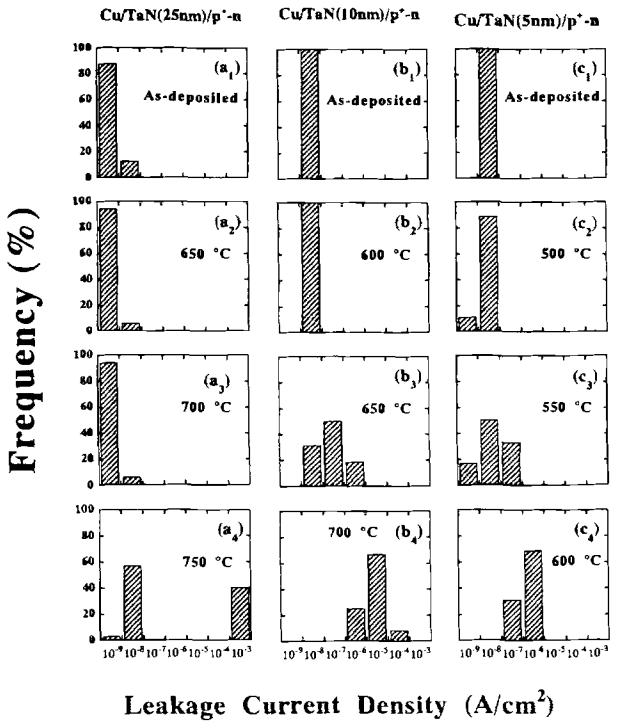


Fig. 3. Histograms showing the distributions of reverse bias leakage current density for (a) Cu/TaN(25 nm)/p⁺-n, (b) Cu/TaN (10 nm)/p⁺-n, and (c) Cu/TaN(5 nm)/p⁺-n junction diodes annealed at various temperatures.

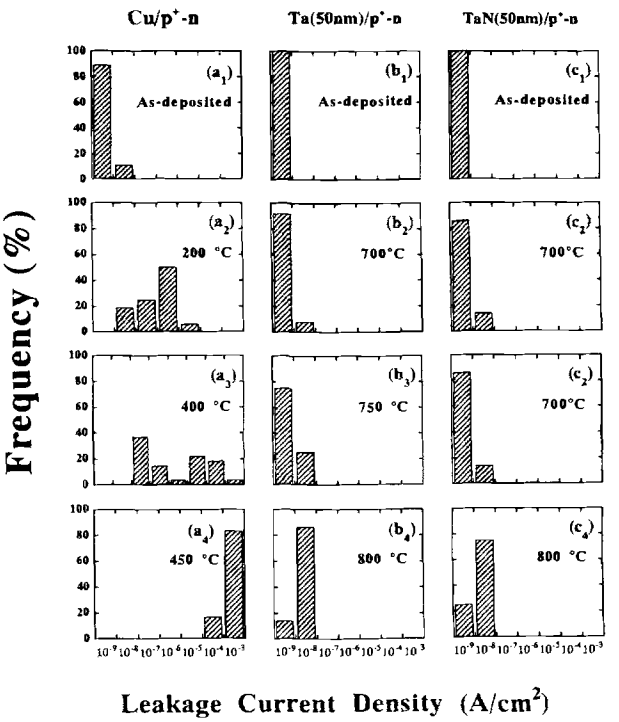


Fig. 4. Histograms showing the distributions of reverse bias leakage current density for (a) Cu/p⁺-n, (b) Ta(50 nm)/p⁺-n, and (c) TaN(50 nm)/p⁺-n junction diodes annealed at various temperatures.

of barrier effectiveness for Ta and TaN films of different thickness are summarized in Table I. The results show that the barrier capability of a Ta layer can be substantially improved by incorporation of nitrogen using reactive nitridation technique. Moreover, thermal stability of the Cu/Ta/p⁺-n and Cu/TaN/p⁺-n diodes was found to be dependent on the thickness of the barrier, implying that Cu diffusion in the barrier layer is mainly controlled by film defects, such as grain boundaries, voids, and dislocations.

Cu/p⁺-n, Ta/p⁺-n, and TaN/p⁺-n junction diodes.—For comparison, the Cu/p⁺-n diodes without a barrier layer and the barrier/p⁺-n diodes without a Cu overlayer were also fabricated for thermal stability study. Figure 4 illustrates the distributions of reverse bias leakage current density for the Cu/p⁺-n, Ta/p⁺-n, and TaN/p⁺-n junction diodes annealed at various temperatures. The Cu/p⁺-n diodes suffered severe degradation after annealing at 200°C (Fig. 4a), while the Ta/p⁺-n and TaN/p⁺-n diodes were able to retain their integrity up to at least 800°C. Thus, the degradation of Cu/Ta/p⁺-n and Cu/TaN/p⁺-n diodes (Fig. 2 and 3) was attributed to the presence of Cu overlayer.

Material Analyses.—XRD analysis.—The crystallographic structure of sputter-deposited TaN_x depends on the concentration of nitrogen in the TaN_x film.[18,19] Figure 5 shows the XRD spectra for the Ta(300 nm)/Si sample annealed at various temperatures. Diffraction patterns taken from the as-deposited Ta layer was indexed to be β–Ta.[29] For the sample annealed at 650°C, the spectrum remained unchanged as compared with the as-deposited sample. However, a number of weak $TaSi_2$ [30] peaks appeared for the sample annealed at 700°C. After annealing at 800°C, signals representing the crystalline phase of $TaSi_2$ became much stronger, indicating significant grain growth. Since Ta silicidation was not observed at 600°C and the electrical characteristics of Cu/Ta/p⁺-n diodes failed at temperatures below 600°C (Fig. 2), we excluded the possibility of Ta silicidation to be one of the Ta-barrier failure mechanisms for the Cu/Ta/p⁺-n junction diodes. Noya et al. reported that Ta_5Si_3 or amorphous layer formation at the Ta/Si interface preceded the $TaSi_2$ growth.[31,32] However, our results of XRD analyses showed only $TaSi_2$ phase in the thermally annealed

Table I. Comparative results of barrier effectiveness for Ta and TaN films evaluated by electrical measurement on the Cu/barrier/p⁺-n junction diodes.

	Ta			TaN		
Barrier layer	25 nm	10 nm	5 nm	25 nm	10 nm	5 nm
Thermal stability temperature	550°C	500°C	450°C	700°C	600°C	500°C

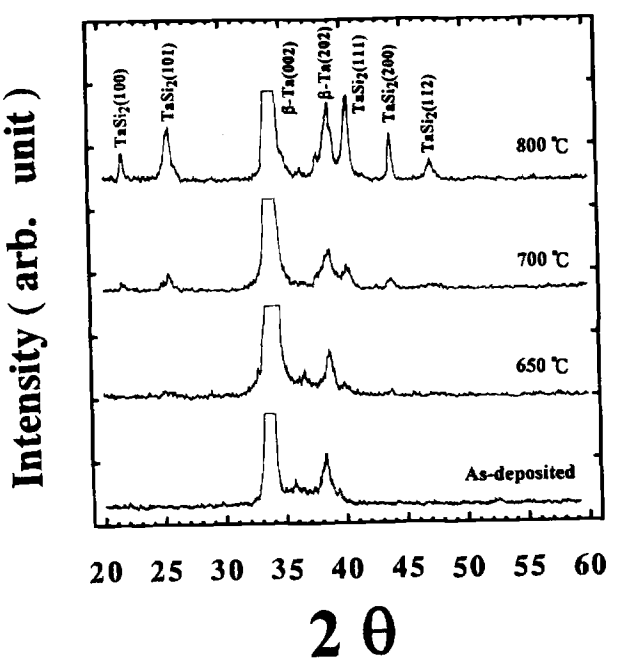


Fig. 5. XRD spectra for Ta(300 nm)/Si sample annealed at various temperatures.

Ta/Si system, similar to the results reported by Holloway et al.[20] This discrepancy might result from the difference in deposition temperature as well as thickness of Ta metal and annealing conditions between Noya's and ours.

Figure 6 shows XRD spectra for the TaN(300 nm)/Si sample. The diffraction patterns taken from the as-deposited TaN layer was indexed to be cubic TaN.[33] The spectrum remained unchanged even after the sample was annealed at 800°C, indicating structural integrity of the TaN(300 nm)/Si sample. By comparing the XRD spectra of the TaN/Si samples (Fig. 6) with those of the Ta/Si samples (Fig. 5), we found clearly that the contact system of TaN/Si is chemically more stable than that of Ta/Si.

Figure 7 shows XRD spectra for the Cu/Ta(25 nm)/Si and Cu/TaN(25 nm)/Si samples after annealing at various temperatures. For the Cu/Ta/Si sample annealed at 650°C, signal of Ta_5Si_3 phase[34] was detected; after annealing at 750°C, signal of Cu[35] disappeared while many peaks relating to Ta silicide and Cu silicide[36] appeared, indicating complete failure of the Ta-barrier film (Fig. 7a). Compared with the XRD spectra for the Ta/Si samples (Fig. 5), we found that the presence of Cu film on the surface of the Ta/Si structure accelerated the formation of Ta silicide.[20] Silicide signals did not appear for the Cu/TaN/Si sample thermally annealed at temperatures up to 750°C (Fig. 7b). Clearly, thermal stability of the Cu/TaN/Si structure is superior to that of the Cu/Ta/Si contact system. Furthermore, raising the annealing temperature to 800°C resulted in the appearance of Cu silicide signal, but the Ta silicide signal was not detected (Fig. 7b). These results imply that the failure of Cu/TaN/p$^+$-n diodes at 750°C or below (Fig. 3) was not related to Ta silicidation at the TaN/Si interface. Instead, Cu atoms diffused through the annealed TaN film via local defects (such as grain boundaries, voids, and stress-induced weak points) should be blamed.

Sheet resistance measurement.—The sheet resistance change of annealed samples, normalized to the as-deposited sheet resistance value, is denoted as $\Delta Rs/Rs\%$ and defined as follows

$$\frac{\Delta Rs}{Rs}\% = \frac{Rs_{\text{after anneal}} - Rs_{\text{as-deposited}}}{Rs_{\text{as-deposited}}} \times 100\%$$

Figure 8 shows the percentage change of sheet resistance vs. annealing temperature for the samples of Cu/Ta

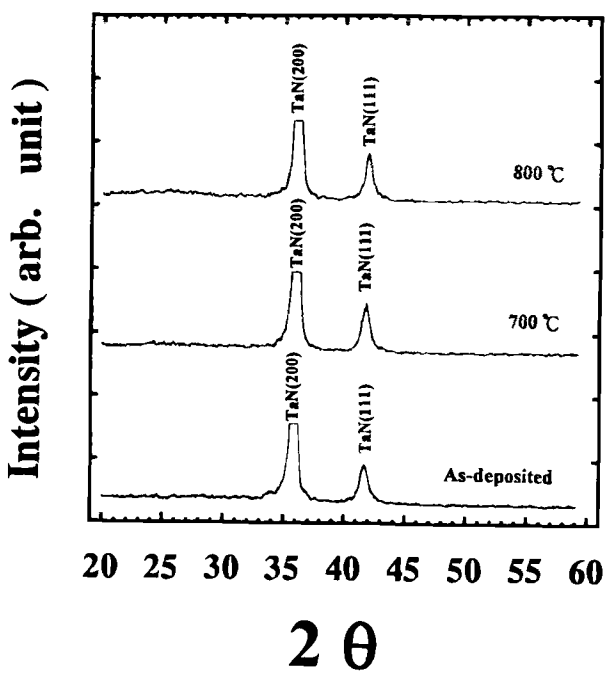
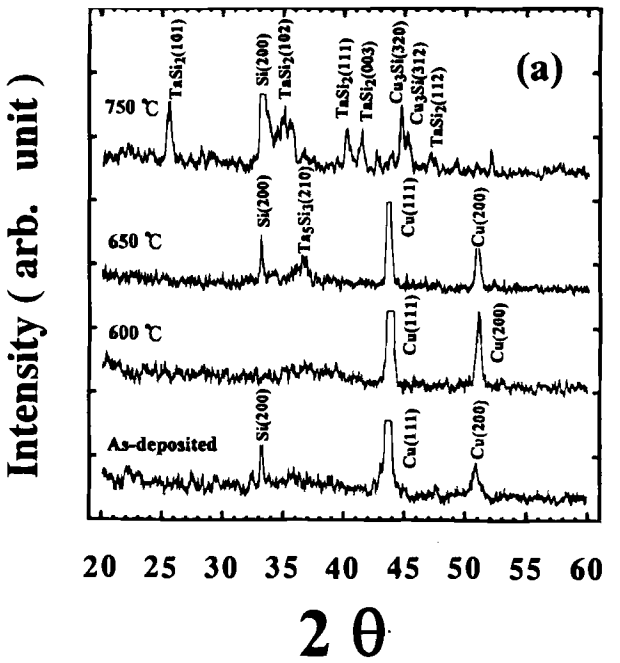


Fig. 6. XRD spectra for TaN(300 nm)/Si sample annealed at various temperatures.



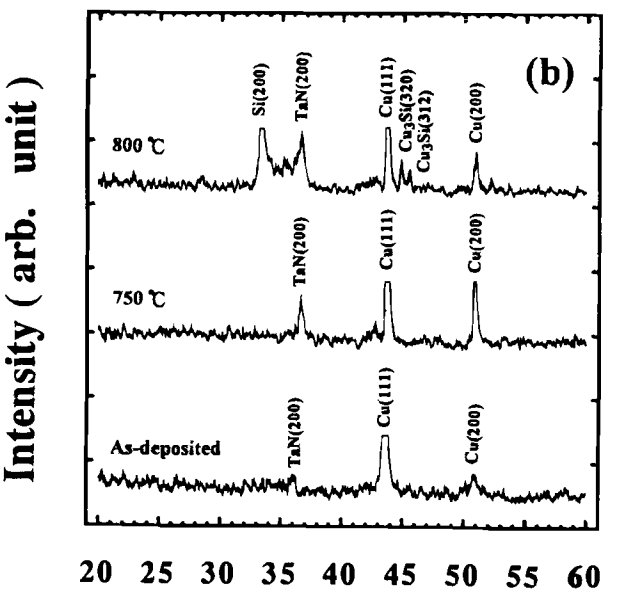


Fig. 7. XRD spectra for (a) Cu/Ta(25 nm)/Si and (b) Cu/TaN (25 nm)/Si samples annealed at various temperatures.

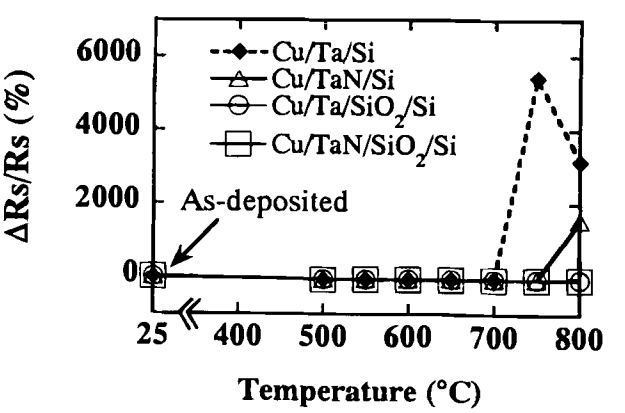


Fig. 8. Percentage change of sheet resistance vs. annealing temperature for the samples of Cu/Ta(25 nm)/Si, Cu/TaN(25 nm)/Si, Cu/Ta(25 nm)/SiO_2/Si, and Cu/TaN(25 nm)/SiO_2/Si.

Table II. Compound phases detected by XRD analysis for various multilayer structures studied in this work.[a]

Annealing temperature	Samples structure				
	Ta/Si	TaN/Si	Cu/Ta/Si	Cu/TaN/Si	Cu/Ta/SiO_2/Si
600°C	×	×	×	×	×
650°C	×	×	Ta_5Si_3	×	×
700°C	$TaSi_2$	×	Cu_3Si, Ta_5Si_3	×	×
750°C	$TaSi_2$	×	Cu_3Si, $TaSi_2$, Ta_5Si_3	×	×
800°C	$TaSi_2$	×	Cu_3Si, $TaSi_2$	Cu_3Si	×

[a] "×" indicates no observation of compound phase (except TaN).

(25 nm)/Si, Cu/TaN(25 nm)/Si, Cu/Ta(25 nm)/SiO_2/Si, and Cu/TaN(25 nm)/SiO_2/Si. For the Cu/Ta(25 nm)/Si sample, the sheet resistance remained constant after annealing at temperatures up to 700°C, but a dramatic increase occurred

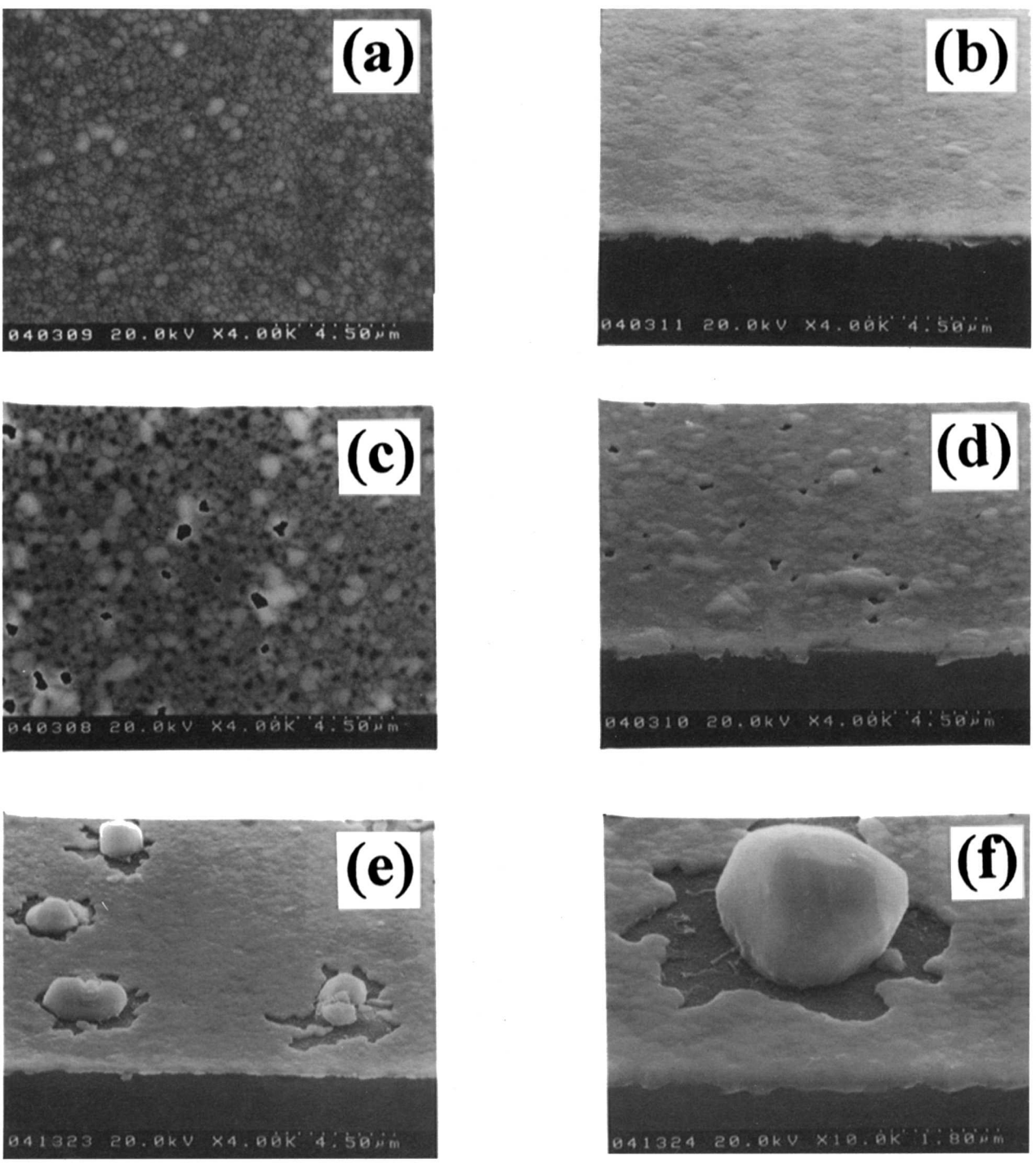


Fig. 9. Top view and oblique view SEM micrographs for the Cu/TaN(25 nm)/p^+-n diodes annealed at (a) and (b) 700°C, and (c), (d), (e), and (f) 750°C. The micrographs (c) and (d) were taken on a slightly degraded diode, and (e) and (f) were taken on a severely degraded diode.

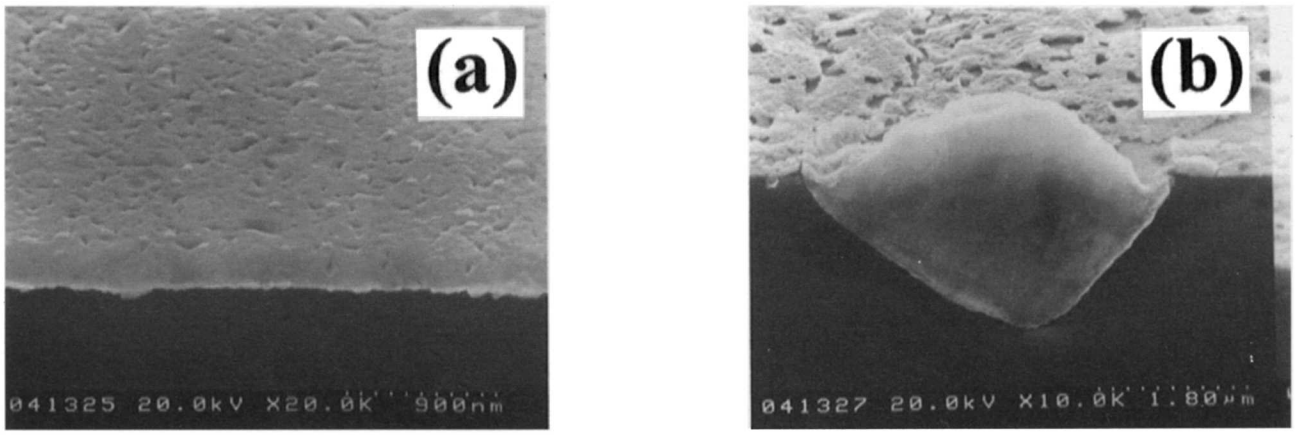


Fig. 10. SEM micrographs for the Cu/Ta(25 nm)/p^+-n diodes annealed at (a) 600 and (b) 650°C.

after annealing at 750°C. Sheet resistance for the Cu/TaN(25 nm)/Si sample remained unchanged after annealing at temperatures up to 750°C but made a significant increase after annealing at 800°C. The increase in sheet resistance for the Cu/Ta(25 nm)/Si and Cu/TaN(25 nm)/Si samples reflects the consumption of conductive Cu layer due to Cu_3Si formation, as confirmed by the XRD analysis shown in Fig. 7. Although sheet resistance of the Cu/Ta (25 nm)/Si sample remained unchanged after annealing at 700°C, the results of electrical measurement showed that the Cu/Ta(25 nm)/p^+-n junction diodes suffered severe degradation after the devices were annealed at 650°C. This indicates that electrical measurement is a much more sensitive technique for barrier failure detection.

For the samples with a 500 nm oxide layer between the barrier metal and Si substrate, sheet resistance of the Cu/Ta(25 nm)/SiO_2/Si and Cu/TaN(25 nm)/SiO_2/Si samples remained constant up to at least 800°C. Moreover, no signal relating to Ta–Si or Cu–Si compound was detected by XRD analysis. The different results between the Cu/barrier/SiO_2/Si and Cu/barrier/Si samples imply that the Si substrate in the Cu/barrier/Si contact system acted as a Cu-sink, which plays an important role in determining the thermal stability of the Cu/barrier/Si structure.

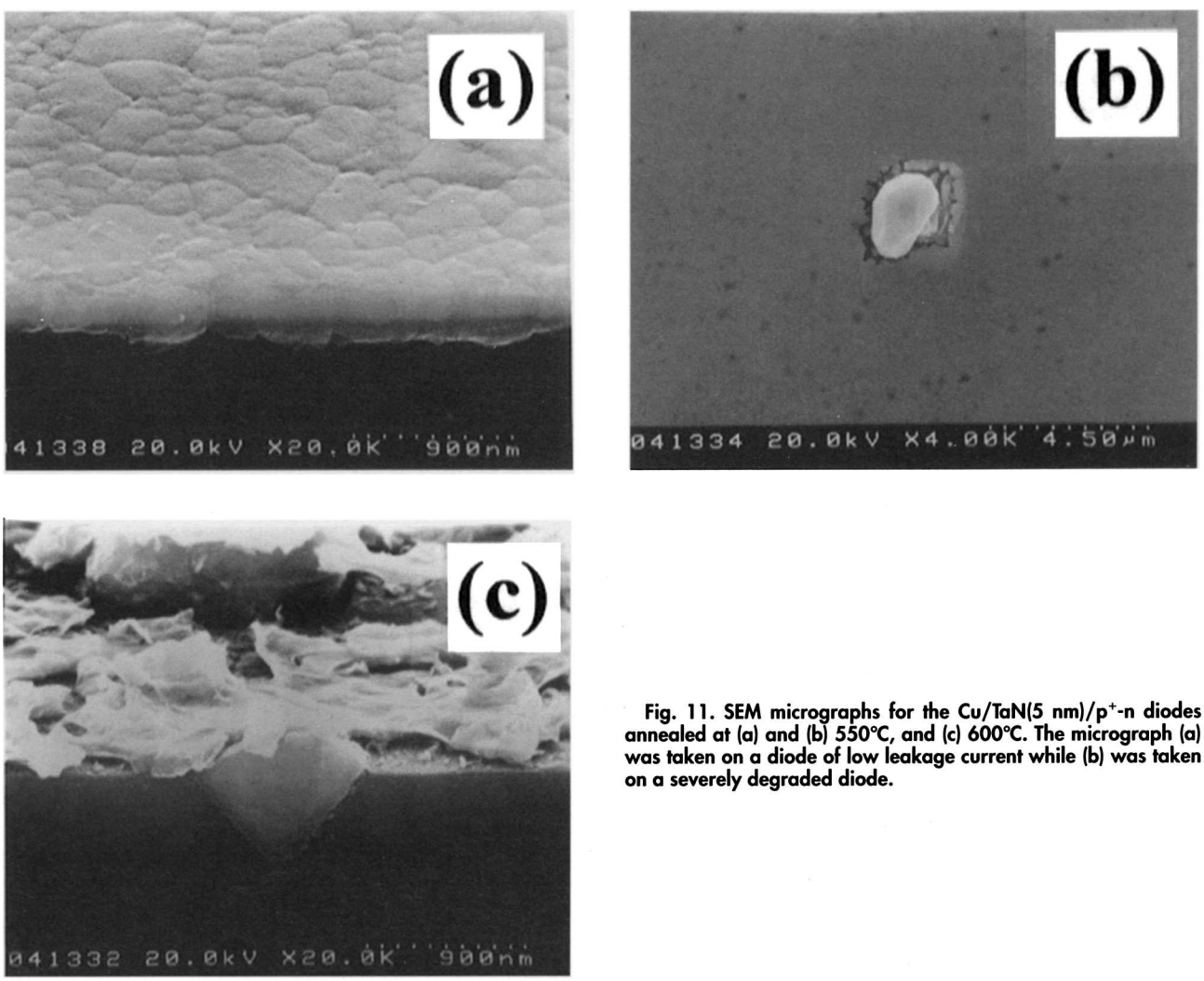


Fig. 11. SEM micrographs for the Cu/TaN(5 nm)/p^+-n diodes annealed at (a) and (b) 550°C, and (c) 600°C. The micrograph (a) was taken on a diode of low leakage current while (b) was taken on a severely degraded diode.

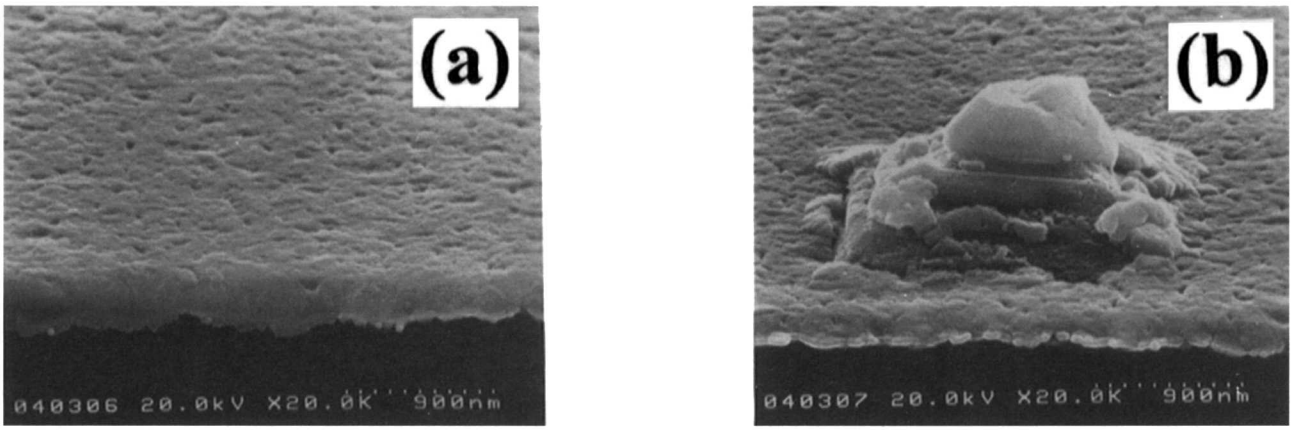


Fig. 12. SEM micrographs for the Cu/Ta(5 nm)/p^+-n diodes annealed at (a) 500 and (b) 550°C.

Comparative results of thermal stability for the multilayer structures studied in this work based on XRD analysis are summarized in Table II.

SEM observation.—SEM was used to investigate the surface and cross-sectional morphology of the thermally annealed Cu/barrier/p^+-n junction diodes. Figure 9 shows the surface morphology of Cu/TaN(25 nm)/p^+-n junction diodes annealed at 700 and 750°C. Surface morphology of the diodes remained stable after annealing at 700°C (Fig. 9a and b). After annealing at 750°C, some of the diodes degraded severely (with high leakage current) while the others were only slightly degraded with reverse bias leakage current density less than 100 nA/cm^2, as shown in Fig. 3. For those diodes showing only a slight degradation, surface morphology of the diodes is shown in Fig. 9c and d; only a number of small openings were observed on the surface. For those severely degraded diodes, Fig. 9e and f shows that there are highly localized protrusions on the diode's surface. Thus, failure of the devices is associated with these protrusions, which were presumably caused by Cu diffusion through the localized weak points in the TaN barrier layer. For the Cu/Ta(25 nm)/p^+-n junction diodes, SEM micrographs revealed that the device's structure was able to remain stable after annealing at 600°C, as shown in Fig. 10a; however, localized protrusions were found after annealing at 650°C, as shown in Fig. 10b.

Figure 11 shows the SEM micrographs for the Cu/TaN (5 nm)/p^+-n diodes annealed at 550 and 600°C. After annealing at 550°C, the diodes with a low leakage current density nearly retained their structural integrity (Fig. 11a), while a few highly localized protrusions were found for the diodes with a large leakage current density (Fig. 11b). After annealing at 600°C, dense localized protrusions were found on the surface of the annealed samples (Fig. 11c). For the Cu/Ta(5 nm)/p^+-n diodes, SEM observation revealed that the device's structure basically remained stable after annealing at 500°C (Fig. 12a). However, Cu penetrated the Ta barrier to form η''-Cu_3Si precipitate after annealing at 550°C. This precipitate extends into the Si substrate and out of the sample surface, as shown in Fig. 12b. Based on the results of SEM observation (Fig. 9, 10, 11, and 12) and electrical measurement (Fig. 2 and 3), we conclude that the electrical degradation for the thermally annealed Cu/barrier/p^+-n junction diodes is closely related to the presence of highly localized defects in the barrier layers. This suggests that the failure of very thin Ta and TaN barrier is principally due to permeation of Cu atoms through the barrier layer via local weak points (including grain boundaries) during the process of thermal annealing.

Conclusion

Thermal stability of very thin sputtered Ta and reactively sputtered TaN films used as a diffusion barrier between Cu and silicon substrate was investigated. We found that thermal stability of the Cu/barrier/Si system depends on the barrier thickness and that the presence of Cu film on the Ta and TaN barrier surface of the barrier/Si structure accelerated the formation of Ta silicide. The Cu/Ta/p^+-n junction diodes with a 25 nm thick Ta barrier were able to sustain a 30 min thermal annealing at temperatures up to 550°C without causing degradation to the device's electrical characteristics. For a 5 nm thick Ta barrier layer, thermal stability of the Cu/Ta/Si diodes was reduced to 450°C. The barrier capability of the sputtered Ta layer can be effectively improved by incorporation of nitrogen in the Ta layer using reactive sputtering technique. The Cu/TaN/p^+-n junction diodes with a 25 nm thick TaN barrier remained stable up to 700°C. For a 5 nm thick TaN layer, thermal stability of the Cu/TaN/p^+-n diodes was reduced to 500°C. The failure of very thin Ta and TaN barrier was not related to Ta silicidation at the barrier/Si interface; instead, Cu atoms diffused through the barrier layer during the process of thermal annealing via local defects, such as grain boundaries and stress-induced weak points, leading to failure of the barrier layer.

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Investigation of Boron Penetration Through Thin Gate Dielectrics Including Role of Nitrogen and Fluorine

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ABSTRACT

This work examines boron penetration from p^+ polysilicon through 50–70 Å gate dielectrics following B or BF_2 implantation. Gate oxides were grown in N_2O/O_2 mixtures with average nitrogen contents varying from 0 to 1.4%. A series of capacitance–voltage measurements were used to determine the amount of boron penetration, and secondary ion mass spectroscopy measurements were carried out to measure the depth profiles of incorporated nitrogen and fluorine. In addition, to better understand the role of fluorine, experiments were carried out to investigate the redistribution of fluorine in the poly/SiO_2/Si system.

Introduction

Scaling of complementary metal-oxide semiconductor (CMOS) processes down to submicron channel lengths greatly improves device density and circuit speed but introduces many challenges in process technology. One difficulty is the scaling of the gate dielectric, particularly for the fabrication of p^+ polysilicon gates in p-channel devices. The concern is the diffusion of boron through the gate oxide. Boron penetration from the p^+-polysilicon gates can cause fluctuations in flatband voltage (V_{FB})[1] which are accompanied by increases in electron charge trapping and inverse subthreshold slope.[2]

The diffusivity of boron can be modified by many factors. Increased boron diffusivity is observed when fluorine or hydrogen is introduced in the oxide.[3] In contrast, incorporation of nitrogen in SiO_2 is known[4,5] to reduce boron diffusivity. Injection of silicon interstitials in the oxide has also been suggested to decrease boron diffusivity.[6]

It has been proposed that boron diffusion increases with decreasing oxide thickness.[7] However, recent work has found no thickness dependence.[3,8,9] Aoyama et al.,[3] who have carried out perhaps the most extensive set of experiments on boron penetration in thin oxides, found no oxide thickness dependence on boron diffusion in the absence of fluorine. However, in the presence of fluorine, they extracted higher B diffusion for thinner oxides. The difference was attributed to the fact that the boron diffusion strongly depends on fluorine content of the oxide, which was presumed to vary with thickness.

Although B diffusion is expected to depend locally on the oxide structure and composition, modeling to date has been generally limited to determining an effective average diffusivity as a function of processing conditions.[5,7] To generate a predictive model, it is important to consider the underlying oxide composition and structure that results in the observed diffusivity. In order to help address these issues, we have conducted a series of experiments in which both boron diffusivity as well as the composition of the oxide were studied.

Experimental

MOS capacitors were fabricated on 4 in. silicon (100) wafers with background phosphorus doping of 2–4 Ω cm. A field oxide of 0.6 μm was grown and etched to define active areas (100 × 100 μm). Gate dielectrics were grown in pure O_2 at 870°C, pure N_2O at 910°C, or an N_2O/O_2 at 870°C mixture. Undoped polysilicon was deposited at 625°C immediately following gate dielectric growth. The polysilicon was implanted to a dose of 5×10^{15} cm^{-2}, using P^+ at 40 keV and BF_2^+ or B^+ at 25 keV. A low-temperature cap oxide of 0.5 μm was deposited at 425°C to avoid outdiffusion of boron. Wafers were annealed at 900–1050°C for various times to ensure boron penetration. After removal of the cap oxide, the polysilicon was patterned and etched. Aluminum deposition followed by sintering was performed on some samples and capacitance–voltage measurements showed no difference between capacitors with and those without aluminum electrodes.

Capacitors were characterized using high-frequency (100 kHz) capacitance–voltage (CV) measurements. In addition, secondary ion mass spectroscopy (SIMS) measurements were carried out[a] to quantify the amount of nitrogen and fluorine incorporation in the gate oxides, as well as in the polysilicon and substrate.

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[a] Performed by Evans East, Plainsboro, New Jersey.