Improving Radiation Hardness of EEPROM/Flash Cell By N_2O Annealing

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***Abstract*— The effects of an N_2O anneal on the radiation effects of a split-gate electrical erasable programmable read only memory (EEPROM)/flash cell with a recently-proposed horn-shaped floating gate were studied. We have found that although the cells appear to survive 1 Mrad(Si) Co^{60} irradiation without data retention failure, the write/erase cycling endurance was severely impeded after irradiation. Specifically, the write/erase cycling endurance was degraded to 20 K from the pre-irradiation value of 50 K. However, by adding an N_2O annealing step after the interpoly oxidation, the after-irradiation write/erase cycling endurance of the resultant cell can be significantly improved to over 45 K. N_2O annealing also improves the after-irradiation program and erase efficiencies. The N_2O annealing step therefore presents a potential method for enhancing the robustness of the horn-shaped floating-gate EEPROM/flash cells for radiation-hard applications.**

***Index Terms*—EEPROM/flash cells, horn-shaped floating-gate, N_2O annealing, and radiation hardness.**

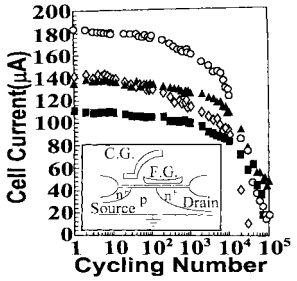

Fig. 1. The effect of write/erase cycling on the cell currents for the cells which were written in the "erase" (i.e., high-conducting) state, and remeasured immediately after irradiation (i.e., without applying an erase pulse after irradiation) for control cells before (square) and after (diamond) irradiation; and N_2O-Cells before (triangle) and after (circle) irradiation. Cell fails when the read current in the "erase" state falls below 40 μA (i.e., minimum current required for the sense amplifier to sense as "erase").

I. Introduction

NON-VOLATILE semiconductor memories are viable candidates for operations under harsh environments such as in military and space applications [1]–[4]. Under such harsh environments, device characteristics such as data retention and write/erase cycling endurance require careful considerations. Traditionally, electrical erasable programmable read only memory (EEPROM) employing metal-nitride-oxide semiconductor (MNOS) technology is employed because of the inherent radiation hardness of the MNOS technology which stores the charge in the nitride layer [1], [2]. Floating-gate EEPROM cells, on the other hand, are known to have less radiation hardness, and therefore remain relatively unexplored [3], [4]. This is because during irradiation, electron/hole pairs are generated. The generated holes could be trapped in the oxide, resulting in oxide degradation and electric field change. Some of the holes could also be injected into the floating-gate, neutralizing the stored electrons, causing data loss. Further, the stored electrons could also be emitted over the oxide/floating-gate barrier, causing additional data loss. These would eventually result in data retention failure during irradaition, due to the collapse of the "program" (i.e., high-threshold, low-conducting) state.

However, floating-gate EEPROM/flash cells have in recent years become the mainstream technology for nonvolatile memories. With the aggressive technology scaling and the accompanying reduction in oxide thickness which is known to improve the radiation hardness, it is therefore interesting and technologically important to re-evaluate the suitability of state-of-the-art floating-gate EEPROM/flash cells for the radiation-hard applications. Recently, we have proposed using an N_2O annealing of interpoly oxide to improve the performance of an EEPROM/flash cell with horn-shaped floating-gate [5], [6]. In this paper, we further report the significant improvement of the EEPROM/flash cell performance in terms of radiation hardness by the addition of an N_2O annealing [7].

II. Experiment

Detailed processing steps for fabricating flash cell with horn-shaped floating-gate, with its cross-sectional schemetics shown in the inset of Fig. 1, are described in [5], [6]. The floating gate length is 0.8 μm, the split gate length (i.e., the portion not overlapping the floating-gate) is 0.8 μm; while the width of the cell is 2.2 μm. Briefly, a 0.8-μm, double-level-polysilicon CMOS process was used with a 15-nm first gate oxide. A 170-nm polysilicon layer was deposited to form

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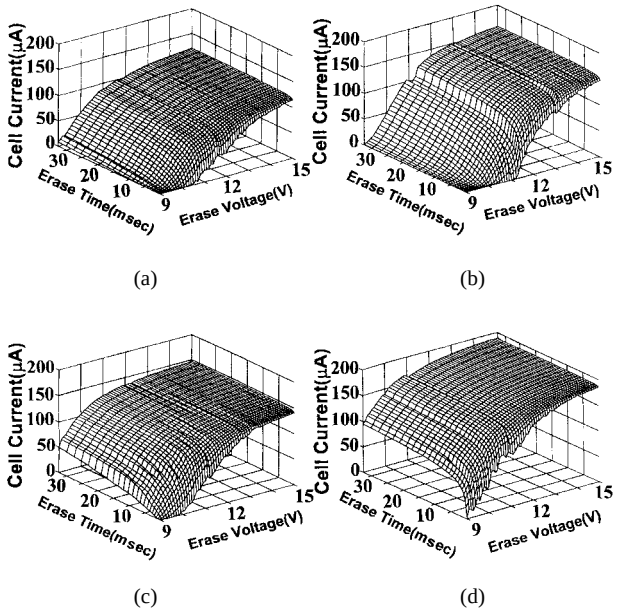

Fig. 2. The erase efficiency for (a) control cell before irradiation, (b) control cell after irradiation, (c) N_2O-cell before irradiation, and (d) N_2O-cell after irradiation.

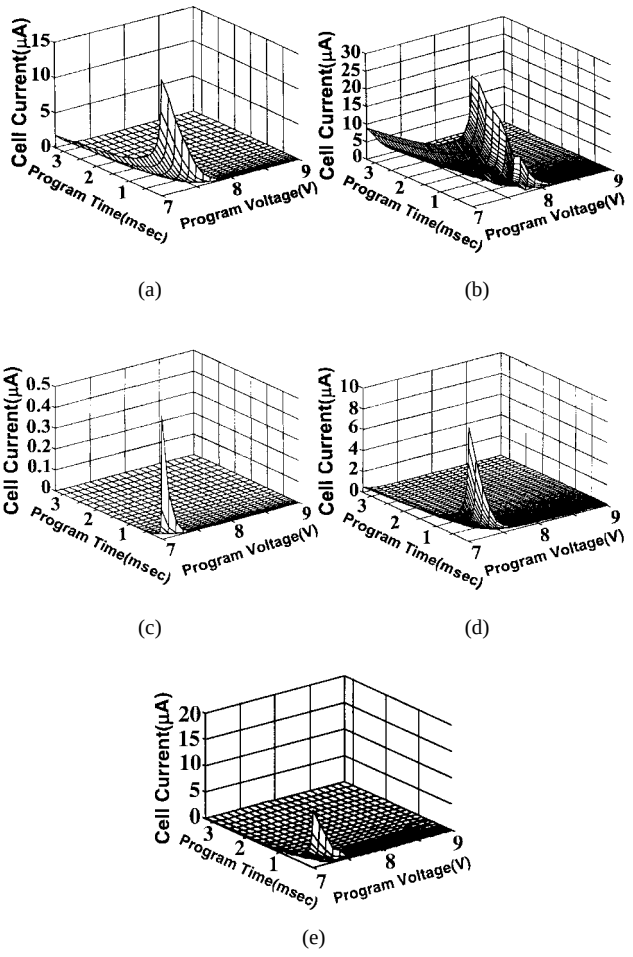

Fig. 3. The program efficiency for (a) control cell before irradiation, (b) control cell after irradiation, (c) N_2O-cell before irradiation, (d) N_2O-cell after irradiation, and (e) after subjecting the irradiated N_2O-cell to a 1000 write/erase cycling.

the floating gate. The horn-shaped floating-gate was created by performing a LOCOS-type oxidation on the floating-gate. Wafers were then split to receive the polyoxide oxidation. For the control split, the polyoxide was grown by a conventional dry O_2 oxidation at 900 °C. While for the N_2O-annealed split, polyoxide was first grown in the dry O_2 oxidation at 900 °C, followed by an N_2O anneal for 15 min at 925 °C. Both splits have comparable final polyoxide thickness. The final oxide thickness at the thickest region is 220 nm.

For the write/erase cycling test, a 14-V 800-μs pulse was applied to the control gate, with source and drain grounded, so as to facilitate interpoly Fowler–Nordheim tunneling for the erase (i.e., erase to "high-conducting state") operation [6]. For programming (i.e., to low-conducting state) the cell with source-side hot-electron injection [8], the drain was held at 12 V, the source at 0.6 V, the substrate at ground, and a 2-V, 800 μs pulse was applied at the control gate. The cell read current was measured by applying 4-V to the control gate, 2 V to the source, while substrate and drain were grounded. For program efficiency test, the cell current was read when the drain voltage was varied with the control gate at 2 V, source at 0.6 V and the substrate at ground. For the erase efficiency test, the cell current was read when the control gate was varied with all other terminals grounded. For radiation study, flash cells were subjected to a radiation from a cobalt-60 source with 1 MRad(Si) dose, and their characteristics were remeasured.

III. Results and Discussion

The effects of irradiation on the write/erase cycling endurance are plotted in Fig. 1 for the cell currents on the cells which were written in the "erase" state prior to irradiation, and were remeasured immediately after irradation (i.e., without applying an erase pulse after irradiation). It is noted that the cell read current actually increases (i.e., an improvement) immediately after irradiation. While for the "program" state, cell current increases (i.e., a degradation) from the pre-irradiation value of 10 pA to about 10 nA immediately after irradiation, and then remains essentially unchanged when subjecting to cycling for both the control and the irradiated cells (data not shown). Since the sense amplifier reference current in our flash cell circuit design is 40 μA, our results show that the cells survive the data retention test after subjecting to 1 Mrad(Si) Co^{60} irradiation (i.e., no toggling of state by irradiation) under both the "erase" and "program" states. This improvement over previous literature's data is believed to be due, at least in part, to the unique cell structure with a thick polyoxide and thin first gate oxide which is known to be beneficial to radiation hardness [3]. However, despite the improvement of initial cell read current in the "erase" state immediately after irradiation, the irradiated cell's read current degrades much more rapidly than that of its nonirradiated counterpart when subjected to write/erase cycling. The after-irradiation endurance degradation rate during write/erase cycling is especially severe for the control cells without N_2O annealing. As a result, the irraidated control cell fails cycling endurance at only about 20 K cycles, due to a fast collapse of the "erase" state (i.e., 40 μA is the minimum current required for the sense amplifier to sense

as "erase"). In contrast, the irradiated N_2O-cell fails cycling endurance at about 45 K cycles. The improvements in the N_2O-cells come from two folds, i.e., a larger initial cell current and a less steep degradation slope during cycling, due to the formation of interfacial oxynitride layer, resulting in a reduced barrier lowering for electron injection and reduced electron trapping by the N_2O anneal [5].

The effects of irradiation on the program and erase efficiencies are also studied. As shown in Fig. 2, the erase efficiency actually improves after irradiation for both the control and N_2O-cells. We believe this is due to hole trappings at the oxide/floating-gate interface as a result of irradiation [3], which serve to increase the interpoly electric field during the "erase" operation in our cells. Since our cell employs a strong drain overlap to couple the drain voltage effectively to the floating-gate, the effect of the positive charge in the first gate oxide on the "erase" efficiency is believed to be minimal. On the other hand, the program efficiency after irradiation is degraded, as shown in Fig. 3. This degradation is especially severe for the control cell without N_2O anneal. This can be explained by hole trappings which occur at the oxide/silicon substrate interface as a result of irradiation. During programming, electrons generated by source-side injection are injected into the gate oxide. Some of these injected electrons will recombine with trapped holes, thus reducing the total amount of electrons which can reach the floating-gate, causing a reduction in the programming efficiency. As shown in Fig. 3(e), our measurements indeed confirmed that during subsequent W/E cycling, part of the holes could be passivated and the program efficiency actually showed a partial recovery.

IV. Conclusion

In this paper, we have studied the effects of N_2O annealing on the radiation hardness of a recently-propsoed EEPROM/flash cell with horn-shaped floating gate. Our results show that both the control and N_2O-annealed cells appear to survive after 1 Mrad(Si) Co^{60} irradiation without data retention failure, a significant improvement over previous literature report. However, despite an initial improvement in after-irradiation cell read current in the "erase" state, the cell current degrades more rapidly, especially on the control cells without N_2O anneal. As a result, the write/erase cycling endurance are significantly degraded after irradiation. By adding an N_2O annealing step after the interpoly oxidaiton, the after-irradiation cycling endurance can be significantly improved to over 45 K, compared to 20 K for the control cells; thus significantly improving the radiation-hardness of the resultant cell. N_2O annealing is also shown to improve the after-irradiation program and erase efficiencies. The addition of an N_2O annealing step thus presents a viable method for further enhancing the robustness of the horn-shaped floating-gate EEPROM/flash cells for radiation-hard applications.

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