A Parallel Structure for CMOS Four-Quadrant Analog Multipliers and Its Application to a 2-GHz RF Downconversion Mixer

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***Abstract*—A parallel structure for a CMOS four-quadrant analog multiplier is proposed and analyzed. By applying differential input signals to a set of combiners, the multiplication function can be implemented. Based on the proposed structure, a low-voltage high-performance CMOS four-quadrant analog multiplier is designed and fabricated by 0.8-μm N-well double-poly-double-metal CMOS technology. Experimental results have shown that, under a single 1.2-V supply voltage, the circuit has 0.89% linearity error and 1.1% total harmonic distortion under the maximum-scale input 500-mV$_{P\text{-}P}$ at both multiplier inputs. The -3-dB bandwidth is 2.2 MHz and the dc current is 2.3 mA. By using the proposed multiplier as a mixer-core and connecting a newly designed output buffer, a CMOS RF downconversion mixer is designed and implemented by 0.5-μm single-poly-double-metal N-well CMOS technology. The experimental results have shown that, under 3-V supply voltage and 2-dBm LO power, the mixer has -1-dB conversion gain, 2.2-GHz input bandwidth, 180-MHz output bandwidth, and 22-dB noise figure. Under the LO frequency 1.9 GHz and the total dc current 21 mA, the third-order input intercept point is $+7.5$ dBm and the input 1-dB compression point is -9 dBm.**

***Index Terms*—Analog multiplier, low voltage, RF mixer, wireless communication.**

I. Introduction

It is known that the analog multiplier is an important building block in analog signal processing systems. It can be applied to phase comparators, frequency mixers, and neural networks. Generally, the analog multipliers in different applications have different requirements. In the application of phase comparators, the phase delays from both input ports to the output port of the multipliers should be equal. This means that the multipliers should have a symmetric structure. In the application of radio-frequency (RF) mixers, the linearity, frequency response, and the port-to-port isolation of the multipliers are important characteristics. In the application of neural networks, both chip area and power consumption of the multipliers are important issues. So far, many high-performance CMOS analog multipliers have been proposed [1]–[10]. Among them, the proposed multiplier structures in [1]–[3] are asymmetric. The multiplier structure in [4] uses resistive divider and thus has low port-to-port isolation. The multipliers in [5]–[8] have a complex structure and thus the bandwidth is limited. The multipliers in [9] and [10] have a large chip area.

In this paper, a parallel structure for CMOS analog multipliers is proposed, which can be designed to satisfy the different requirements in different applications. The proposed multiplier structure is based on the quarter-square identity implemented by using six combiners [11]. It has a simple and symmetric architecture and can be designed to achieve high bandwidth with high port-to-port isolation, or small chip area with small power dissipation for different applications. Moreover, the most noticeable feature of the proposed multiplier structure is its capability of low-voltage operation. Unlike other low-voltage analog multipliers which use at least two stacked transistors [12]–[15], the proposed multiplier uses only one stacked transistor. Thus it can be operated at lower supply voltage of 1.2 V while sustaining high linearity under high input signal swing. This feature make the proposed multiplier very suitable for the battery-operated portable systems.

Recently, due to the increasing demand on high-performance low-cost wireless communication systems, more and more effort has been devoted to the implementation of CMOS RF mixers [16]–[18]. These mixers have good performance and are suitable for the application of wireless systems. In this paper, as an illustrative application example of the proposed multiplier structure, an RF downconversion mixer is designed by using the proposed multiplier as the mixer-core and a new operational-transconductance-amplifier (OTA) buffer as the output stage. The proposed RF mixer has high input/output bandwidth while sustaining high linearity. Thus it can be applied to either zero-IF or dual-conversion receivers.

In Section II, the operational principle, circuit realization, and experimental results of the proposed analog multiplier are presented. In Section III, the design methodology and the experimental results of the RF downconversion mixer are given. In Section IV, a conclusion is given.

II. Multiplier Design

A. Operational Principle

The block diagram of the proposed analog multiplier is shown in Fig. 1. In Fig. 1, the six blocks Com_1–Com_6 are called the combiners because they combine the input signals to form the output. The output functions of the combiners can

Manuscript received April 3, 1997; revised December 1, 1997. This work was supported by the National Science Council (NSC), Taiwan, ROC, under Grant NSC-86-2221-E-009-080.

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Publisher Item Identifier S 0018-9200(98)03505-7.

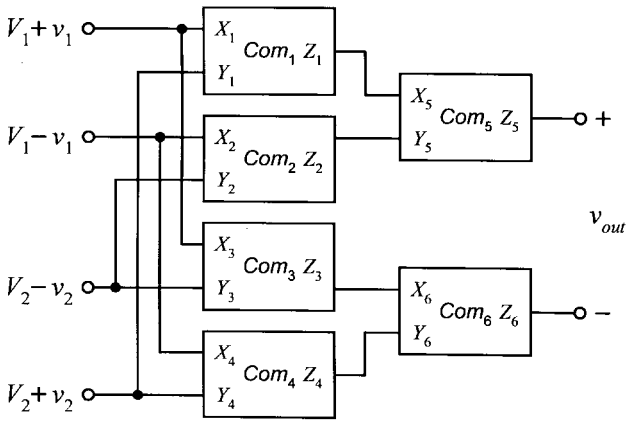


Fig. 1. The proposed structure of the analog multiplier using six combiners.

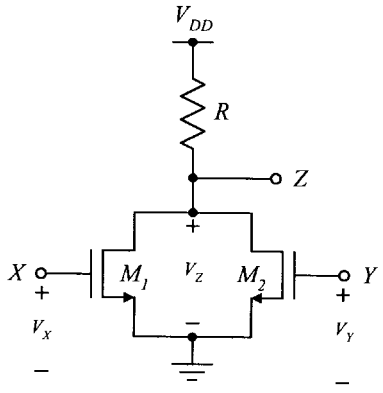


Fig. 2. The circuit diagram of the combiner.

be expressed as

$$Z_i = A_1X_i^2 + A_2Y_i^2 + A_3X_i + A_4Y_i + A_5 \quad (i = 1\text{–}4) \tag{1a}$$

$$Z_i = B_1X_i^2 + B_2Y_i^2 + B_3X_i + B_4Y_i + B_5 \quad (i = 5,\ 6) \tag{1b}$$

where Z_i is the output of the combiner *Com*$_i$$(i = 1\text{–}6)$, X_i and Y_i are the inputs to *Com*$_i$, and A_1–A_5 and B_1–B_5 are constants. Generally, (1) is the second-order functions. If the constants A_1, A_2, B_1, and B_2 in (1) are set to zero, (1) is reduced to the first-order functions similar to those in [4].

As shown in Fig. 1, the input signals of the multiplier are applied to *Com*$_1$–*Com*$_4$, whereas the output is taken as the difference of the outputs of *Com*$_5$ and *Com*$_6$. Assume that the common-mode dc voltages V_1 and V_2 are imposed upon the input signals $\pm v_1$ and $\pm v_2$, respectively. Then the inputs to X_1 and X_3 (X_2 and X_4) are written as $V_1 + v_1$ ($V_1 - v_1$) whereas those to Y_2 and Y_3 (Y_1 and Y_4) as $V_2 - v_2$ ($V_2 + v_2$), as shown in Fig. 1. The output of *Com*$_1$–*Com*$_4$ Z_1–Z_4 can be obtained by substituting the input voltages of X_i and Y_i $(i = 1\text{–}4)$ into (1a). After that, Z_5 and Z_6 can be derived from (1b). The output signal is given by $v_{\text{out}} = Z_5 - Z_6$. Through some calculations, it can be found that if $B_1 = B_2$ and $B_3 = B_4$, the undesired terms in the expression of v_{out} can be cancelled, and the resultant v_{out} is

$$v_{\text{out}} = 8B_1(2A_1V_1 + A_3)(2A_2V_2 + A_4)v_1v_2 = K'v_1v_2. \tag{2}$$

Thus, the output is a linear multiplication of v_1 and v_2 with the multiplication constant $K' = 8B_1(2A_1V_1 + A_3)(2A_2V_2 + A_4)$. This verifies the multiplication function of the analog multiplier structure in Fig. 1.

The key component in the multiplier of Fig. 1 is the combiner. Any circuit that performs the function in (1) can be used as the combiner. To form the multiplier with the combiners, the constraints are $B_1 = B_2$ and $B_3 = B_4$.

B. Circuit Realization

The second-order transfer function in (1) can be implemented by the MOS transistors. To implement the combiner using the MOS transistors, a parallel circuit structure is proposed as shown in Fig. 2, where the drain terminals of two MOS transistors M_1 and M_2 are connected to the resistor R. The transfer characteristic of the combiner in Fig. 2 can be modeled by the drain current equation of MOS transistors in the saturation region. Since the nonideal effects of channel-length modulation and mobility degradation can be efficiently suppressed in the analog multiplier structure of Fig. 1, the ideal drain current equation is used to model both combiner and multiplier, and then the nonideal effects will be discussed. Using the ideal square-law current identity of the MOS transistors, the drain current I_D can be expressed as

$$I_D = K(V_{GS} - V_T)^2 \tag{3}$$

where $K = \mu_S(C_{ox}/2)(W/L)$ is the transconductance parameter, μ_S is the effective surface carrier mobility, C_{ox} is gate oxide capacitance per unit area, $W(L)$ is the channel width (length) of the MOS device, V_{GS} is the gate-source voltage, and V_T is the threshold voltage. If M_1 and M_2 are in the saturation region, the voltage V_Z at the drain terminal of the combiner becomes

$$\begin{aligned} V_Z &= V_{DD} - R\left[K_1(V_X - V_T)^2 + K_2(V_Y - V_T)^2\right] \\ &= -RK_1V_X^2 - RK_2V_Y^2 + 2RK_1V_TV_X + 2RK_2V_TV_Y \\ &\quad + \left(V_{DD} - RK_1V_T^2 - RK_2V_T^2\right). \end{aligned} \tag{4}$$

It can be found that (4) is the same as the required function (1).

The complete analog multiplier can be obtained by connecting the combiners as shown in Fig. 1. The resultant circuit diagram is shown in Fig. 3. In *Com*$_1$–*Com*$_4$, the value of the resistors R_{bi}, $i = 1\text{–}4$, is R_b, whereas all the MOSFET's M_{ai} (M_{bi}) are identical with the same $K_a(K_b)$. Substituting R_b, K_a, and K_b into (4) and comparing to (1a), one can obtain the corresponding coefficients A_1–A_5 as

$$\begin{aligned} A_1 &= -R_bK_a \\ A_2 &= -R_bK_b \\ A_3 &= 2R_bK_aV_T \\ A_4 &= 2R_bK_bV_T \\ A_5 &= V_{DD} - R_bK_aV_T^2 - R_bK_bV_T^2. \end{aligned} \tag{5}$$

In *Com*$_5$ and *Com*$_6$, the value of the resistors R_{c1} and R_{c2} is R_c, whereas all the MOSFET's M_{ci} are identical to the same

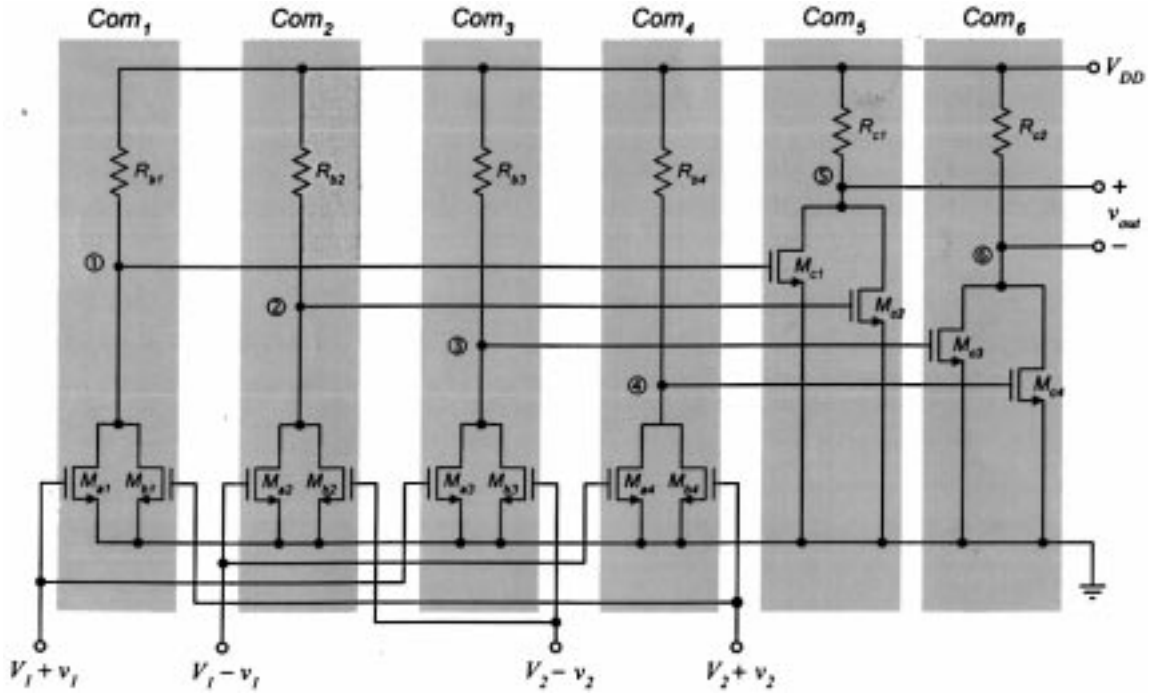


Fig. 3. The circuit diagram of the proposed analog multiplier.

K_c. Substituting R_c and K_c into (4) and comparing to (1b), one can obtain the corresponding coefficients B_1–B_5 as

$$\begin{aligned} B_1 &= B_2 = -R_cK_c \\ B_3 &= B_4 = 2R_cK_cV_T \\ B_5 &= V_{DD} - 2R_cK_cV_T^2. \end{aligned} \tag{6}$$

Thus, the output voltage v_{out} can be derived by substituting A_1–A_5 in (5) and B_1–B_5 in (6) into (2). The result is

$$\begin{aligned} v_{\text{out}} &= \left[-32R_cK_cR_b^2K_bK_a(V_1 - V_T)(V_2 - V_T)\right]v_1v_2 \\ &= K'v_1v_2. \end{aligned} \tag{7}$$

The multiplication function is thus realized.

One of the advantages of the new structure in Fig. 3 is that the supply voltage can be very low. The minimum supply voltage of the circuit is determined by the required input signal swing. As in Fig. 3, the input signal range is between V_{DD} and V_T. If the input signal swing is 0.5 V and V_T is 0.7 V, the minimum supply voltage $V_{DD\,\text{min}}$ is 1.2 V.

In order to perform the multiplication function, all the transistors in the circuit should be kept in the saturation region under the maximum input signal. Thus, the minimum voltage at the nodes ①–④, which occurs when both inputs are at V_{DD}, should be high enough to keep the transistor M_c on and both the transistors M_a and M_b in the saturation region. Thus the design equation can be written as

$$V_{DD} - R_b(K_a + K_b)(V_{DD} - V_T)^2 > \max(V_T, V_{DD} - V_T). \tag{8}$$

The similar restriction is also imposed at the nodes ⑤ and ⑥. The minimum voltage at the nodes ⑤ or ⑥, which occurs when one of the inputs v_1 or v_2 is at the maximum voltage and the other at the minimum, should be high enough to keep the transistor M_c in the saturation region. Thus we have

$$V_{DD} - R_cK_c\left(V_{L1}^2 + V_{L2}^2\right) > \max(V_{L1}, V_{L2}) \tag{9}$$

where

$$\begin{aligned} V_{L1} &= V_{DD} - V_T - R_bK_a(V_{DD} - V_T)^2 \\ V_{L2} &= V_{DD} - V_T - R_bK_b(V_{DD} - V_T)^2. \end{aligned} \tag{10}$$

Equations (7)–(10) provide the design guideline for the proposed multiplier. For a given V_{DD}, the values of R_b, K_a, and K_b can be designed by using (8). After that, the values of R_c and K_c can be determined from (8) and (9).

It is noted that, unlike some analog multipliers whose input range at one input is dependent on that at the other input [19]–[23], both inputs of the proposed multiplier can swing to V_{DD} simultaneously. Thus they have the same input range. Furthermore, the circuit can be designed to be either symmetric or asymmetric by setting the values of K_a and K_b. With the above advantageous features, the proposed multiplier can be applied to various applications.

C. Nonideal Effects

The above derivation of the multiplication function is based on the assumptions of perfect square-law MOSFET characteristics and completely matched devices. However, some nonideal effects exist to affect the multiplication function. The nonideal effects include mobility degradation effect and channel-length modulation effect of MOS devices as well as device mismatches due to process variations. For simplicity, the high-order terms are neglected in modeling the nonideal effects on the multiplier structure. Thus mobility degradation effect and channel-length modulation effect can be modeled separately.

TABLE I
THE EXTRA TERMS GENERATED BY THE ELEMENT MISMATCHES IN THE MULTIPLIER

Extra Terms	Mismatch Items					
	K_a, K_b	K_c	V_{Ta}, V_{Tb}	V_{Tc}	R_b	R_c
dc offset	√	√	√	√	√	√
v_1	√	√	√	√	√	
v_2	√	√	√	√	√	
v_1^2	√	√	√	√	√	√
v_2^2	√	√	√	√	√	√
$v_1^2 v_2$	√	√	√		√	
$v_1 v_2^2$	√	√	√		√	
v_1^3	√	√	√		√	
v_2^3	√	√	√		√	
$v_1^2 v_2^2$	√	√			√	√
v_1^4	√	√			√	√
v_2^4	√	√			√	√

Taking into account the mobility degradation effect, the current equation of the MOS transistors can be written as

$$I_D = K\frac{(V_{GS}-V_T)^2}{1+\theta(V_{GS}-V_T)} \tag{11}$$

where θ is the mobility reduction parameter. Using (11) to derive the output voltage of the multiplier and ignoring the high-order terms of θ, the output voltage v_{out} becomes

$$\begin{aligned} v_{\text{out}} = &\Big\{1-\tfrac{3}{2}(V_1-V_T)\theta_a-\tfrac{3}{2}(V_2-V_T)\theta_b \\ &-3\big[R_bK_a(V_1-V_T)^2 \\ &\quad +R_bK_b(V_2-V_T)^2-V_{\text{DD}}+V_T\big]\theta_c\Big\}K'v_1v_2 \\ &-\left[\frac{1}{2(V_1-V_T)}\theta_a+3R_bK_a\theta_c\right]K'v_1^3v_2 \\ &-\left[\frac{1}{2(V_2-V_T)}\theta_b+3R_bK_b\theta_c\right]K'v_1v_2^3 \end{aligned} \tag{12}$$

where θ_a, θ_b, and θ_c are the mobility reduction parameters of the transistors M_a, M_b, and M_c, respectively, and K' is the multiplication constant defined in (7).

Taking into account the channel-length modulation effect, the current equation of the MOS transistors can be written as

$$I_D = K(V_{GS}-V_T)^2(1+\lambda V_{DS}) \tag{13}$$

where λ is the channel-length modulation parameter. The output voltage considering the channel-length modulation effect can be found in [24].

The linearity of the multiplier has been simulated by HSPICE using a level 6 device model. The results have shown that the maximum-scale total harmonic distortion (THD) without considering the device mismatch effect is very small compared to the THD with considering the mismatch effect. This means the dominant error source of the proposed multiplier is the device mismatch. This is because the multiplication function in (7) is realized by cancelling the undesired terms at the output, which relies on the matching characteristics of the devices. In the multiplier circuit of Fig. 3, the parameters required to be matched are the transconductances K_a, K_b, and K_c; the threshold voltages V_{Ta}, V_{Tb}, and V_{Tc}; and the resistances R_b and R_c. Due to the device mismatches, the extra terms other than the multiplication term can be found through theoretical calculation [24]. The extra terms generated by the mismatched parameters are listed in Table I. It can be seen from Table I that the matching characteristics of the parameters K_a, K_b, K_c, and R_b are more important than other matching parameters. Generally, better matching characteristics can be obtained by using larger dimensions of transistors and resistors. However, the chip area consumption and frequency performance could be degraded at the same time. Thus, tradeoff should be encountered in the circuit design.

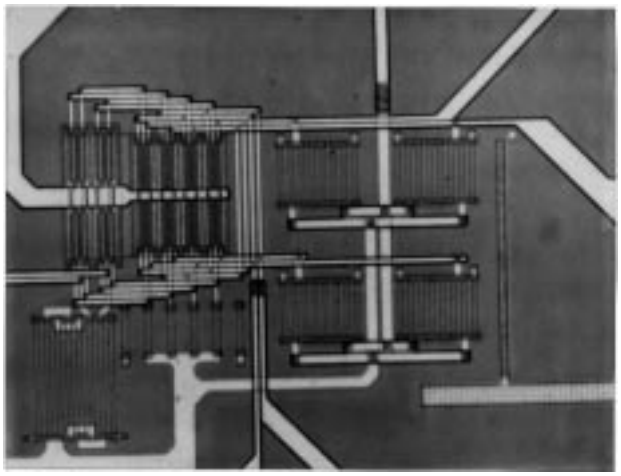


Fig. 4. The microphotograph of the fabricated analog multiplier.

In the design of the proposed multiplier structure, both transistor dimensions and resistor values can be chosen to achieve the optimal gain, dynamic range, bandwidth, or noise performance according to the application requirement. In this case, the proposed multiplier structure is designed to be operated at the minimum supply voltage while maintaining high-linearity characteristic and small chip area. The design criterion is to maximize the signal swing while keeping all the active devices in the saturation region. The resultant aspect ratio in micrometers of the transistors are $(W/L)_a = (W/L)_b = 50/1$ and $(W/L)_c = 50/2$, whereas the resistor values are $R_b = 400\ \Omega$ and $R_c = 4\ \text{k}\Omega$ with the width 4.2 and 3 μm, respectively. By using these parameters, the SPICE Monte Carlo simulations with 0.03-V standard deviation of V_T and 0.02-μm standard deviation of dimensions in both the transistors and resistors have been performed. The results show that the THD is about 1%. The THD can be further reduced by using longer channel transistors. The simulations have shown that, with the channel lengths of transistors increased four times and other parameters adjusted to maintain the same signal swing, the THD can be reduced to 0.5% due to the reduced channel-length mismatch errors.

D. Experimental Results

The designed CMOS analog multiplier with $V_{DD} = 1.2$ V is fabricated by 0.8-μm N-well double-poly-double-metal CMOS technology with the nominal threshold voltage $V_T = 0.7$ V. The resistors in the circuit are implemented by n^+ poly resistors. The microphotograph of the experimental chip is

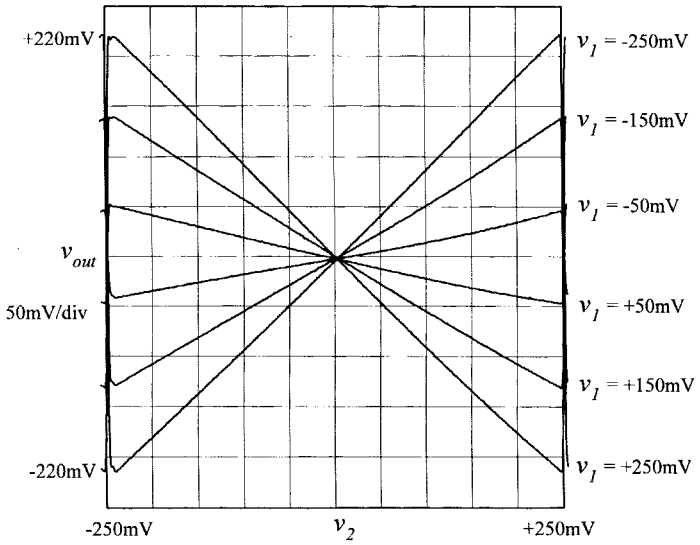


Fig. 5. The measured dc transfer characteristics of the fabricated analog multiplier with the input signal voltages v_1 and v_2 between ± 250 mV.

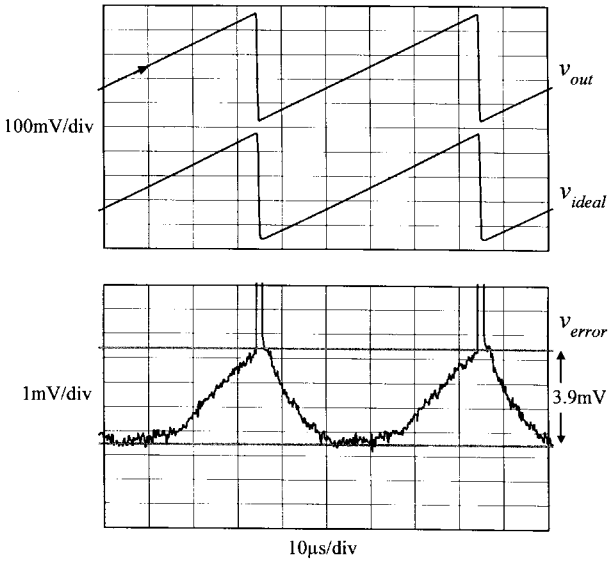


Fig. 6. The measured maximum-scale linearity error of the fabricated multiplier.

shown in Fig. 4. The active chip area is $114 \times 199\ \mu m^2$. In the measurements of the fabricated multiplier, an arbitrary waveform generator with 1-mV resolution is used to generate the required differential input signals.

Fig. 5 shows the measured dc transfer characteristics of the fabricated analog multiplier with the input voltages v_1 and v_2 between ± 250 mV and the corresponding maximum output swing ± 220 mV. The linearity measurement is performed by supplying v_1 and v_2 with ± 250 mV dc and ± 250 mV voltage ramp, respectively, and measuring the voltage difference between v_{out} and an ideal voltage ramp with equal amplitude. The measured waveforms are shown in Fig. 6 where the top waveform is the measured v_{out}, the middle waveform is an ideal voltage ramp v_{ideal}, and the bottom waveform is the error voltage $v_{error} = v_{\text{out}} - v_{ideal}$. As shown in Fig. 6, the maximum-scale linearity error is 3.9 mV/440 mV = 0.89%. Fig. 7 shows the measured harmonic distortion

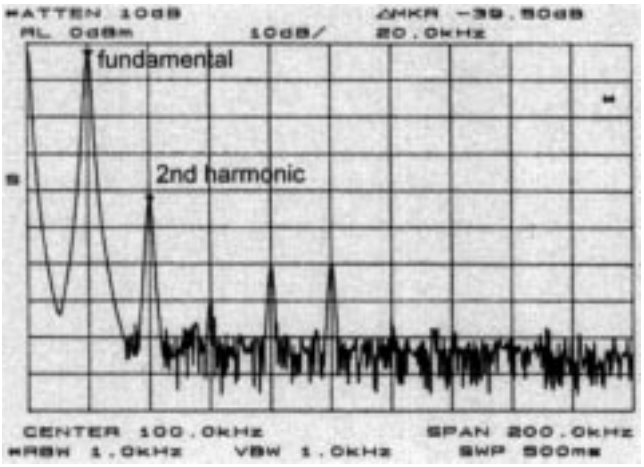


Fig. 7. The measured harmonic distortion of the fabricated analog multiplier under the maximum-scale inputs.

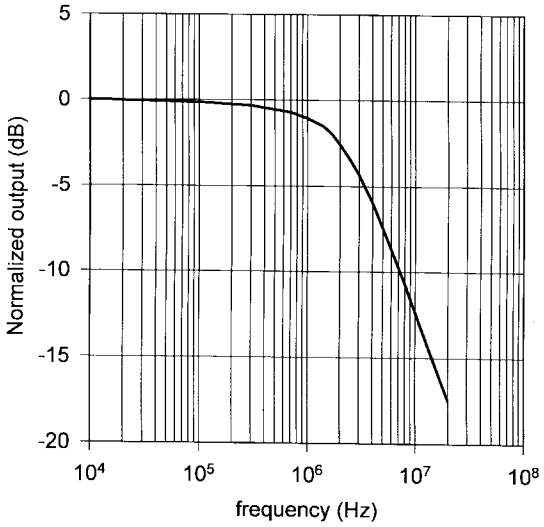


Fig. 8. The measured frequency response of the fabricated multiplier.

of the fabricated multiplier, where ± 250-mV dc voltage and 20-kHz 500 $mV_{P\text{-}P}$ sinusoidal wave are applied to v_1 and v_2, respectively. In Fig. 7, the maximum-scale total harmonic distortion is 1.1%.

The frequency response of the fabricated multiplier is shown in Fig. 8 where the measured -3-dB bandwidth is 2.2 MHz. This bandwidth is limited by the RC low-pass section formed by the multiplier output resistance of 4 kΩ and the package capacitance about 18 pF. If an output buffer is used to reduce the output capacitance of the multiplier, the signal bandwidth can be much higher. This will be verified in the design of RF mixers. Since the multiplier is symmetric, the measurement results remain the same where the input voltages v_1 and v_2 are interchanged. The measurement results of the fabricated analog multiplier are summarized in Table II.

III. RF Mixer

A. Mixer Characteristics

In the RF mixers, the important design parameters are noise figure (NF), conversion gain (CG), third-order input-intercept-

TABLE II
THE MEASURED CHARACTERISTICS OF THE FABRICATED ANALOG MULTIPLIER

Parameter	Value
Technology	0.8μm
VDD	1.2V
Input Range	$500mV_{P-P}$
Output Swing	$440mV_{P-P}$
Linearity Error	0.89%
THD	1.10%
Bandwidth	2.2MHz
DC current	2.3mA

point (IIP_3), input bandwidth, output bandwidth, port-to-port isolation, and local oscillator (LO) power. These parameters should be designed to meet the requirements of various standards for different wireless communication systems.

In this paper, the proposed mixer is intended to be used as the RF downconversion mixer in the wireless receiver. The RF downconversion mixer is often placed after a low-noise amplifier (LNA). The LNA provides sufficient power gain to mask the noise contribution of the subsequent stages. Thus the noise figure contributed by the mixer can be ignored if its value is lower than the total gain of the previous stages. For a receiver with 20-dB gain contributed by LNA, the NF of the mixer should be lower than 20 dB.

Since the LNA has provided sufficient gain, the CG of the mixer should not be high to overdrive the subsequent stages. Higher gain also implies higher signal swing in the circuit, which could degrade the linearity and the dynamic range. Nevertheless, very low gain far below 0 dB is also unacceptable because the noise contributed by the stages after the mixer becomes higher. Thus the value of CG around 0 dB is acceptable.

In modern wireless systems, the receivers could be subject to an environment with large adjacent-channel interfering signals. Due to the nonlinearity of the receiver, those interfering signals produce co-channel interference which degrades the signal-to-noise-ratio of received signals. Thus, IIP_3 of the receiver, which indicates the ability of the receiver to reject the interfering signals, becomes a very important feature of the RF receiver. In most cases, the signal power handled by the RF mixer is higher than those by the other stages in the receiver. Thus, IIP_3 of RF mixers is a critical parameter in the receiver design. In order to sustain a high receiver linearity, IIP_3 of the mixer should be as high as possible.

To cover the interested signal frequency ranges according to the standard, both the input bandwidth in the RF port and the output bandwidth in the IF port of the mixer should be high enough. For the application of modern wireless systems, the required input bandwidth is 900 MHz or 1.9 GHz. But the output bandwidth requirement depends on the architecture of the receiver. In a dual-conversion receiver, the IF is about 70–100 MHz for the 900-MHz system or 90–240 MHz for the 1.9-GHz system [25]–[28]. In a zero-IF receiver, the output bandwidth of a few megahertz is enough.

The port-to-port isolation and LO power are also important issues in the mixer design. The LO power in the order of a few dBm is often required by the mixer to obtain high linearity and high dynamic range. Such a high LO power causes the LO energy leaks through the RF port and radiates from the antenna if the port isolation of the mixer is not high enough. The design criteria of the mixer is to keep the LO power as low as possible and increase the port isolation.

B. Buffer Design

When the mixer is not integrated with the IF circuits, the IF output of the mixer is required to drive a low-impedance load such as an external filter or the instrument impedance. However, the circuit in Fig. 3 is not suitable for driving the low-impedance load. Thus an output buffer is required. In order to keep the IF signals undistorted, the buffer should have high driving capability with high linearity and high bandwidth. The conventional buffer amplifier has sufficient driving capability, but its bandwidth is not high enough [29]–[31]. Therefore, a new high-performance OTA buffer is designed.

Fig. 9 shows the circuit diagram of the proposed OTA buffer which consists of an input stage, a predriver stage, and an output stage. The input stage performs the subtraction of the input signals and provides a little gain to compensate the loss of the predriver stage. The polysilicon resistors R_1 and R_2 are chosen as load elements because they have higher frequency response and higher signal swing than the active loads. The predriver stage performs level-shifting and single-to-differential conversion of the signals from the input stage. The output stage is a push–pull stage driven by two level-shifted signals from the opposite side. This cross-coupled scheme provides additional common-mode rejection for the circuit.

In order to operate the circuit under the best condition, the level-shifted signals driving the output stage should have equal amplitude, which requires the transistors M_8–M_{11} to have matched transconductances. Moreover, the dimensions of the transistors M_{12}–M_{15} should be matched to those of M_8–M_{11}. If these matching requirements are met, the currents flow through both PMOS and NMOS transistors of the output stage are matched and the second-harmonic distortion of the output current can be dramatically reduced. This phenomenon is illustrated in Fig. 10 where the currents flow through both PMOS and NMOS transistors of the output stage and the combined output current on a 50-Ω load are drawn as a function of the input voltage. As seen in Fig. 10, the combined output current has a larger linearity range than those obtained by driving a single transistor. Thus high linearity can be obtained with low output transistor bias currents. In addition to the high-linearity characteristic, the buffer also benefits from the low-impedance nodes ①–⑥ in the circuit. Thus, high-frequency response can be obtained. The buffer is intended for open-loop operation and no compensation is employed.

The supply voltage of the buffer is determined by the required signal swing at the nodes ③–⑥. The maximum signal swing at the nodes ③–⑥ $V_{swing,\max}$ can be expressed as

$$V_{swing,\max} = \tfrac{1}{2}(V_{DD} - V_{DS,\text{on}} - 2V_T) \qquad (14)$$

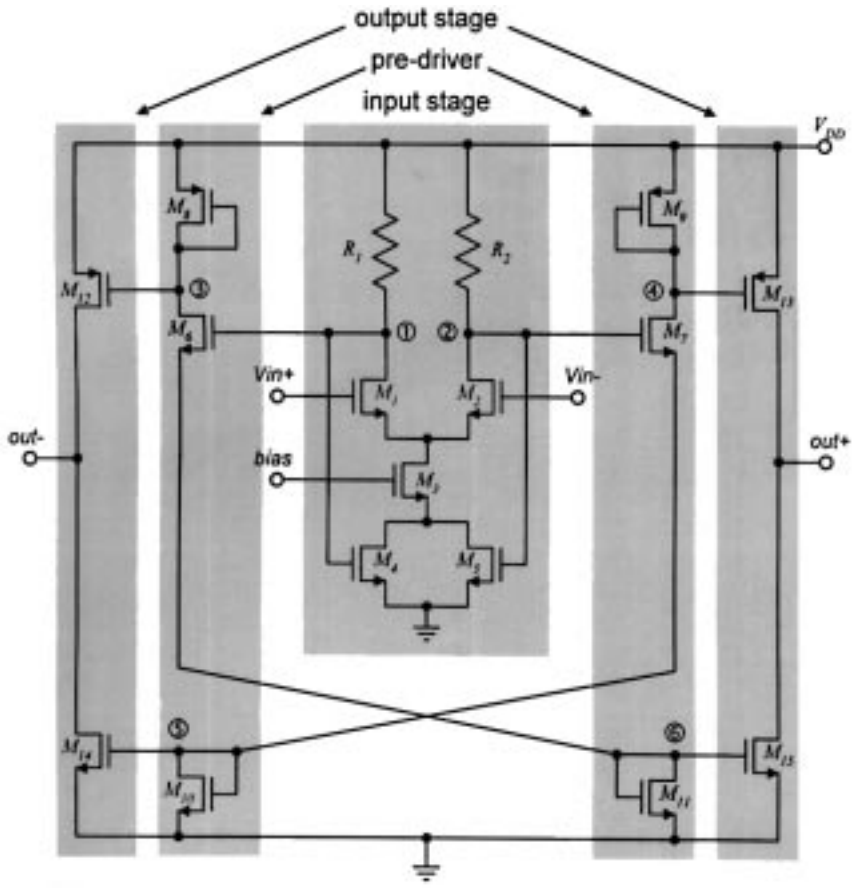


Fig. 9. The circuit diagram of the proposed OTA buffer.

where $V_{DS,\,\mathrm{on}}$ is the minimum saturation drain-to-source voltage of the transistor M_6 (M_7). In this design, given $V_{DS,\,\mathrm{on}} = 0.2$ V, $V_T = 0.7$ V, and $V_{DD} = 3$ V, $V_{swing,\,\mathrm{max}}$ is 0.7 V. The simulated gain and bandwidth of the buffer with 50-Ω loads are -1 dB and 180 MHz, respectively. The dc current is 6 mA.

C. Mixer Design

The multiplier in Fig. 3 is used as a mixer-core which is directly connected to the OTA buffer to form a complete mixer. An intuitive operational principle of the mixer-core is given as follows. Assume the v_1 port in Fig. 3 is supplied with a large enough LO signal to drive the transistors ON and OFF. When LO is at high voltage, the transistors M_{a1} and M_{a3} are ON, whereas the transistors M_{a2} and M_{a4} are OFF. Thus the nodes ① and ③ are at low voltage that disable the transistors M_{c1} and M_{c3}. In this case, the RF signal v_2 can be transmitted to the output through the transistors M_{b2}, M_{b4}, M_{c2}, and M_{c4}, and the output is out-phase. When LO is at low voltage, the transistors M_{a2} and M_{a4} are ON, whereas the transistors M_{a1} and M_{a3} are OFF. Thus the nodes ② and ④ are at low voltage that disable the transistors M_{c2} and M_{c4}. In this case, the RF signal v_2 can be transmitted to the output through the transistors M_{b1}, M_{b3}, M_{c1}, and M_{c3}, and the output is in-phase. Thus the RF signal is switched by the LO signal.

For the mixer-core of an RF downconversion mixer, the element values in Section II-C are not the optimum design.

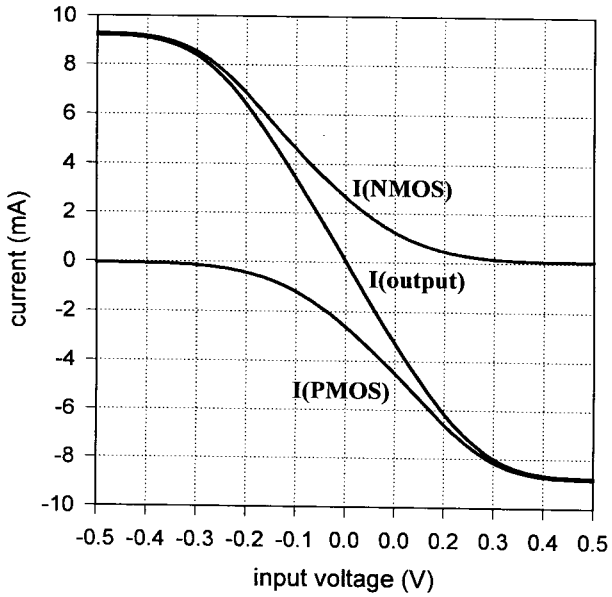


Fig. 10. The simulated currents flow through both PMOS and NMOS transistors of the output stage and the combined output current on a 50-Ω load as a function of input voltage.

Redesigning of the element values is required to meet the requirements given in Section III-A.

The voltage conversion gain CG_v of the mixer can be derived from (7) and rewritten in terms of small-signal pa-

rameters. The result is

$$CG_v = \left(-4\sqrt{2}R_cK_cR_b^2g_{ma}g_{mb}\right)V_{\mathrm{LO,rms}}A_{buffer} \quad (15)$$

where g_{ma} and g_{mb} are the transconductances of the transistors M_a and M_b, respectively, $V_{\mathrm{LO,rms}}$ is the LO amplitude expressed in V_{rms}, and A_{buffer} is the voltage gain of the buffer.

The input bandwidth $f_{\mathrm{in,3\,dB}}$ of the mixer is determined by the RC time constant at the nodes ①–④ in Fig. 3, which is given by

$$f_{\mathrm{in,3\,dB}} = \frac{1}{2\pi R_bC_{tot}} \quad (16)$$

where C_{tot} is the total capacitance on the nodes, which can be expressed as

$$C_{tot} = C_{Da} + C_{Db} + C_{Gc} + C_{res} \quad (17)$$

where C_{Da} and C_{Db} are the drain terminal capacitances of transistors M_a and M_b, respectively, C_{Gc} is the gate terminal capacitance of transistor M_c, and C_{res} is the parasitic capacitance of resistor R_b.

The noise factor F of the mixer can be derived based on the following assumptions. 1) Under the large LO signal, the average transconductances of the transistors are equal to the quiescent transconductances. 2) The image-band noise power is equal to the RF-band noise power. Both of them are transferred to the IF frequency band completely. 3) Only thermal noise is considered. 4) The noise contributed by the buffer stage is ignored. The derived F is given as (18), shown at the bottom of the page, where g_{mc} is the transconductance of the transistor M_c, and R_{in} is the source resistance 50 Ω. In the numerator of (18), the four terms represent the noise contributed by the transistors M_a and M_b, the transistor M_c, the resistor R_b, and the resistor R_c. Hand calculation of (18) shows that the most noisy sources are the transistors M_a and M_b. Their contribution is about 80% of the total noise.

The tradeoffs among the element values in the mixer-core design can be observed from (15)–(18). As in (15) and (16), the resistance R_b affects both CG_v and $f_{\mathrm{in,3\,dB}}$. Thus, it is an important parameter in the mixer design. Since R_b is a dominant parameter, the design of the element values can be started from the determination of R_b to achieve $f_{\mathrm{in,3\,dB}}$. In fact, the large parasitic capacitance associated with the resistor leaves very few choices of R_b for the gigahertz range operation. The R_b value of a few hundred ohms is reasonable. While R_b is set, the parasitic capacitance C_{res} can be determined from the dimension of R_b. At the same time, the upper limit of C_{tot} is also set by the required $f_{\mathrm{in,3\,dB}}$ from (16). Substituting the obtained C_{res} and C_{tot} into (17), the maximum terminal capacitances of the transistors can be determined, which implies the channel widths of the transistors are limited.

Since R_b is designed and CG_v, $V_{\mathrm{LO,rms}}$, and A_{buffer} are given, the unknown parameters R_c, K_c, g_{ma}, and g_{mb} in (15) can be determined. Since the channel widths of the transistors are set, g_{ma} and g_{mb} can be obtained by giving proper channel length and dc bias. Then the value of R_c and K_c can be determined from (15). With all the device parameters determined, the noise factor can be calculated from (18). If the resultant F is not low enough, g_{ma} and g_{mb} should be increased. This can be achieved by increasing the bias currents or decreasing the channel lengths of M_a and M_b. However, increasing the bias current increases the power consumption, whereas decreasing the channel length increases the mismatch errors that degrade the linearity. Thus, the tradeoffs among noise factor, power consumption, and linearity performance should be made. If the result is still not satisfactory after using the above two design methods, the design process should be resumed with another value of R_b.

TABLE III
THE ELEMENT VALUES OF THE PROPOSED MIXER

MIXER-CORE		BUFFER	
Parameter	Value	Parameter	Value
$W/L\,(M_a)$	20/0.5	$W/L\,(M_1,M_2)$	80/2
$W/L\,(M_b)$	40/0.5	$W/L\,(M_3)$	200/1
$W/L\,(M_c)$	10/0.5	$W/L\,(M_4,M_5)$	50/1
R_b	500Ω	$W/L\,(M_6,M_7)$	40/0.6
R_c	500Ω	$W/L\,(M_8,M_9)$	90/0.6
		$W/L\,(M_{10},M_{11})$	34/0.6
		$W/L\,(M_{12},M_{13})$	900/0.6
		$W/L\,(M_{14},M_{15})$	340/0.6
		R_1,R_2	1kΩ

In this design, the nominal supply voltage is 3 V. This value of supply voltage is required for the buffer operation. If the mixer is to be on-chip connected to other circuits, the buffer is not required and the supply voltage can be lower. The element values of the mixer-core and the buffer are listed in Table III. The input terminals of the mixer-core v_1 and v_2 are served as LO port and RF port, respectively. Both the dc bias of RF and LO ports are 1.5 V. The width of the resistor R_b is 4 μm, which results in 0.06 pF C_{res}. The total capacitance C_{tot} is 0.15 pF; thus, the input bandwidth $f_{\mathrm{in,3\,dB}}$ is 2.1 GHz. The simulated CG_v is 0.89 (−1 dB) while the LO power is 2 dBm (0.283 V_{rms}). The noise figure calculated using (18) is 23.8 dB. The dc current of the mixer-core is 15 mA. This value is designed after the tradeoff with both noise figure and linearity.

The dc current could be decreased if the required input bandwidth is not so high. With the bandwidth requirement decreased to 1 GHz, the designed value of C_{tot} is increased. This means the transistor dimensions can be increased; thus, the same transconductances can be obtained with lower dc bias currents. The simulations have shown that, with the device dimensions and resistor values of the mixer-core changed to $(W/L)_a = 40/0.5$, $(W/L)_b = 80/0.5$, $(W/L)_c = 5/0.5$, $R_b = 670\,\Omega$, $R_c = 500\,\Omega$, and dc bias voltage = 1.05 V, the mixer-core can reach the same performance as the previous design while decreasing the dc current to 9 mA.

$$F = \frac{\frac{16}{3}(g_{ma}+g_{mb})(R_bR_cg_{mc})^2 + \frac{16}{3}g_{mc}R_c^2 + 8R_bg_{mc}^2R_c^2 + 4R_c}{R_{\mathrm{in}}CG_v^2} + 1 \quad (18)$$

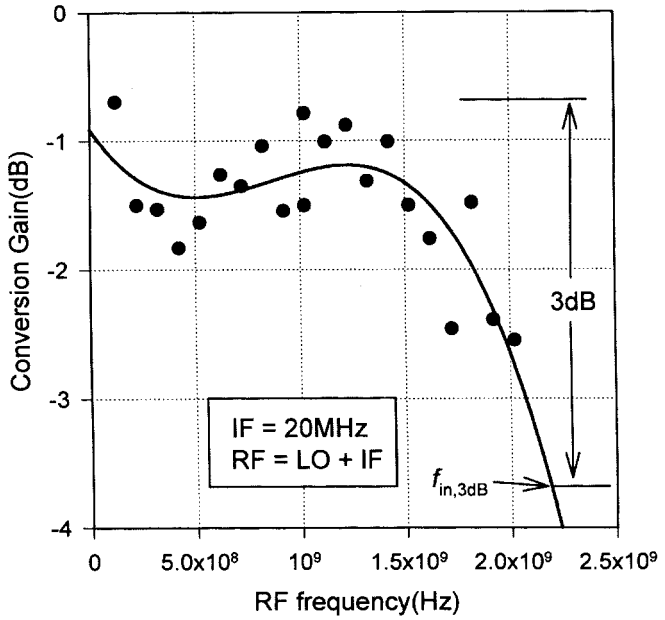


Fig. 11. The measured input bandwidth of the fabricated mixer.

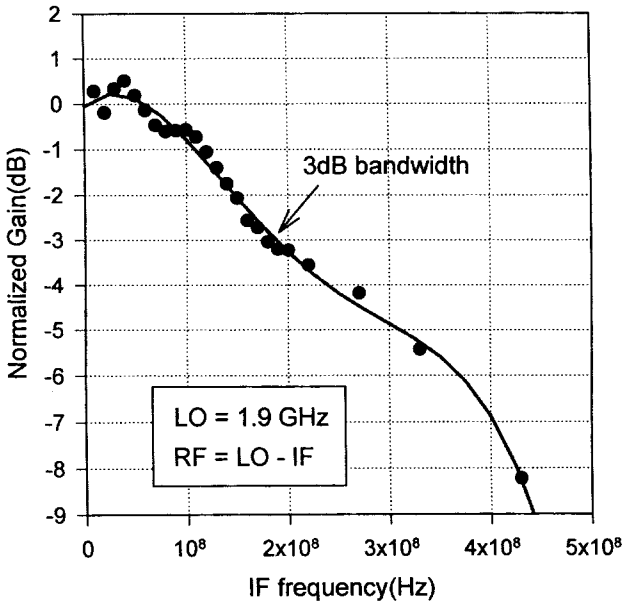


Fig. 12. The measured output bandwidth of the fabricated mixer.

D. Experimental Results

The experimental chip of the proposed mixer is fabricated by 0.5-μm single-poly-double-metal N-well CMOS technology. The active chip area is 590×220 μm^2. In order to perform the high-frequency measurements, the experimental chip is mounted on the PCB directly, which effectively reduces the I/O parasitics. In the experimental board, both RF and LO ports are terminated with matching resistors; thus, the port reflections can be lower than -10 dB in the measured frequency band. The differential signals in the measurements are generated through three passive single/differential converters connected to the RF, LO, and IF ports. The bandwidth of the converters is 2 GHz. The accuracy of the measured signal power level is about ± 0.5 dB.

The measured power conversion gain versus RF signal frequency with IF fixed to 20 MHz is shown in Fig. 11. In the measurement, the high frequency is limited by the bandwidth of the single/differential converters. However, the extrapolated input bandwidth shown in Fig. 11 is 2.2 GHz which is close to the calculated value. The measured output bandwidth of the fabricated mixer with LO fixed to 1.9 GHz is shown in Fig. 12, where the measured -3-dB bandwidth is 180 MHz, which is consistent with the simulated bandwidth of the output buffer. The intrinsic output bandwidth of the mixer-core is much higher than this value. The simulations have shown that the internal bandwidth at the output nodes of the mixer-core is up to 620 MHz. With proper changes of the component values, this value can be designed to be higher than 1 GHz. Thus an upconversion mixer can also be implemented by the proposed multiplier structure.

Since the most popular frequency bands of the modern wireless systems are 900 MHz and 1.9 GHz, the LO frequencies are set to the above two frequencies in the following measurements. The measured NF versus IF frequency of the fabricated mixer is shown in Fig. 13, where the minimum IF

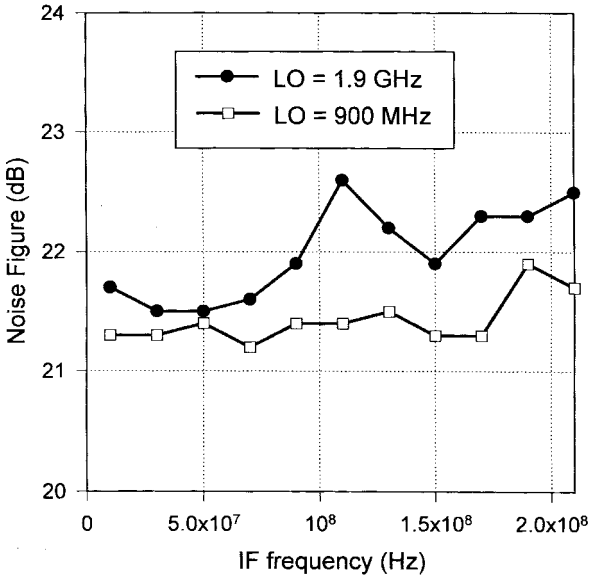
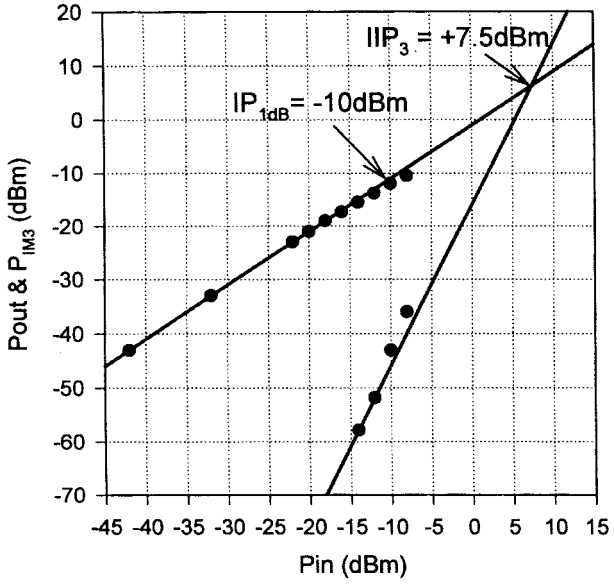


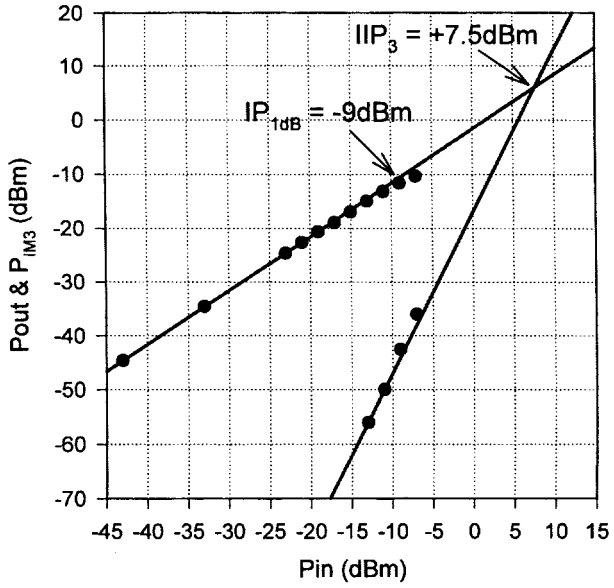
Fig. 13. The measured NF versus IF frequency of the fabricated mixer.

frequency in the measurement is limited to 10 MHz by the instrument. As seen in Fig. 13, the measured NF is about 22 ± 1 dB in the entire IF frequency band. This value is slightly lower than the calculated value (23.8 dB) because the average transconductances of the transistors under the large LO signal swing are higher than the quiescent transconductances used in the calculation.

The measured third-order input intercept point IIP_3 and the measured input 1 dB compression point $IP_{1\,dB}$ of the fabricated mixer with LO $=$ 900 MHz and 1.9 GHz are shown in Fig. 14(a) and (b), respectively. The two-tone frequencies in the measurement with LO $=$ 900 MHz (1.9 GHz) are 930 MHz (1.93 GHz) and 940 MHz (1.94 GHz). As seen in Fig. 14(a), the measured IIP_3 and $IP_{1\,dB}$ are $+7.5$ dBm and -10 dBm, respectively. In Fig. 14(b), IIP_3 and $IP_{1\,dB}$ are $+7.5$



(a)



(b)

Fig. 14. The measured, IIP_3 and IP_{1dB} of the fabricated mixer under (a) 900-MHz LO and (b) 1.9-GHz LO.

dBm and −9 dBm, respectively. It has been found that the value of IIP_3 measured at one of the differential output ports of the mixer is the same as that measured at the differential output ports of the mixer. This means that the intermodulation distortion of the mixer is mainly contributed by the mixer-core and the output buffer only contributes negligible distortion. The high-linearity characteristic of the buffer is thus proved.

The measured LO-to-RF isolation versus LO frequency is shown in Fig. 15, where the isolation degrades from −71 to −27 dB as the frequency increases from 100 MHz to 1.9 GHz. This means that the coupling between RF and LO ports is capacitive. The capacitive coupling is mainly caused by the asymmetry and crossover of the interconnection lines in the circuit layout. The measured characteristics of the fabricated downconversion mixer are summarized in Table IV.

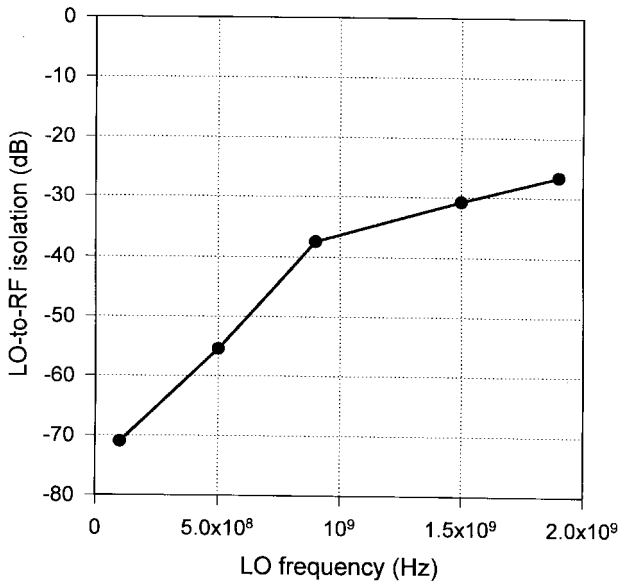


Fig. 15. The measured LO-to-RF isolation of the fabricated downconversion mixer.

TABLE IV
THE MEASURED CHARACTERISTICS OF THE MIXER

Parameter	Value
Technology	0.5 μm
VDD	3 V
LO power	2 dBm
CG	-1 dB
RF bandwidth	2.2 GHz
IF bandwidth	180 MHz
NF	22 dB
IIP_3	+7.5 dBm
IP_{1dB}	-9 dBm
Isolation	> 27dB@1.9GHz
DC current	21 mA

IV. CONCLUSION

A new CMOS analog multiplier based on the square-law characteristics of MOS devices has been designed and analyzed. The multiplier can be operated at very low supply voltage while sustaining a high linearity characteristic. Moreover, it has the advantageous characteristics of symmetric structure, high-frequency response, and small chip area. Thus, the proposed CMOS analog multiplier is very feasible in various applications. By using the proposed analog multiplier structure, an RF downconversion mixer has been successfully designed and fabricated. The performance of the experimental chip has been verified through the measurement. It has also been shown from the experimental results that the fabricated RF mixer can meet the requirements of 900 MHz and 1.9 GHz wireless communication systems. Further research will be conducted to integrate the designed RF mixer with an RF bandpass amplifier [32] to form a high-integration CMOS receiver.

ACKNOWLEDGMENT

The authors would like to thank the reviewers for their valuable comments and suggestions. They also wish to thank

the Chip Implementation Center (CIC) of the National Science Council (NSC), Taiwan, ROC, for giving them the chance to implement the chip.

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