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MULTIPLE-CELL SQUARE-TYPE LAYOUT DESIGN FOR OUTPUT TRANSISTORS IN SUBMICRON CMOS TECHNOLOGY TO SAVE SILICON AREA

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Abstract—A new multiple-cell square-type layout design is proposed to realize the large-dimension output transistors for submicron low-voltage CMOS ICs. By using this layout design, the layout area of CMOS output buffers can be effectively reduced 30–40% with respect to the traditional finger-type layout. The drain-to-bulk parasitic capacitance of the output transistors is also reduced 40% by this square-type layout. Experimental results in a 0.6 μm CMOS process have shown that the maximum driving (sinking) capability per unit layout area of a CMOS output buffer realized by the proposed multiple-cell square-type layout is improved 54% (34%) more than that by the traditional finger-type layout. The human-body-model (machine-model) ESD robustness per unit layout area of the CMOS output buffer realized by the proposed multiple-cell square-type layout is increased 25.2% (17.3%) as comparing to that by the traditional finger-type layout. © 1998 Published by Elsevier Science Ltd. All rights reserved

1. INTRODUCTION

In submicron low-voltage CMOS technology, VDD had been scaled down to save power consumption and to provide better device reliability. To offer enough output driving/sinking currents as well as to provide stronger ESD reliability, the W/L ratios of output transistors are often enlarged up to several hundreds. But in the high-integration applications, especially in the high-pin-count and pad-limited CMOS VLSI, the layout area available for each output pad with output buffer including latchup guard rings is seriously limited. So, an area-efficient output buffer with high driving capability and high ESD robustness is strongly required in submicron CMOS technology.

In 1989, *Baker* proposed a *waffle*-type layout to enhance ESD hardness of NMOS output transistor[1]. The *waffle*-type layout had been shown to offer better ESD protection capability than that in the finger-type layout within the same layout area. In 1992, *Vemuru* made a comparison between the finger-type and *waffle*-type layout[2]. He found that *waffle*-type layout contributes about 10% area reduction to that of finger-type, as well as the *waffle*-type layout produces lower gate resistance suitable for wide-band or low-noise applications. The schematic *waffle*-type layout style is shown in Fig. 1, where the drain and the source of an NMOS have the same layout spacing from the contact to the poly gate.

Recently, some efforts have contributed to investigate the relations between the layout parameters and ESD hardness of submicron CMOS devices. It had been found that the spacing from the drain contact to the edge of gate oxide is an important layout parameter to affect ESD reliability of CMOS devices[3–5]. A larger spacing from the drain contact to the gate-oxide edge leads to a higher ESD robustness. This minimum spacing was found to be about 5–6 μm in the submicron CMOS technologies to sustain better ESD protection without much increasing the layout area. But in the *waffle*-type layout, the spacings from both the source contact and the drain contact to the edge of gate oxide are required to be equal. In the traditional finger-type layout, the spacing from the drain contact to the gate-oxide edge can be different to the spacing from the source contact to the gate-oxide edge. Due to this spacing constraint on the drain contact to its gate-oxide edge for ESD-reliability consideration, the *waffle*-type layout becomes to occupy more layout area than the traditional finger-type layout under the same W/L ratio.

In this paper, a new layout design is proposed to realize CMOS output transistors in a smaller layout

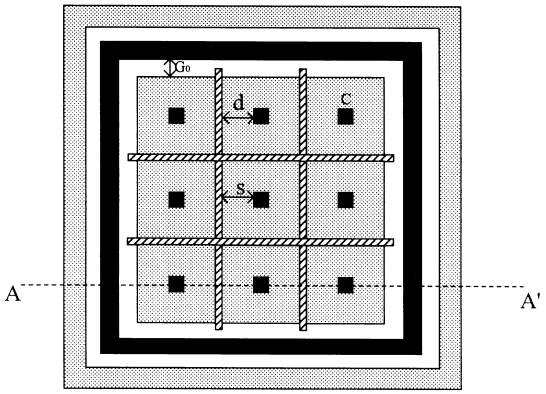


Fig. 1. The schematic diagram of the waffle-type layout

area but with a higher driving capability and better ESD robustness[6].

2. TRADITIONAL FINGER-TYPE LAYOUT

The traditional finger-type layout for an NMOS device is shown in Fig. 2. Its cross-sectional view along the line A–A′ in Fig. 2 is shown in Fig. 3, which is demonstrated in a p-substrate CMOS process. In Fig. 2, a large-dimension NMOS device is separated as four parallel small-dimension NMOS devices. The spacing from the drain contact to the poly-gate edge is marked as "*d*". The spacing from the source contact to the poly-gate edge is marked as "*S*". For better ESD robustness of CMOS output buffer in submicron CMOS technologies, this "*d*" spacing is found to be about 5–6 μm[3–5]. But, the "*S*" spacing has no important effect on the ESD reliability of CMOS output buffer. This "*S*" spacing is often used as 1 μm in the practical layout. Outside the source region, there are two

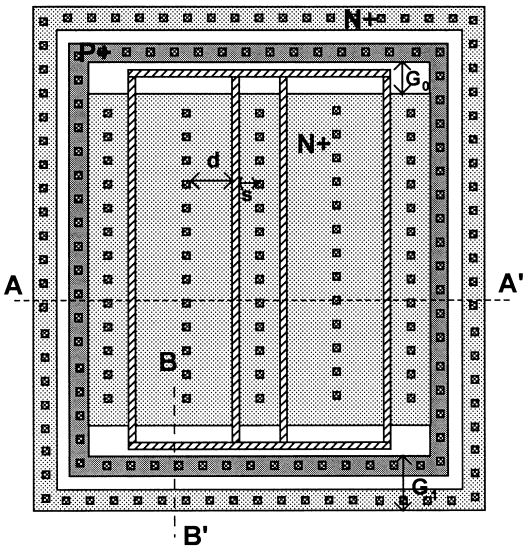


Fig. 2. A schematic diagram of the traditional finger-type layout

latchup guard rings surrounding the whole NMOS device. One is a P+ diffusion connected to ground (GND) to offer the substrate bias. The other is an N+ diffusion connected to VDD as a dummy collector to prevent CMOS latchup.

But in the traditional finger-type layout, there is an important spacing denoted as "G_0" in Fig. 2, which often degrades the ESD robustness of the CMOS output buffer. To explain this "G_0" spacing, a schematic cross-sectional view along the line B–B′ is shown in Fig. 4. In Fig. 4, there exists a parasitic diode D1 between the P+ diffusion (connected to GND) and the N+ diffusion of the drain. The spacing from the edge of P+ diffusion to the edge of drain N+ diffusion is marked as "G_0". If this spacing is smaller than that of the drain contact to its source contact, the diode D1 will be first broken down due to the ESD peak-discharging effect before the NMOS drain is broken down[7]. Thus, with the consideration of ESD reliability, this G_0 spacing has better to be greater than the spacing from the drain contact to the source contact. But with a wider spacing G_0, the total layout area will be increased. A practical layout example of a CMOS output buffer realized by the finger-type layout in a 0.6 μm CMOS process is shown in Fig. 5, where the device dimension (W/L) of the output NMOS (also PMOS) is 500/1.0 (μm/μm) and the layout area including the latchup guard rings for the output NMOS (also PMOS) is 117.4×82 μm^2.

The total layout area of an NMOS transistor in the finger-type layout including two latchup guard rings can be calculated by the following equations. In the TSMC (Taiwan semiconductor manufacturing company) 0.6 μm SPDM (single–poly–double-metal) design rules, the channel width "w" of each finger in the finger-type layout is specified to be between 25 to 50 μm. The total layout area of an finger-type NMOS transistor with double guard rings is:

$$\mathbf{A}_{\text{finger}} = [(d + L + s + c) \cdot \frac{W}{w} + 2G_1] \cdot [w + 2(G_0 + G_1)] \ (\mu\text{m}^2). \quad (1)$$

where L is the channel length (μm); W is the total channel width (μm); w is the channel width of each poly-gate finger (μm); d is the spacing from the drain contact to poly-gate edge (μm); s is the spacing from the source contact to poly-gate edge (μm); c is the width of a contact (μm); G_1 is the spacing of the double guard rings (μm); and G_0 is the spacing from the drain N+ diffusion to the P+ diffusion guard ring (μm).

The total number of poly-gate fingers in the whole NMOS layout is $W/w = N$, where N must be an integer. The total layout area of the drain N+ diffusion can be obtained as

$$AD = N \cdot w \cdot (d + c/2) = W \cdot (d + c/2) \ (\mu\text{m}^2). \quad (2)$$

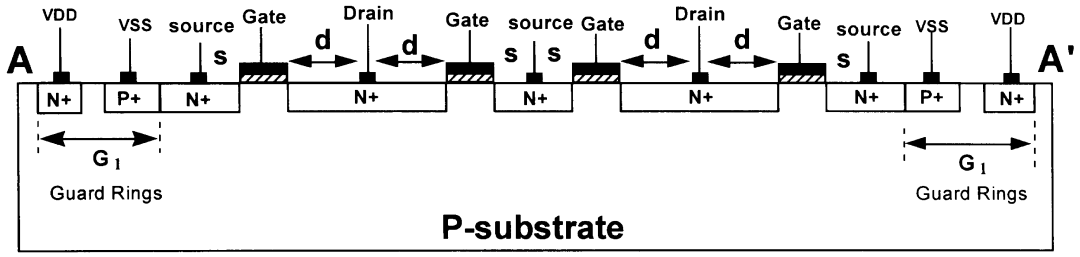


Fig. 3. The cross-sectional view of the NMOS device along the line A–A′ in Fig. 2

The total perimeter of the drain region (N+ diffusion) in the whole NMOS layout is

$$PD = W + 2\frac{W}{w} \cdot (d + c/2)\ (\mu\text{m}). \tag{3}$$

The different width (w) of poly-gate fingers will result in a different layout area of a finger-type NMOS. The minimum layout area of the finger-type NMOS can be found by the following equations.

$$\partial A/\partial N = -2G_1 W/N^2 + 2(d + L + s + c) \cdot (G_1 + G_0); \tag{4}$$

$$\frac{\partial A^2}{\partial^2 N} = 4G_1 W/N^3. \tag{5}$$

When $\partial A^2/\partial^2 N \geq 0$, the total layout area has its minimum value. The N to meet this minimum value is

$$N = \sqrt{G_1 \cdot W/(G_0 + G_1) \cdot (d + L + s + c)}. \tag{6}$$

N must be an integer, and the value of W/N is between 25–50 μm. Putting the N into Equation (1), the minimum layout area of a finger-type NMOS transistor can be calculated and used as the reference of comparison in the next section.

3. MULTIPLE-CELL SQUARE-TYPE LAYOUT

3.1. *Square-type layout design*

To reduce layout area for cost saving and to overcome the parasitic diode D1 in the traditional finger-type layout of CMOS output transistors, a multiple-cell square-type layout design is proposed. The schematic multiple-cell square-type layout of an output NMOS is shown in Fig. 6. The schematic cross-sectional view along the line A–A′ in Fig. 6 is

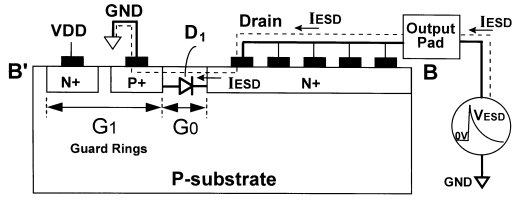


Fig. 4. The cross-sectional view along the line B–B′ in Fig. 2 with the ESD peak-discharging effect on the fingers end of the finger-type layout

also the same as that shown in Fig. 3. This multiple-cell square-type layout can be implemented in any CMOS or BiCMOS technologies. It can be also used to implement PMOS devices. In Fig. 6, there are four small-dimension square cells to form a large-dimension NMOS device. Each small-dimension square cell is identical to each other. The black square region in the center of a square cell is the drain contact of the NMOS device. The poly gate in each square cell is also drawn in a square ring. The N+ diffusion of the source region is also drawn in a square shape and surrounds the gate and the drain region. The contacts at the source region are placed in a square-shape arrangement. Outside the NMOS device, there is a P+ diffusion connected to ground to offer the substrate bias. This P+ diffusion surrounds the whole NMOS device. Besides, an N+ diffusion surrounding this P+ diffusion and connected to VDD works as latchup guard ring. All the layout elements in a square cell, including the contacts, have to be placed as symmetrical as possible to ensure uniform ESD current flow in the NMOS device so as to increase its ESD reliability. An NMOS device with a larger device dimension can be assembled by a plurality of the square cells.

A typical CMOS output buffer realized by the proposed square-type layout design in a 0.6 μm CMOS process is shown in Fig. 7, where the large-dimension output NMOS (also PMOS) is assembled by 15 square cells. The total device dimension (W/L) of the output NMOS (also PMOS) in Fig. 7 is 600/1.0 (μm/μm) and the layout area including the latchup guard rings for the output NMOS (also PMOS) is only $119.4 \times 87.7\ \mu\text{m}^2$. By using this proposed multiple-cell square-type layout design, there is no "G_0" spacing in the square-type layout. The layout area due to the wider "G_0" spacing in the traditional finger-type layout can be saved. Moreover, there is no parasitic diode D1 to directly close to the edge of the drain region in the multiple-cell square-type layout, so the ESD robustness of output devices is not degraded by the ESD peak-discharging effect in the finger-type layout as shown in Fig. 4.

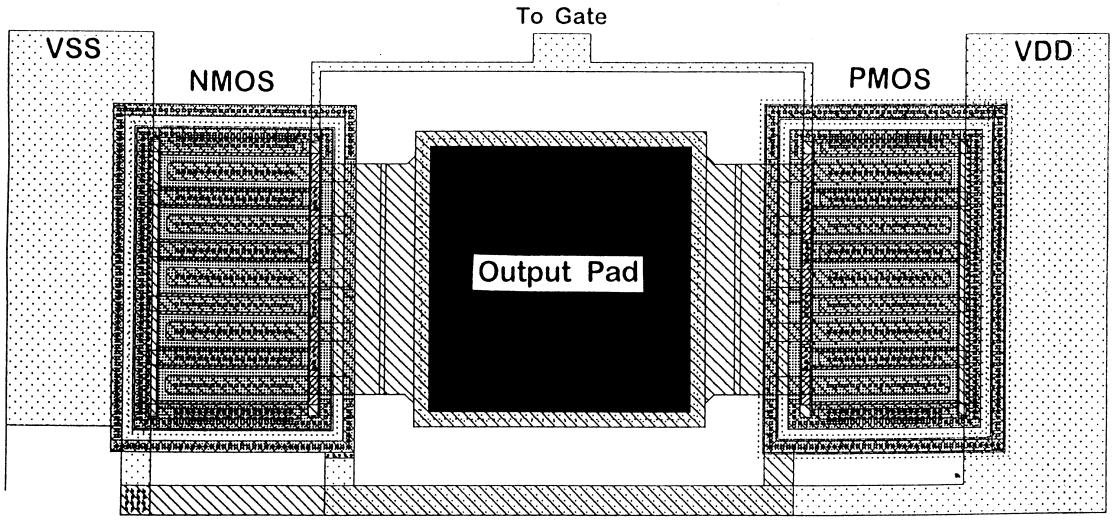


Fig. 5. A practical layout example of a CMOS output buffer realized by the traditional finger-type layout in a 0.6 μm CMOS process

3.2. *Calculation of the square-type layout area*

In the square-type layout, the total layout area of the output NMOS transistor can be calculated as:

$$\mathbf{A}_{\text{square}} = [(\frac{w}{4} + 2L + 2S) \cdot M + 2G_1] \cdot [(\frac{w}{4} + 2L + 2S) \cdot N + 2G_1] \ (\mu\text{m}^2), \quad (7)$$

where L is the channel length (μm); W is the total channel width of the NMOS device (μm); $w = 4(2d + c)$ is the channel width of a single square cell (μm); d is the spacing from the drain contact to the poly-gate edge (μm); S is the spacing from the center of source contact to the poly-gate edge (μm); c is the width of the square drain contact in the square cell (μm); G_1 is the total spacing of double guard rings (μm); M is the number of square cells in the column direction of the whole NMOS layout; and N is the number of square cells in the row direction of the whole NMOS layout.

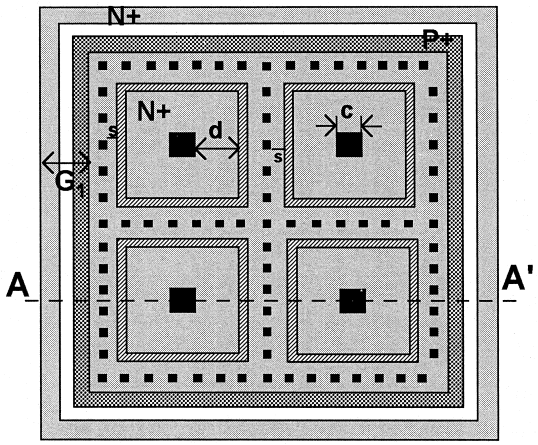


Fig. 6. The schematic diagram of the proposed multiple-cell square-type layout

The total number of the square cells in a whole NMOS layout is $M \times N$. The total diffusion area of the drain region (N+ diffusion) is

$$AD_{\text{square}} = \frac{wW}{16} \ (\mu\text{m}^2). \quad (8)$$

The total diffusion perimeter of the drain region (N+ diffusion) is

$$PD_{\text{square}} = W \ (\mu\text{m}). \quad (9)$$

3.3. *Comparison between the square-type and finger-type layouts*

To verify the layout efficiency, comparison on the total layout area of an NMOS transistor between the traditional finger-type layout and the multiple-cell square-type layout under the same spacing "d" of 5 μm is shown in Fig. 8(a). The total layout area includes the spacing "G_1" of 10.3 μm (the spacing of double latchup guard rings) in both the traditional finger-type layout and the square-type layout. In the square-type layout, the edge "C" of drain contact is 2 μm. In Fig. 8(a), the area of the square-type layout with a larger device channel width is significantly reduced as compared to that of the finger-type layout. For example, the total layout area of an NMOS with a device dimension (W/L) of 432/0.8 (μm/μm) in the finger-type layout is 6982 μm^2, but that in the square-type layout is only 4789 μm^2. This shows the excellent area-saving efficiency of the proposed multiple-cell square-type layout about 30% reduction, as comparing to the finger-type layout. When the spacing of "d" is more larger, the output buffer transistor realized by the square-type layout can save much more area than that realized by the finger-type layout. Figure 8(b) shows the relations between the device channel width and the percentage of layout area ratio

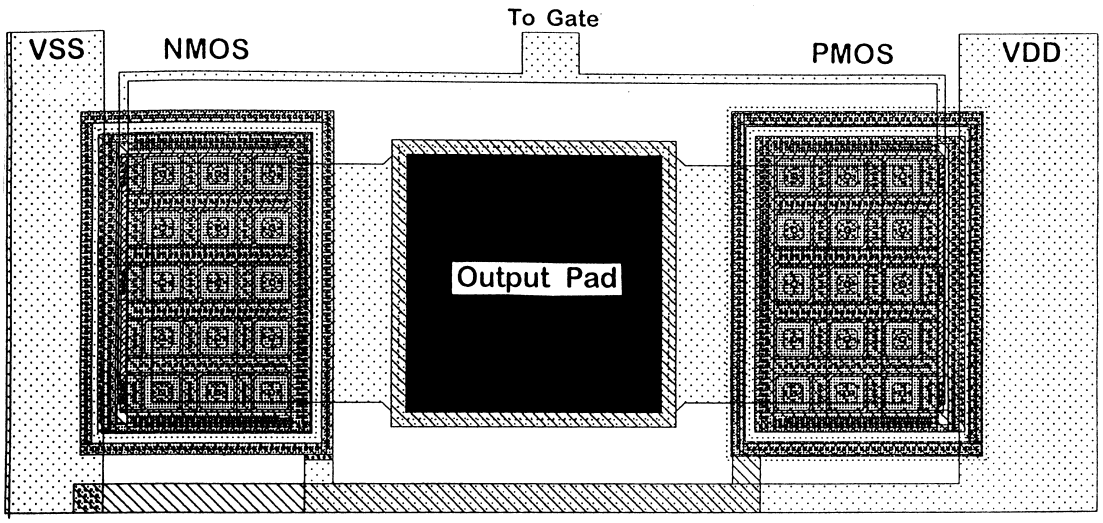


Fig. 7. A practical layout example of a CMOS output buffer realized by the multiple-cell square-type layout in a 0.6 μm CMOS process

(square-type to finger-type) with different layout parameters of "*d*". In Fig. 8(b), the square-type device has a much smaller layout area as compared to the finger-type device while the spacing "*d*" or the channel width is increased. This comparison obviously confirms the excellent advantage of the reduction on the layout area in this proposed multiple-cell square-type layout design.

Moreover, the drain-to-bulk parasitic capacitance at the output node is also reduced by this multiple-cell square-type layout. Figure 9(a) shows a comparison of the total drain capacitance between the finger-type and the square-type layout under the same spacing d of 5 μm. The drain parasitic capacitance in the square-type layout is only about 65% of that in the finger-type layout with the same device dimension. The ratio (square-type to finger-type) of the drain capacitance under different spacing "*d*" is shown in Fig. 9(b). The capacitance ratio is independent to the device channel width, but dependent to the spacing "*d*". It is clearly shown that the drain capacitance of an NMOS device realized by the square-type layout can be significantly reduced about 30–45% as compared to that by the finger-type layout. With a lower drain capacitance, this square-type layout is more suitable for CMOS output buffer in high-speed or high-frequency applications.

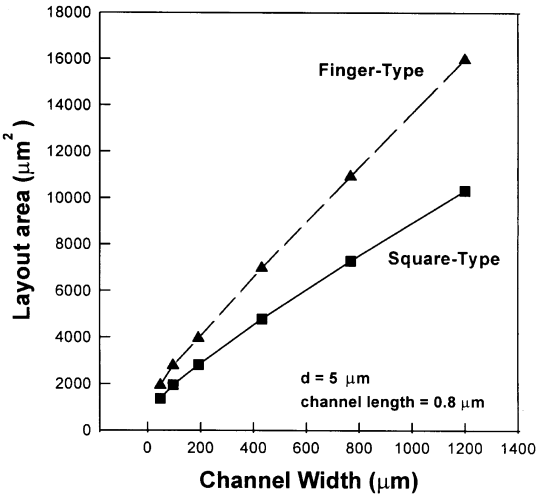
4. EXPERIMENTAL RESULTS

One set of output buffers with different W/L ratios in the finger-type layout and the square-type layout has been designed and fabricated in a 0.6 μm CMOS process. A microphotograph of the fabricated CMOS output buffer in the multiple-cell square-type layout is shown in Fig. 10.

4.1. *Output driving/sinking capability*

The driving/sinking capability of a CMOS output buffer can be monitored by measuring the I–V curves of the output NMOS and PMOS. The drain current of the output NMOS (PMOS) is measured under the bias of $V_{ds} = 3$ V (-3 V) and $V_{gs} = 3$ V (-3 V) with its source grounded. The measured results of the sinking/driving current of the output NMOS and PMOS in the square-type and the finger-type layout are shown in Figs 11 and 12, respectively. Figure 11(a) shows the dependence of the drain current on the channel width of the output NMOS in both the finger-type and square-type layouts. Figure 11(b) shows the relation between the drain current and the layout area of the output NMOS in both the finger-type and square-type layouts. From Fig. 11, the maximum NMOS sinking current density per unit layout area is about 12.13 (9.04) $\mu A/\mu m^2$ for the output buffer in the square-type (finger-type) layout. The maximum sinking current per unit layout area of the output NMOS in the multiple-cell square-type layout is improved about 34.2% more than that in the traditional finger-type layout.

Figure 12(a) shows that the drain current of the square-type layout almost linearly increases while the channel width of the output PMOS is increased. The dependence of the drain current of the output PMOS in both the square-type and finger-type layouts on the total layout area is shown in Fig. 12(b). The maximum PMOS driving current per unit layout area is about 5 (3.24) $\mu A/\mu m^2$ for the output PMOS in the square-type (finger-type) layout. From the measured datas, the maximum driving capability per unit layout area of the output PMOS in the multiple-cell square-type layout is improved about 54.3% more than that in the traditional finger-type layout.



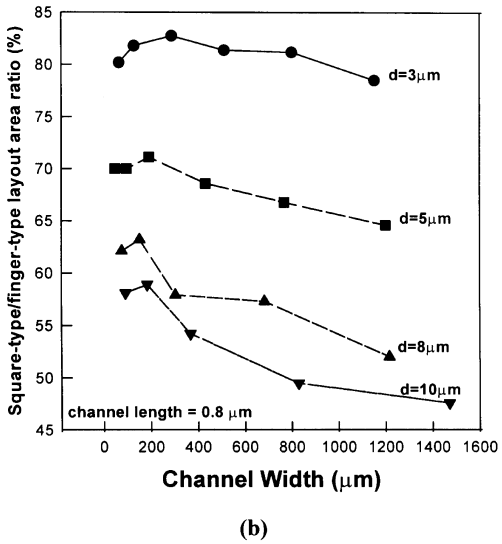


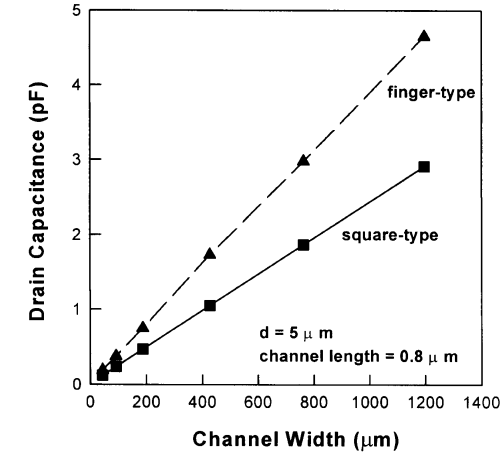
Fig. 8. (a) Comparison of layout area between the finger-type layout and the square-type layout with different channel widths, under the same spacing d of 5 μm. (b) The relations between the percentage of the square-to-finger layout area ratio and the device channel width with different layout parameters of d

4.2. *Output ESD robustness*

The human-body-model (HBM) and machine-model (MM) ESD testing results of a CMOS output buffer in the finger-type and square-type layouts are listed in Table 1. An output NMOS with a device dimension (W/L) of 640/0.8 (μm/μm) in the finger-type layout sustains the HBM (MM) ESD voltage of 2500 V (200 V) with a layout area of 135.6×58 μm^2. The output NMOS with a device dimension (W/L) of 564/0.8 (μm/μm) in the square-type layout sustains the HBM (MM) ESD voltage of 2000 V (150 V) with a layout area of only 79.6×62.5 μm^2. The ESD robustness per unit layout area of the square-type layout is about 0.397 (0.0298) V/μm^2 in the HBM (MM) ESD stress, but that of the finger-type layout is only 0.317 (0.0254) V/μm^2. Thus, the square-type layout provides an increase of 25.2 (17.3)% in the HBM (MM) ESD robustness per unit layout area, as comparing to the finger-type layout. This has verified that the multiple-cell square-type layout can enhance the uniform ESD current distribution among the multiple cells of the output transistor to effectively improve its ESD robustness with a smaller layout area.

4.3. *Discussion*

In[7], an alternative layout design with the multiple-cell octagon-type structure had been proposed to improve ESD robustness and driving capability



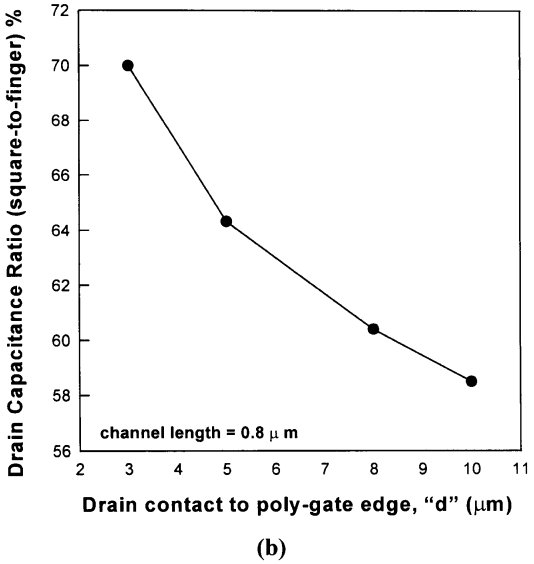


Fig. 9. (a) Comparison of the drain parasitic capacitance between the finger-type and the square-type layout with different device widths, under the same spacing d of 5 μm. (b) The relations between the percentage of square-to-finger drain capacitance and the spacing "d"

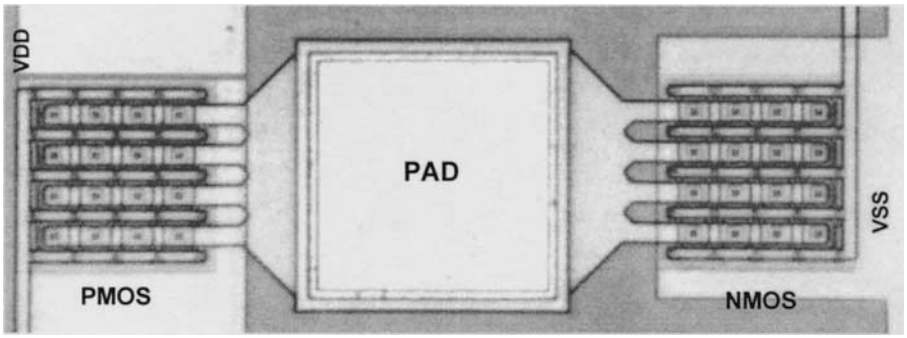


Fig. 10. A microphotograph of a CMOS output buffer realized by the multiple-cell square-type layout

of CMOS output buffers. The experimental results had shown that the output driving (sinking) current per unit layout area of the octagon-type output buffer is 47.7% (34.3%) more than that of the finger-type output buffer, and the HBM (MM) ESD robustness per unit layout area of the output buffer is 41.5% (84.6%) more than that of the finger-type output buffer[7]. With relative comparison to the

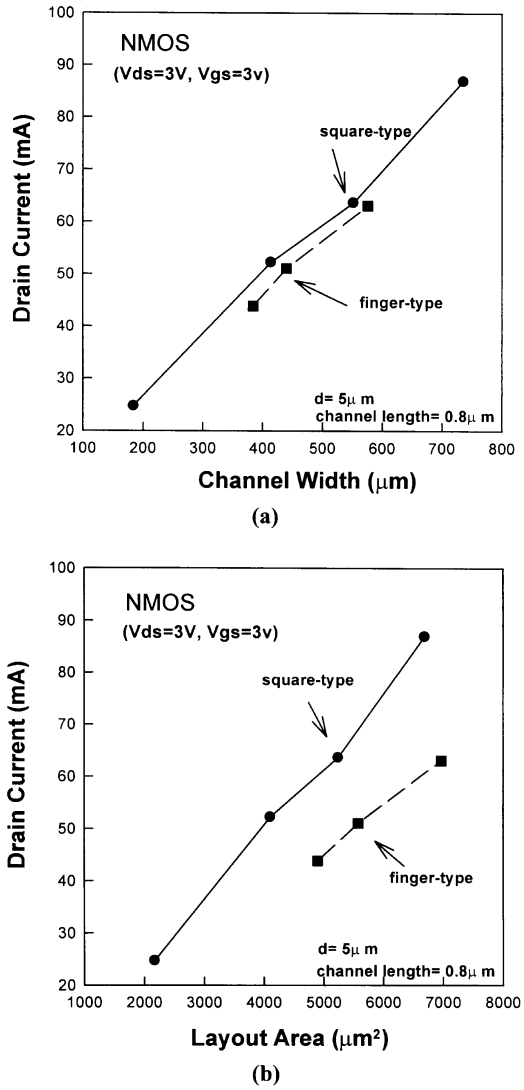


Fig. 11. Comparison of the maximum drain current vs (a) the channel width; (b) the total layout area; of the output NMOS in the square-type layout and the finger-type layout

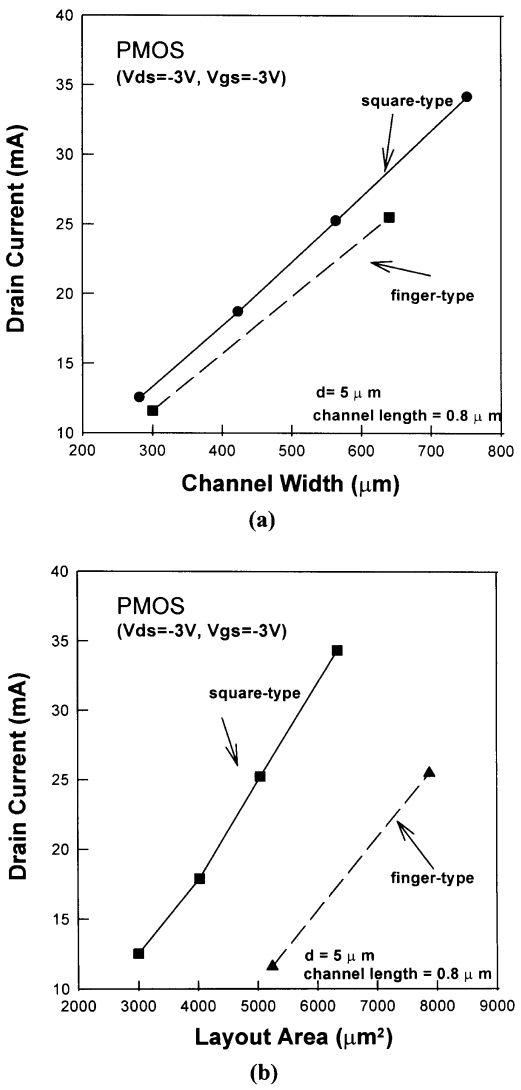


Fig. 12. Comparison of the maximum drain current vs (a) the channel width; (b) the total layout area; of the output PMOS in the square-type layout and the finger-type layout

Table 1.

Parameter (unit)			HBM		MM	
Layout style	W/L (μm/μm)	area (μm^2)	V	V/μm^2	V	V/μm^2
Finger type	640/0.8	135.6×58	2500	0.317	200	0.0254
Square type	560/0.8	79.6×62.5	2000	0.397	150	0.0298

finger-type layout, this square-type layout provides a somewhat higher driving capability than that of the octagon-type layout in per unit layout area. But, the octagon-type layout can sustain about 1.6 times (4.9 times) higher HBM (MM) ESD stress than the square-type layout in per unit layout area. Because there are many P+ islands (N+ islands) connected to VSS (VDD) among the multiple cells of the octagon-type output NMOS (PMOS) to uniformly provide the p-substrate (n-well) bias[7], the uniform turn-on behavior among the multiple cells of the output buffer is further enhanced by the octagon-type layout. Thus, the octagon-type layout performs a much better ESD robustness per unit layout area than the square-type layout, especially in the machine-model ESD events with the faster ESD transition. However, the P+ islands (N+ islands) in the octagon-type output NMOS (PMOS) occupy some extra layout area, and they need a CMOS process with three metal layers to realize the output buffers in such octagon-type layout structure. The octagon-type layout is also more complex and difficult to be drawn than the square-type layout. So, the square-type layout is generally more suitable for the consumer ICs to save silicon area, which are fabricated by the CMOS process with only two metal layers.

5. CONCLUSION

With theoretical calculation and experimental verification, a multiple-cell square-type layout design has been successfully used to realize the output transistors in submicron CMOS ICs with higher driving capability and better ESD robustness in per unit layout area. By applying this square-type layout to the CMOS output buffers, the total layout area of a high-pin-count and pad-limited chip can be significantly reduced. The drain-to-bulk parasitic capacitance at the output pad is also reduced by this square-type layout. This multiple-cell square-type layout design can be applied to realize the devices in both the output buffers and the input ESD protection circuits for submicron CMOS ICs to save silicon area in the high-density, high-speed, and high-reliability applications.

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