A New Simple and Reliable Method to Form a Textured Si Surface for the Fabrication of a Tunnel Oxide Film

Kow-Ming Chang, Chii-Horng Li, Bao-Sheng Sheih, Ji-Yi Yang, Shih-Wei Wang, and Ta-Hsun Yeh

***Abstract*—In this work, a textured Si surface was formed with a new simple and reliable method for tunnel oxide fabrication. First, a thin poly-Si layer (12 nm thick) was deposited on Si surface and a 30-nm thick dry oxide film was then grown in O_2 ambient. This oxide film was served as a sacrificial oxide. The poly-Si film and Si substrate were both oxidized during thermal oxidization. After stripping this sacrificial oxide, a textured Si surface was obtained. Tunnel oxide grown on this textured Si surface has an asymmetrical J–E characteristics, less interface states generation and better reliability (larger $Q_{\rm bd}$) as compared to those of normal oxide.**

***Index Terms*—Nonvolatile memory devices, textured Si surface.**

I. Introduction

REDUCING the programming voltages is important in the future for nonvolatile memory devices such as advanced EPROM's, EEPROM's, and flash EEPROM's. Growing a tunnel oxide film with a textured SiO_2/Si interface can meet the lower programming voltage requirement. Several methods have been reported to form the tunnel oxide with a textured SiO_2/Si interface, e.g., by etching the Si surface [1]–[3] or by thermal oxidation of a thin poly-Si film [4]–[6] on the Si substrate. However, there are many problems with the use of these methods. In the case of etching process, the controllability of etching is not easy [2]. Moreover, in the case of oxidizing a thin poly-Si film on the Si substrate, good electrical characteristics are difficult to obtain and they should be optimized by stopping the oxidation process just on the poly-Si/Si-substrate interface [6]. Moreover, the electrical behaviors of oxides in [6] is similar to polyoxides (oxide grown on poly-Si substrate) and only substrate injection ($+V_g$) stress is used to evaluate the values of $Q_{\rm bd}$.

In this letter, we propose a simple and reliable method to prepare a textured Si surface for the fabrication of a tunnel oxide film. Tunnel oxide film grown on this textured single-crystal Si surface with excellent electrical properties and reliabilities can be easily obtained.

II. Experiments

A 12-nm poly-Si film was first deposited on (100) 4–7 Ω·cm p-type Si wafers, by using a LPCVD system at 590 °C and a 30-nm thick dry SiO_2 film was then grown at 900 °C in dry O_2 ambient. For comparison, wafers without the poly-Si deposition were also grown (30-nm thick dry SiO_2 film at 900 °C). This 30-nm thick SiO_2 film served as a sacrificial oxide film. The deposition rate of poly-Si was controlled at about 6 nm/min at pressure of 100 mTorr. During the oxidation step, both the poly-Si film and the Si substrate were oxidized. Due to the enhanced oxidation rate of the poly-Si grain boundaries, a rugged SiO_2/Si interface was formed. After stripping the 30-nm thick sacrificial oxide film, a textured Si surface was obtained which was observed by the AFM micrograph in Fig. 1. The surface roughness is 0.596 and 0.079 nm (RMS values) of textured Si wafer and normal Si wafer, respectively. This is a simple and reliable process to form a textured Si surface which does not need to etch the surface of Si substrate [2] and is without the constraint of stopping the oxidation process on the poly-Si/Si-substrate interface to get better electrical characteristics [6]. Moreover, tunnel oxide is grown on the textured single-crystal Si wafer (not on poly-Si substrate) which is different from the method of [6].

Tunnel oxide films were then grown on the textured Si surface and, for comparison, on a normal Si surface at 900 °C in dry O_2 ambient. A 30-nm thick $POCl_3$-doped LPCVD poly-Si film was deposited on the oxides for the MOS capacitors fabrication. The effective oxide thickness of the SiO_2 films in our experiments was 10 nm, which was determined by the high-frequency C–V measurement. The areas of the MOS capacitors were 3×10^{-4} cm^2 with circular shapes. A white light lamp was used when the capacitors were biased at positive gate voltage (substrate injection polarity).

The experiments are repeated several times to confirm the process reliability of our method and the same results can be obtained in every experiment.

III. Results and Discussions

Fig. 2 shows the J–E characteristics of oxide films grown on a textured Si surface (textured oxide) and on a normal Si surface (normal oxide). The J–E curves of textured oxide are similar to normal oxide. This means that the characteristics of textured oxide are close to normal oxide. This is due to the fact that the growth of textured oxide is on single-crystal Si surface (not on poly-Si film). However, it is found that for both injection polarities ($+V_g$ and $-V_g$), textured oxide exhibits a higher electron conduction efficiency than

Manuscript received June 23, 1997; revised November 26, 1997. This work was supported by the National Nano Device Laboratory, Hsinchu, Taiwan, R.O.C., under Grant NSC-86-2215-E-009-047.

The authors are with the Department of Electronic Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C.

Publisher Item Identifier S 0741-3106(98)03305-9.

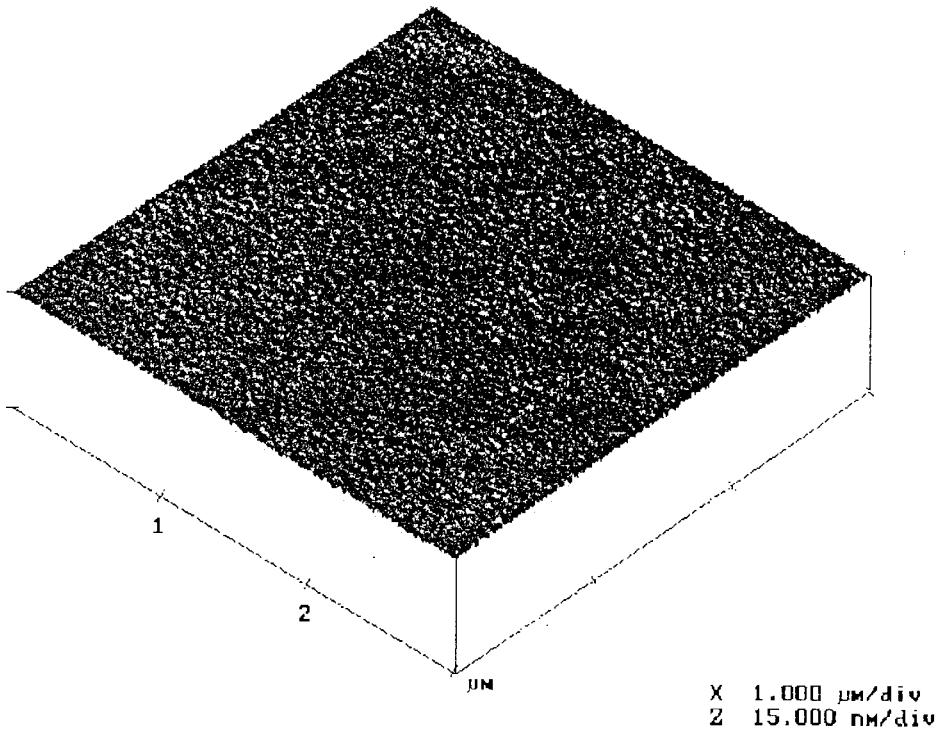


Fig. 1. The AFM micrograph of the textured Si-substrate surface.

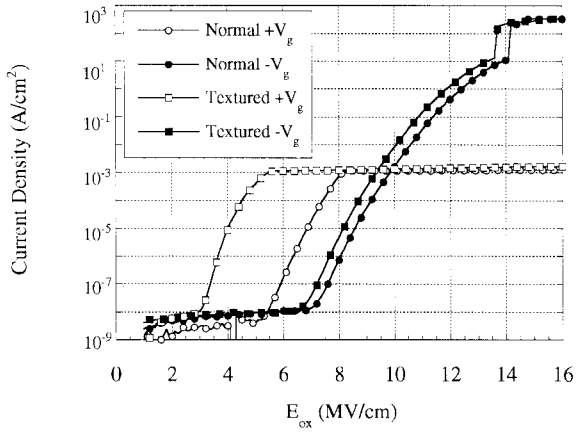


Fig. 2. The positive V_g and negative V_g J–E characteristics for the 10-nm thick textured and normal oxides.

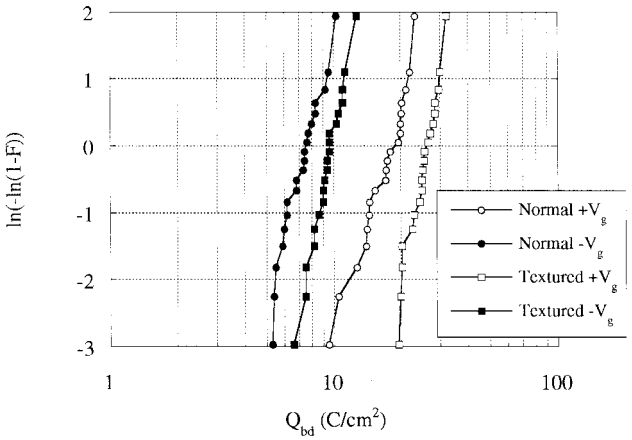
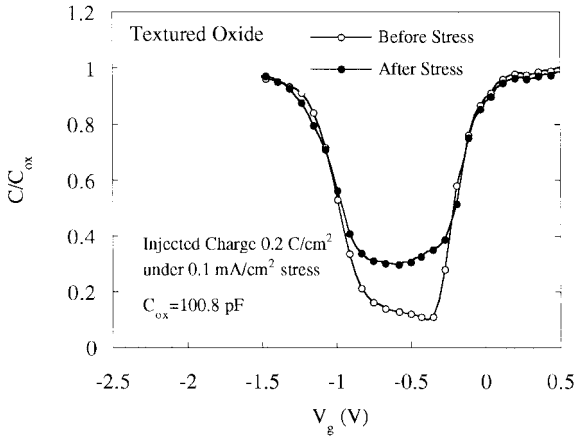


Fig. 3. The Weibull plot of charge-to-breakdown ($Q_{\rm bd}$) of textured and normal oxides in both polarities under 100 mA/cm^2 constant current stressing.

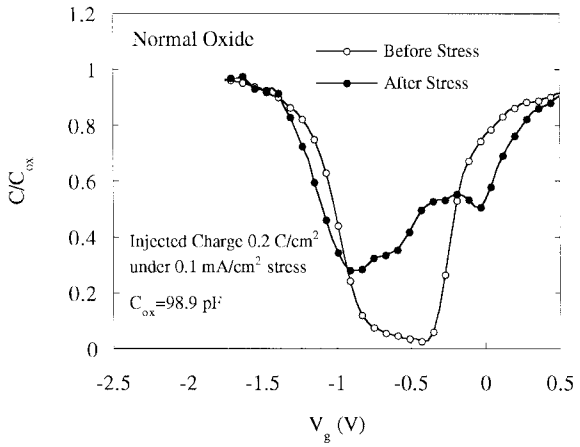
that of the normal oxide. Moreover, for substrate injection polarity ($+V_g$), a much higher electron conduction in textured oxide can be observed. The textured surface of Si-substrate, as seen in Fig. 1, has semi-sphere-like asperities. If oxide film is grown or deposited on this textured Si surface, a rugged SiO_2/Si interface can be expected. A field enhancement effect at the asperities of the rugged SiO_2/Si interface of the textured oxide enhances electron injection into oxide film [4], which makes the Fowler–Nordheim (FN) injection occur at lower gate voltages. The lower FN occurred voltage and asymmetry of J–E characteristics of textured oxide are beneficial for the device applications for low programming voltage application.

Fig. 3 shows the Weibull plot of charge-to-breakdown ($Q_{\rm bd}$) of textured and normal oxides with the injection polarities from gate ($-V_g$) and substrate ($+V_g$) under 100 mA/cm^2 stress. It is found that $Q_{\rm bd}$ of textured oxide was larger than that of normal oxide in both polarities. This may be due to the fact that, for the textured oxide, a lower bulk electric field existed [7] which increased the stressing endurance and a higher $Q_{\rm bd}$ was observed.

Fig. 4 shows the quasi-static C–V characteristics of textured and normal oxides before and after the injection of 0.2 C/cm^2 under 0.1 mA/cm^2 stress. For the textured oxide, the degradation in the C–V curve after stressing was smaller than that of the normal oxide. In other words, interface traps generation and the net traps charging induced by FN injection are much smaller in the textured oxide compared with the normal oxide, as indicated by the much smaller C–V distortion and shift.



(a)



(b)

Fig. 4. (a) The quasi-static C–V characteristics of textured oxide before and after the injection of 0.2 C/cm^2 under 0.1 mA/cm^2 stressing. (b) The quasi-static C–V characteristics of normal oxide before and after the injection of 0.2 C/cm^2 under 0.1 mA/cm^2 stressing.

Fig. 5 shows the curves of the gate voltage shift versus the stressing time of textured tunnel oxide and normal oxide under a constant current stressing of -10 mA/cm^2. It is seen that both oxides exhibit the electron trapping behaviors. However, the gate voltage shift of textured oxide is smaller than that of normal oxide. This implies that textured oxide has a better immunity of electron trapping under high field stressing. The localized thinly tunnel oxide exists on textured Si surface. Thin effective thickness leads to weak stress. Weak stress shows better $Q_{\rm bd}$, fewer $D_{\rm it}$, and fewer electron traps.

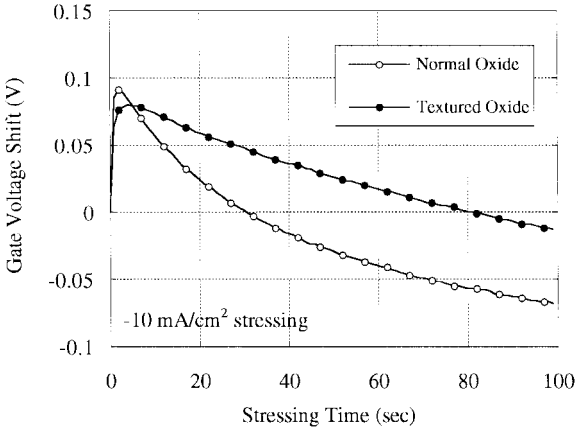


Fig. 5. The curves of gate voltage shift versus the stressing time for textured oxide and normal oxide under a constant current stressing of -10 mA/cm^2.

IV. Conclusion

A new simple and reliable method to form a textured Si surface has been proposed in this letter. Tunnel oxide grown on this textured Si substrate possesses an asymmetrical J–E characteristics, less interface states generation and better reliability (larger $Q_{\rm bd}$). They are suitable for the low-voltage operations of nonvolatile memory devices in the future.

References

[1] M. Olcer, H. J. Buhlmann, and M. Ilegems, "Enhanced current injection in thermal oxides growth on texturized silicon," *J. Electrochem. Soc.*, vol. 133, no. 3, p. 621, 1986.

[2] C. Y. Kwok, A. Williams, M. Gross, E. Gauja, and S. O. Kong, "Effects of controlled texturization of the crystalline Si surface on the SiO_2/Si effective barrier height," *IEEE Electron Device Lett.*, vol. 15, p. 513, Dec. 1994.

[3] M. Y. Hao, and J. C. Lee, "Electrical characteristics of oxynitrides grown on textured single-crystal silicon," *Appl. Phys. Lett.*, vol. 60, no. 4, p. 445, 1992.

[4] S. L. Wu, C. L. Lee, and T. F. Lei, "Tunnel oxide prepared by thermal oxidation of thin polysilicon film on silicon (TOPS)," *IEEE Electron Device Lett.*, vol. 14, p. 379, Aug. 1993.

[5] H. P. Su, H. W. Liu, P. W. Wang, K. L. Cheng, I. M. Jen, G. Hong, and H. C. Cheng, "Novel tunneling dielectric prepared by oxidation of ultrathin rugged polysilicon for 5-V-only nonvolatile memories," *IEEE Electron Device Lett.*, vol. 16, p. 250, June 1995.

[6] S. L. Wu, D. M. Chiao, C. L. Lee, and T. F. Lei, "Characterization of thin textured tunnel oxide prepared by thermal oxidation of thin polysilicon film on silicon," *IEEE Trans. Electron Devices*, vol. 43, p. 287, Feb. 1996.

[7] Y. Fong, A. T. Wu, and C. Hu, "Oxides grown on textured single-crystal silicon-dependence on process and application in EEPROM's," *IEEE Trans. Electron Devices*, vol. 37, p. 583, Mar. 1990.