Pergamon

Solid-State Electronics Vol. 42, No. 5, pp. 823–830, 1998
Published by Elsevier Science Ltd. All rights reserved
Printed in Great Britain
0038-1101/98 $19.00 + 0.00

PII: S0038-1101(97)00282-7

WELL SUPPLY VOLTAGE EFFECT ON ESCAPE CURRENT OF GUARD RINGS IN EPITAXIAL CMOS TECHNOLOGY

CHIH-YAO HUANG[1] and MING-JER CHEN[2]

[1]Mosel-Vitelic Inc., Science-Based Industrial Park, Hsinchu 300, Taiwan, R.O.C.
[2]Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

(Received 15 September 1997; accepted 29 October 1997)

Abstract—An n-well guard ring dual collector structure formed on an epitaxial substrate has been characterized and simulated. The measured *I–V* characteristics have exhibited that a reduction of well supply voltage from 5.0 to 1.0 V causes an increase in the escape current into the outer well by a factor of about 14, while the base and inner guard ring collector currents are hardly changed. This will influence neighboring latchup susceptibility substantially. This experimental observation can provide a new evidence of the published theory responsible for the escape current: the injected minority carriers flow through a quasi-neutral layer between the upper collecting plate and the bottom high/low junction reflecting plate. Based on this theory actual epitaxial layer thickness can be extracted with low guard ring voltages as well. Published by Elsevier Science Ltd. All rights reserved

1. INTRODUCTION

Minority-carrier well-type guard ring has been intensively employed as one of the layout techniques in order to overcome the latchup in CMOS circuits[1]. Input/output areas of CMOS circuits usually suffer from overstress of outside world especially in the worst noisy environment. Under such circumstances the n^+ contact regions in the input/output regions act as minority carrier injectors into the neighboring SCR-like structure, and the amount of the injected carriers may exceed the critical level required to trigger the neighboring region into latchup. Therefore, well-type guard rings surrounding the parasitic injectors are utilized to collect these minority carriers injected into the substrate, and hence to avoid latchup by bipolar decoupling effect. The efficiency of such guard rings is greatly enhanced by an epitaxial layer grown on a heavily-doped substrate[2]. Further study had pointed out that such enhancement is due to Auger recombination in the heavily-doped substrate[3]. The minority-carrier current injected from the parasitic emitter not only flows laterally into the guard-ring well sidewall but also transports vertically down spreading over the whole high/low doping substrate. The vertical component is further divided into two components: the first due to minority carriers injected into a sandwich layer between the upper collecting plate and the bottom reflecting plate, namely sandwich escape current I_{san}, and the second due to those penetrating the high/low junction and then spreading out in the large, highly-doped bulk as in the non-epi substrate, namely substrate escape current I_{sub}[4,5]. Furthermore, an analytic design model has been proposed to quantitatively describe this behavior, and also used to establish design guidelines of the guard rings[4–6]. In addition, the characterization and modeling of the guard ring structure at low temperature have been studied as well[9,10]. As a whole, the previous studies all concerns structural parameters of the guard ring for enhanced latchup immunity, the points of view in[4–6] all emphasize the guard-ring width dependence of the escape currents. In fact, the slope coefficient of the guard-ring design model in these results includes a depletion width term. This implies that escape current is also a function of the guard-ring well supply voltage and this well bias can also control the escape current. Under such circumstance's feasibility of guard rings with different power supply voltages still needs more understanding and investigation. In this paper, a 6 μm wide guard ring has been characterized under different supply biases from 1.0 to 11.0 V to illustrate the well supply voltage effect on the escape current. The accompanying simulation results help to describe and analyze the experimental behaviors in detail. These characteristics have also been used to extract the real epitaxial layer thickness by utilizing the guard-ring design model.

2. EXPERIMENTS

The structure shown in Fig. 1(a) was the dual square collectors surrounding an emitter region on the epitaxial substrate. These two collector regions were two n-wells fabricated by conventional n-well polysilicon CMOS technology. The inner square

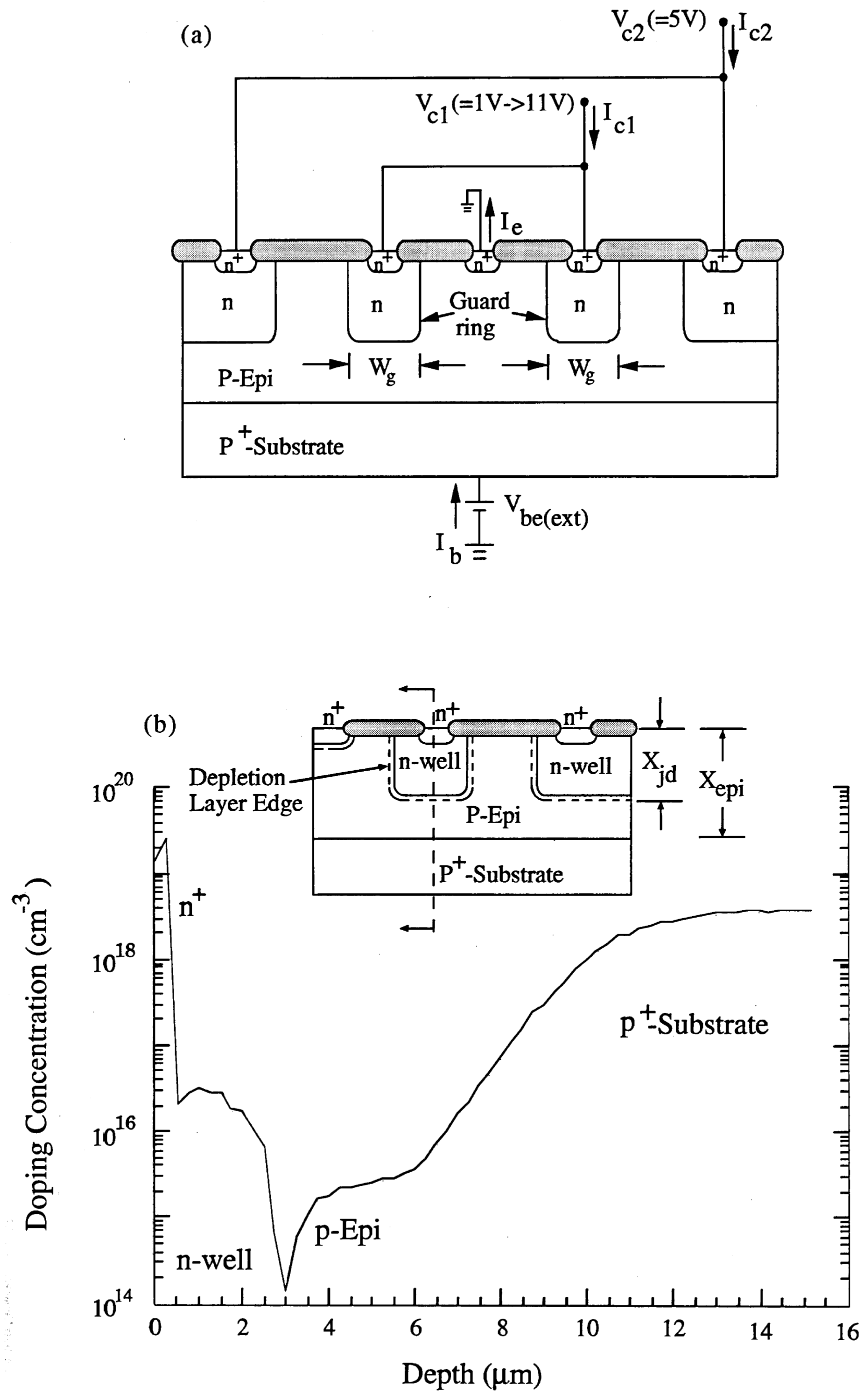

Fig. 1. (a) The schematic cross section of a n-well guard ring structure on the p-epi/p^+-substrate where n^+ emitter, inner and outer n-well collector are also shown. (b) the measured doping profile along the depth direction for test structure illustrated in the upper part of the figure

collector was a 6 μm wide guard ring and the outer one acted as internal circuitry. The lightly doped epitaxial layer where all devices were fabricated was grown on the heavily doped substrate. The doping profile in depth direction measured by spreading resistance is shown in Fig. 1(b). The outer n-well was biased at 5.0 V and the guard ring bias was varied from 1.0 to 11.0 V. The emitter was grounded and substrate-emitter bias $V_{\rm be}$ swept from 0.0 to 1.0 V.

Figure 2(a) shows the Gummel plots of the base current $I_{\rm b}$, the guard ring collection current $I_{\rm c1}$ and the escape currents $I_{\rm c2}$ collected by the outer collectors with the guard ring biases $V_{\rm c1}$ ranging from 1.0 to 11.0 V. To check whether the wider depletion

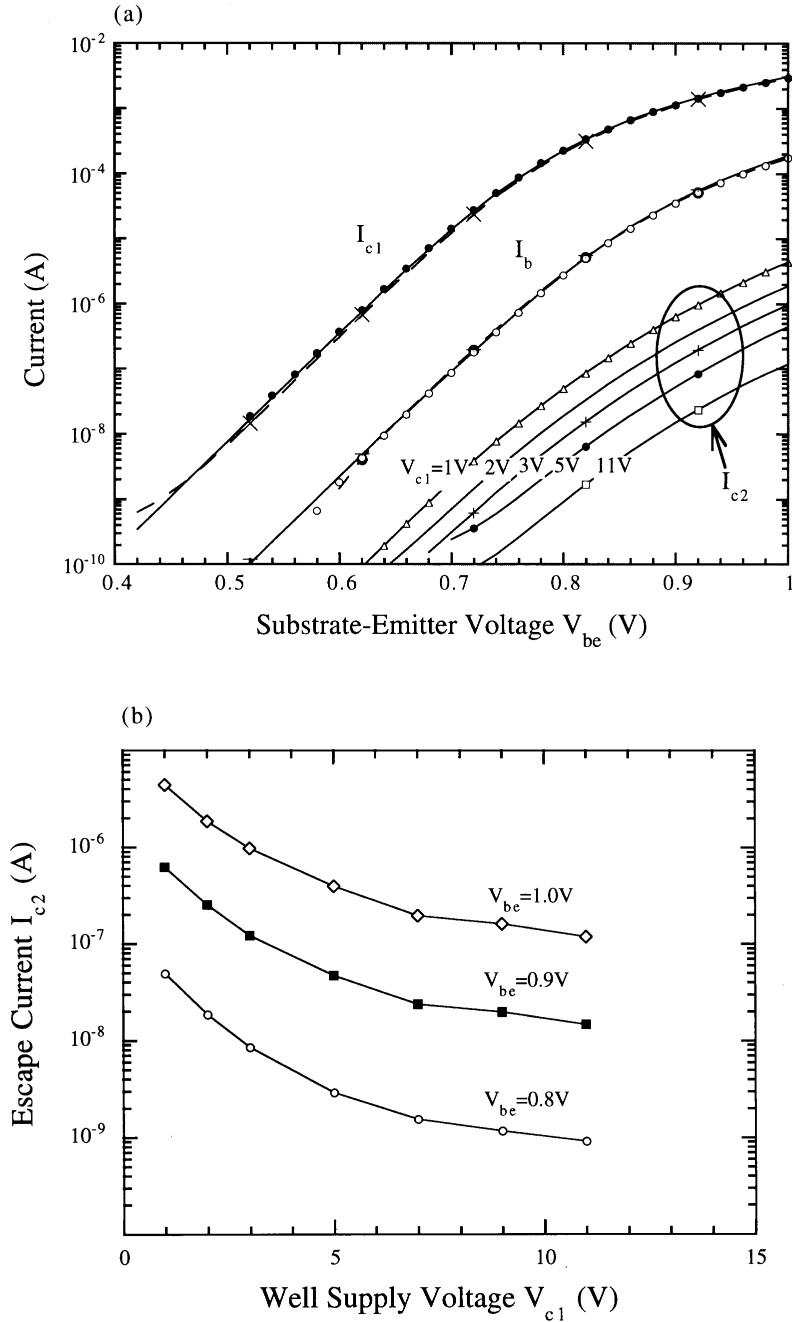

Fig. 2. (a) The Gummel plot of base, collector currents for test structure with guard ring width 6 μm. The escape currents I_{c2} are also measured with different guard ring contact V_{c1} bias from 1 to 11 V. (b) the measured escape currents I_{c2} as function of V_{c1} for different V_{be} bias

region around the inner guard ring interferes the escape probability of the outer well around its sidewall area, the cases of $V_{c1} = V_{c2}$ were also measured and no significant variation in any terminal current was observed as compared with $V_{c2} = 5.0$ V cases. From the illustration I_b, I_{c1} all remain the same during V_{c1} variation, but I_{c2} decreases with the increase of the V_{c1} biases. Figure 2(b) shows the escape currents as a function of V_{c1} with the different V_{be} values. When V_{c1} initially decreases from 11.0 V I_{c2} rises moderately, whereas with V_{c1} smaller than 7.0 V the increased amount of I_{c2} apparently becomes significant, which will be discussed in the following section. For V_{c1} ranging from 1.0 to 11.0 V there is a diminishment of I_{c2} by a factor of 60–40. Moreover, for V_{c1} within 5 V in most real applications 17 to 10 times rises in I_{c2} are obtained. The guard ring bias from 5.0 to 1.0 V is estimated to have the same effect on the collection efficiency as that with an equivalent narrower guard ring, which

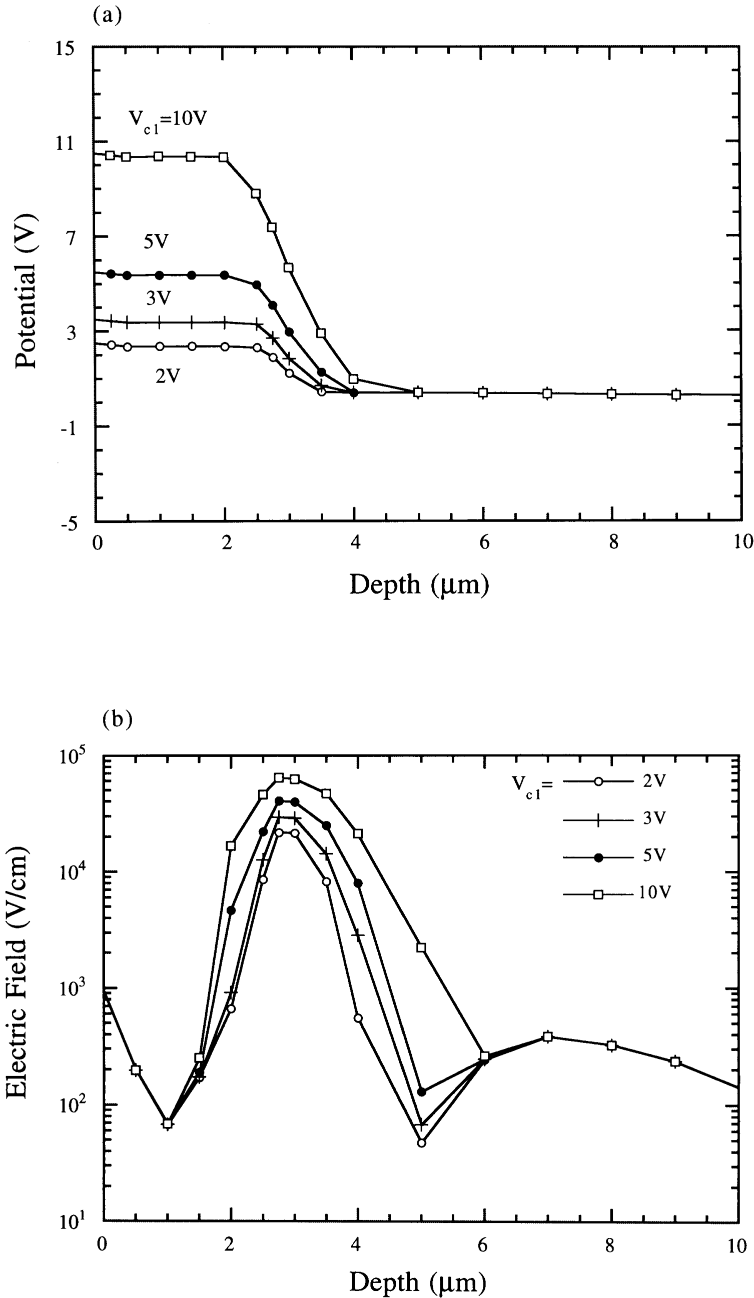

Fig. 3. (a) The simulated potential distribution along the depth direction at X-coordinate = 11.5 μm with different guard ring contact V_{c1} bias at V_{be} = 0.7 V. (b) the simulated electric field along the depth direction with different guard ring contact V_{c1} bias at V_{be} = 0.7 V

narrows 2.6 times the thickness of the sandwich layer. This estimation will be explained in the next section.

3. SIMULATIONS AND DISCUSSIONS

In order to confirm the detailed behaviors inside the structure, 2D device simulator TMA MEDICI was utilized to simulate the above structure[7]. The measured doping profile was inputted into MEDICI directly as vertical doping data. The physical models such as Auger recombination, concentration dependent Shockley–Read–Hall recombination and bandgap narrowing effect have been taken into account. The simulator has been calibrated to fit the experimental I–V characteristics so as to provide accurate simulation predictions. Figure 3(a) and (b) are the simulation results of the potential distribution and magnitude of the electric field along the depth direction with the different V_{c1} values at V_{be} = 0.7 V. It's obvious that larger bias at the guard ring contact produces a wider well de-

pletion width, namely a thinner quasi-neutral sandwich-layer thickness. Subsequently, the sandwich-layer thickness can be modulated by the power supply voltage at well V_{c1}. A wider reverse-bias depletion width means that it is easier to sweep more minority carriers across this field region into the n-well. The doping profile of the epitaxial sandwich layer can be divided into two regions according to Fig. 1(b): the first changes linearly just below the well bottom junction until 4.0 μm deep, and the second, which can be assumed nearly uniform, slowly increases from 4.0 to 6.0 μm depth, where the high/low doping transition edge is clearly seen. The pronounced variation of the first part of the doping profile gives rise to a larger built-in electric field. In addition to the larger built-in field, depletion width expands rapidly in the p-type epitaxial layer around the region from 3.0 to 4.3 μm owing to the low value of the first part of the doping profile below the n-well bottom, and consequently I_{c2} reduces rapidly with V_{c1} increase in the range from 1.0 to 6.0 V as shown in Fig. 2(b). The electric depletion region, which width is determined from 2D contour plot by charge neutrality principle in MEDICI, bounds on depth position about 4.4 μm deep with V_{c1} bias equal to 7.0 V as shown in Table 1. The concentration in the second part of the doping profile becomes higher than the first and more uniform with the vertical distance deeper than 4.4 μm, as a result the depletion width becomes slowly varied with V_{c1} larger than 7.0 V. Therefore I_{c2} in Fig. 2(b) with V_{c1} above 7.0 V decays more gradually. The above discussion is applicable to V_{be} biases up to the onset of the high-level injection region, i.e., V_{be} around 1.0 V region.

Figure 4(a) and (b) show the electron current density along the vertical line located on the right half of the guard ring well at $V_{be} = 1.0$ V for different V_{c1} values. This vertical line is located at the dashed line of the cross section in Fig. 1(b). In Fig. 4(a) for vertical depth below 4.0 μm larger V_{c1} bias produces less X-component flowing current density implying large part of the escape current collected by the outer n-well with low V_{c1} bias. From the above results the escape current I_{c2} can obviously be modulated by the guard-ring reverse-bias voltage, and so this kind of operation provides an alternative way for the regulations of the guard ring performance in CMOS IC's. According to studies in[11,12], minority/majority carrier injection from neighboring region several hundred μm away can greatly degrade latchup hardness. The rise of the escape current under low supply voltage operation will definitely affect neighboring latchup immunity substantially. In Fig. 4(b) the Y-component electron current densities slightly decrease with respect to increased V_{c1} in the heavily doped substrate all along the depth direction. For the region between 6 and 8 μm the Y-component current densities become slightly larger for larger V_{c1} value. This behavior becomes distributed all over the guard ring well bottom when V_{be} becomes larger as indicated in the simulations. This results from the greater reverse-biased electric field around the n-well junction by larger V_{c1} bias. This larger field sweep minority carriers more easily from the p-substrate into the n-well guard ring, hence larger Y-component electron current densities collected by the guard-ring well bottom are created. From the simulation the electron current density distribution along a horizontal line beneath the n-well also illustrates modulation by V_{c1} and a reduction of one order of magnitudes in the electron currents are also observed. Therefore, both the above experimental data and simulation results verify the evidence that the escape currents are mostly composed of the minority carriers injected into the sandwich layer.

As mentioned in the previous studies[4,5], the sum of I_{san} and I_{sub} gives the escape current collected by the outer n-well. A design model has been developed for quantitatively describing the escape current as the sum of the following two components:

$$I_{san} = I_{eff1}\exp\left(-\frac{W_g}{L_{eff1}}\right) \qquad I_{sub} = \eta I_{eff1}\exp\left(-\frac{W_g}{L_{eff2}}\right), \quad (1)$$

where $I_{eff1} = 2qD_n n^* W_{eff}/\pi$ and $L_{eff1} = 2(X_{epi} - X_{jd})/\pi$. The parameter n^* is the effective carrier concentration at the left end side of sandwich layer, D_n is effective diffusion constant, W_{eff} is the effective peripheral length of device, and W_g is the guard-ring well width. X_{epi} represents the epitaxial layer thickness and X_{jd} represents the distance from the semiconductor surface to the n-well depletion-region bottom edge. In the I_{sub} equation L_{eff2} is an empirical fitted parameter, and η represents capability of

Table 1. The depletion width comparisons among the 2D results of the Medici numerical simulations, calculations from the depletion approximation by the linearly-graded assumption and uniform profile assumption

V_{c1} (V)	1	2	3	5	7	9	11
ΔX_{jd} (μm)							
2D simulation	0.4	0.77	0.90	1.15	1.39	1.61	1.81
Linearly-graded assumption	0.83	1.05	1.19	1.42	1.58	1.73	1.85
Uniform assumption	0.78	1.10	1.35	1.74	2.06	2.34	2.59

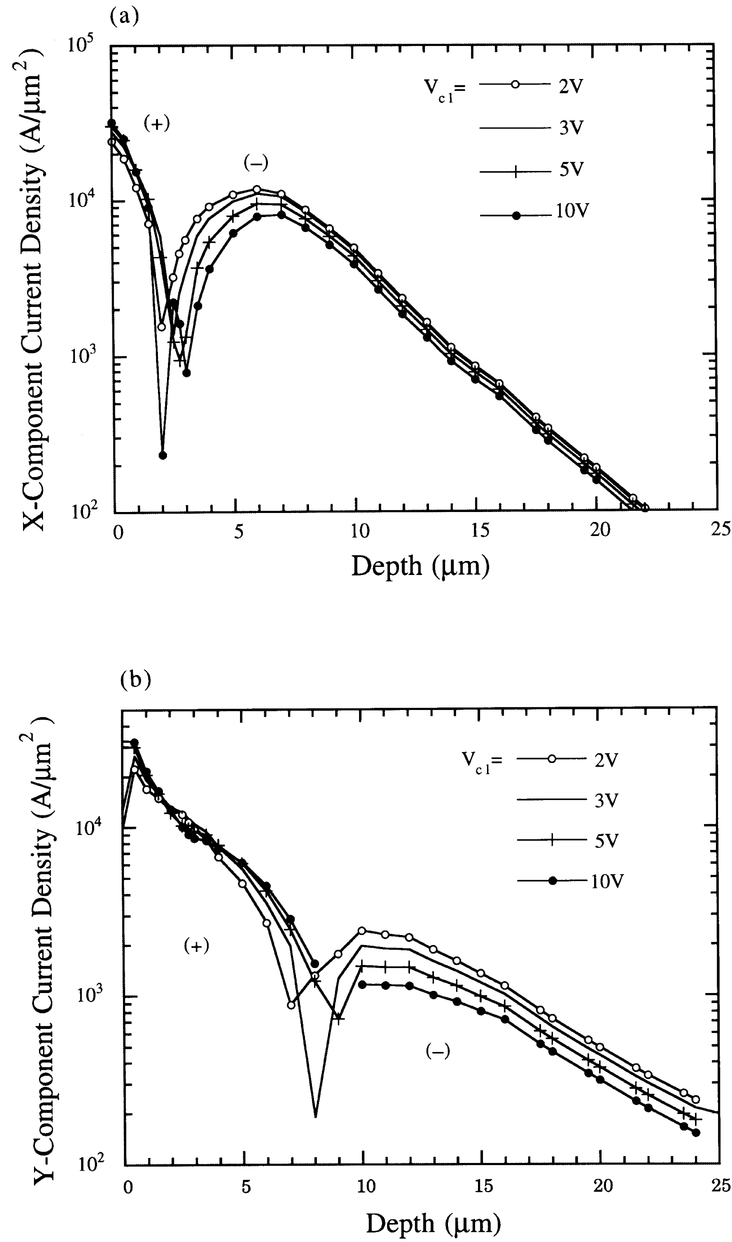

Fig. 4. (a) The X-component and (b) Y-component electron current density along the vertical line located on the right half of the guard ring n-well. The positive sign indicates the current flow direction is right in X coordinate and upward in Y coordinate, the minus sign indicates left in X coordinate and downward in Y coordinate

minority carriers penetrating the high/low junction[4,5]. From the I_{san} equation the increase of X_{jd} results in decreased L_{eff1} and hence a decrease of I_{c2}. In other words, the V_{c1} well supply voltage is an alternative measure to control the guard ring efficiency.

Based on the studies of previous work[5,6], the I_{sub} component is generally much smaller than the I_{san} component especially for narrow guard ring width cases. The effect of V_{c1} can be estimated solely by means of the I_{san} model with acceptable accuracy for small V_{c1} values, because the current along the sandwich layer is more significant for small V_{c1} values. The V_{c1} swept from 11.0 to 1.0 V leads to a rise in the escape current by about 50 times on the average as shown in Fig. 2(b). From Equation (1) such a rise in the I_{san} value requires the guard-ring width to be increased about four times the value of (X_{epi}–X_{jd}). In other words, the effect of the V_{c1} bias is equivalent to that of the guard-ring width increase by four times the thickness of the sandwich layer. In the test structure X_{epi} is about 6 μm and average X_{jd} is about 4 μm, this yields an increase in guard ring width by about

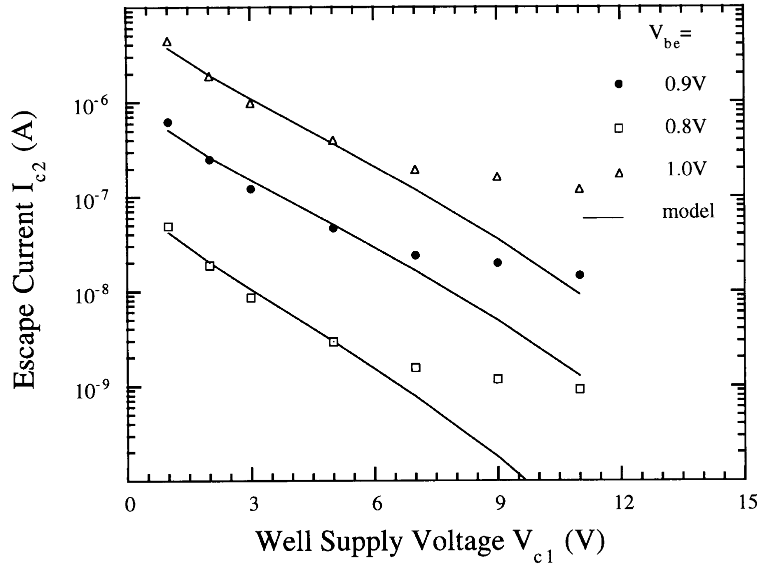

Fig. 5. The comparison of calculation of the fitted model with the experimental data as a function of V_{c1} for different V_{be} bias

8 μm. The V_{c1} voltage ranging from 5.0 to 1.0 V causes a rise of I_{c2} by about 14 times, indicating that the guard ring width should be widened by about 2.6 times the thickness of the sandwich layer. The thinner the epitaxial layer, the less area the guard ring structure may consume.

The data points with low V_{c1} values in Fig. 2(b) exhibit significant dependence on V_{c1}. This property is feasible for extraction of the epitaxial-layer thickness. Starting from I_{san} of Equation (1), X_{jd} can be written as $X_{jw}+\Delta X_{jd}$ where X_{jw} is the n-well metallurgical junction depth, and ΔX_{jd}, the depletion width, is extended downward from the well metallurgical junction of the guard ring bottom, which is located at 3 μm deep. The term (X_{epi}–X_{jw}) is then written as ΔX_{epi}, the I_{c2} equation can be expressed as follows:

$$I_{c2} \cong I_{eff1}\exp\left(\frac{-W_g}{2(\Delta X_{epi} - \Delta X_{jd})/\pi}\right). \quad (2)$$

Now ΔX_{jd} should be expressed as a function of V_{c1}. According to the doping profile shown in Fig. 1(b), the epi-layer from the n-well junction to 4 μm deep can be fitted excellently with the linearly graded profile[8]. Therefore I_{c2} becomes

$$I_{c2} \cong I_{eff1}\exp\left(\frac{-W_g}{2(\Delta X_{epi} - CV_{c1}^{1/3})/\pi}\right), \quad (3)$$

where $C = (12\varepsilon_s/qa)^{1/3}$, a is the coefficient of the linearly graded doping function. Here a equals 1.74×10^{19} cm^{-4}, and C is calculated to be 1.66 μm V$^{-1/3}$. We have obtained the escape current model as a function of V_{c1}. This equation is used to fit the experimental data in Fig. 2(b) for the low V_{c1} region. The fitting at V_{be} around 0.9 V is still able to give the precise doping information because the concentrations of the injected minority carriers in the epi-layer are still smaller than the background doping as indicated in the simulation. The fitted results are illustrated in Fig. 5. The average ΔX_{epi} value extracted from the fitted coefficient is 2.7 μm. Adding the n-well junction depth 3.0 μm, the epitaxial layer thickness is given to be 5.7 μm. Note that this extracted value seems smaller than 9.5 μm reported in[6]. In fact, according to simulation in the guard ring width variation part the current flow along the high/low junction transition is still collected into the guard ring well, while in the well supply voltage variation the current flow into the well is mostly restricted above high/low junction transition as shown in Fig. 4(b). The discrepancies above $V_{c1}=7.0$ V result from the domination of the current below the low-doping transition edge of the high/low junction over the I_{san} component. In such circumstances the design model cannot describe the transition region behaviors precisely. To verify the linearly graded assumption, the depletion width values ΔX_{jd} from the 2D simulation results, the linearly graded and the uniform profile assumptions shown in Table 1 were substituted into Equation (2) for X_{epi} comparison. The same epi-layer thickness was obtained from both the linearly graded assumption and 2D simulation case. For the step profile case X_{epi} is calculated to be 6.5 μm, which is larger than the actual high/low junction depth. This confirms the validity of the linearly graded assumption. The above calculation is well consistent with the measured doping profile shown in Fig. 1(b). Hence the extraction of X_{epi} by means of the I_{san} model can give accurate extraction for a specific structure. This also justifies the validity of guard-ring design model in Equation (1). In addition, the design model is

proved to be still feasible at the onset region of high-level injection although it was primarily developed under low-level injection condition.

4. CONCLUSION

New observations on the well supply voltage effect of the guard rings have been characterized and investigated. By low power-supply voltage regulation the escape currents increase at least an order of magnitude. This result provides the experimental evidence of the minority carriers injecting into the sandwich layer and justifies the feasibility of the guard-ring design model. Such guard-ring bias has the same influence on the escape probability as the guard ring does with its width increase four times the thickness of the sandwich layer. In addition, the escape current characteristics can be utilized to extract the actual epitaxial layer thickness for a device structure.

Acknowledgements—The authors would like to thank Mr Ping-Nan Tseng, Taiwan Semiconductor Manufacturing Company, for fabricating our guard-ring structure design, and Mr Jeng-Kuo Jeng, Vanguard International Semiconductor Corp., for the doping profile measurement. This work was supported by the National Science Council under Contract NSC 84-2215-E-009-043.

REFERENCES

1. Troutman, R. R., *Latchup in CMOS Technology: The Problem and its Cures*. Kluwer Academic Publishers, Boston, 1986.
2. Troutman, R. R., *IEEE Electron Device Lett*., 1983, **4,** 438.
3. Chen, M. J. and Wu, C. Y., *Solid-St. Electron*., 1987, **30,** 879.
4. Chen, M. J. Huang, C. Y., Tseng, P. N., Tsai, N. S. and Wu, C. Y., *Proc. IEEE Custom Integrated Circuits Conf*. 4.5.1, 1991.
5. Chen, M. J., Huang, C. Y. and Tseng, P. N., *IEE Proc. G Circuit Dev. Syst*., 1993, **140,** 182.
6. Huang, C. Y. and Chen, M. J., *IEEE Trans. Electron Dev*., 1994, **41,** 1806.
7. MEDICI 1.0 User's Manual, Technology Modeling Associates, 1992.
8. Sze, S. M., *Physics of Semiconductor Devices*. John Wiley and Sons, New York, 1982, p. 81.
9. Huang, C. Y., Chen, M. J., Jeng, J. K. and Wu, C. Y., *IEEE Trans. Electron Dev*., 1996, **43,** 2249.
10. Huang, C. Y. and Chen, M. J., *Solid-St. Electron*, to be published.
11. Quinke, J., *Microelectron. Reliab*., 1990, **30,** 105.
12. Menozzi, R., Selmi, L., Sangiorgi, E. and Ricco, B., *IEEE Trans. Electron Dev*., 1991, **38,** 1978.