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Effect of reactive ion etching and post-etching annealing on the electrical characteristics of indium-tin oxide/silicon junctions

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Indium tin oxide (ITO) films were deposited onto p-type Si wafers with radio frequency (r.f.) magnetron sputtering. The effect of the silicon surface treatment with reactive ion etching (RIE) on the current–voltage (*I–V*) and capacitance–voltage (*C–V*) characteristics of the ITO/Si junction are investigated. When the Si substrate is etched by RIE prior to the deposition of ITO film, the *I–V* characteristics of the ITO/p-Si junction transfer from an ohmic contact for the unetched-Si to a rectifying contact for the etched Si. In addition, the barrier height, ideality factor, and series resistance increase with increasing etching power. This is attributed to the net positive ion charge and defects on the damaged surface. Thermal annealing can eliminate the damage caused by RIE. The *I–V* curves of ITO/etched p-Si become more ohmic as samples are annealed in N_2 at 300 °C. Secondary ion mass spectroscopy (SIMS) depth profiles indicate that some impurity defects migrate and/or disappear after post-etching annealing.

1. Introduction

Indium tin oxide (ITO) films show an interesting and technologically important combination of properties, they have high transmittance in the visible spectral region, high infrared reflectance and low electrical resistivity. This combination of properties has led to their use in transparent electrodes, antireflection coatings, display devices, photoelectric devices, and solar cells [1–4]. In the solar cell application, ITO films form the necessary heterojunction with the Si semiconducting absorber layer and act as the transparent front conducting electrode as well as the antireflective coating.

The ITO coatings have been fabricated by a variety of techniques, and the rectifying or ohmic behaviour of the ITO/Si heterojunctions depends on the technique used for depositing the ITO. It is reported that spray-deposited or vacuum evaporated ITO yields a rectifying junction on n-Si and an ohmic contact on p-Si [5, 6], while ion-beam-sputtered ITO gives an ohmic contact on n-Si and a rectifying barrier on p-Si [7]. Ishida and co-workers [8, 9], in their work on electron-beam-evaporated ITO films on Si wafers, reported that the intermetallic state at the ITO/Si interface, resulting from indium migration, caused this rectifying behaviour. The rectifying property of ITO/p-Si junctions prepared by ion-beam sputtering was attributed to the formation of a positively charged defect layer formed on the surface of Si during fabrication [10]. Previous work by Chiou *et al.* [11] reported a quasi-ohmic ITO/Si junction where ITO films were sputtered at powers too low to cause enough damage for the rectifying behaviour.

Reactive ion etching (RIE) is a key process in current microelectronics fabrication. As the minimum line width in device fabrication is reduced to 1 μm or less, dry etching processes to produce the desired anisotropic profiles become essential. RIE is a dry etching technique that is capable of etching densely packed micro-dimensional structures. In the fabrication of solar cells, anisotropic etching of ⟨1 0 0⟩ Si was employed to fabricate V-groove multijunction solar cells with reduced reflectivity [12]. However, RIE is carried out in a radiation environment where Si substrates are subjected to bombardment by electrons, ions, and photons. It can inherently induce damage and contamination into semiconductor materials and thus degrade the performance and yield of the final devices [13].

In this study, the effect of reactive ion etching on the electrical behaviour of ITO/Si heterojunction is investigated. Secondary ion mass spectroscopy (SIMS) is employed to study the contamination of Si wafers after RIE treatment. The current–voltage (*I–V*) and capacitance–voltage (*C–V*) characteristics of ITO/Si junctions are analysed. The effects of annealing on the *I–V* behaviour and contamination profile are explored.

2. Experimental procedures

P-type silicon wafers (1 0 0) with resistivity 1–10 Ω cm were used as substrate material. Standard RCA cleaning process, given in the Appendix, was employed to clean the Si substrates. After the RCA cleaning, wafers

were dipped in $HF + H_2O$ (1:100) solution several times, and rinsed in deionized (DI) water for 5 min to remove the SiO_2 layer formed on the Si surface. The Si wafer was then dried with nitrogen. Some substrates were etched with reactive ions before deposition of ITO films.

The plasma reactor used in the study is a conventional parallel plate type with aluminium electrodes of 20 cm diameter and 5 cm separation (VPS-1500/2000, Vacutec AB, Sweden). A 13.56 MHz r.f. generator was employed as the power supply through an automatic matching network. A teflon insulator was used to isolate the powered electrode from the grounded chamber. The substrates were loaded onto the cathode and the chamber pressure was kept at about 6.5 pa. The etching gases used were CF_4 and O_2. The reactant gases were controlled with a mass flow controller, mixed and distributed over the substrate through a specially designed gas ring. The flow rates were 40 $scm^3 min^{-1}$ and 5 $scm^3 min^{-1}$ for CF_4 and O_2, respectively. The power ranged from 30 W to 150 W and the etching time ranged from 30 s to 5 min.

ITO films were prepared by a commercial r.f. magnetron sputtering system (Ion Tech, U.K.). The sputtering target was a one-inch hot-pressed oxide ceramic (90 wt % In_2O_3 10 wt % Sn_2O_3, 99.99 wt % purity) supplied by Superconductive Components, Inc., USA. Details of the preparation of ITO films were described previously [1, 14]. The ITO films sputtered were about 210 nm thick. Film thickness was measured with a stylus surface profiler (Dektak 3030, ULVAC, Japan) with a 12.5-μm radius diamond-tipped stylus and a stylus force of 1–40 mg.

Aluminium electrodes were employed for both current–voltage (I–V) and capacitance–voltage (C–V) tests. The front electrode was applied by evaporating an Al film of ~ 0.7 mm diameter onto the ITO through a metal mask. The back-contact metallization was deposited by vacuum evaporation of ~ 500 nm Al on the back of the substrate. A semiconductor parameter analyser (HP4145, Hewlett Packard Co., USA) was employed in the dark I–V test. The C–V test was carried out with an HP4275 LCR meter.

3. Results and discussion

The surface morphologies of Si substrates etched with $CF_4 + O_2$ at various powers for various times are shown in Fig. 1. As can be seen from these micrographs, the higher the power and/or the longer the etching time, the rougher the surface. Secondary ion mass spectroscopy (SIMS) was used to characterize C, F, and O distributions in the etched Si. Figs 2–4 exhibit the depth profiles of fluorine, carbon, and oxygen for a silicon substrate etched in various conditions. Several observations are apparent from these

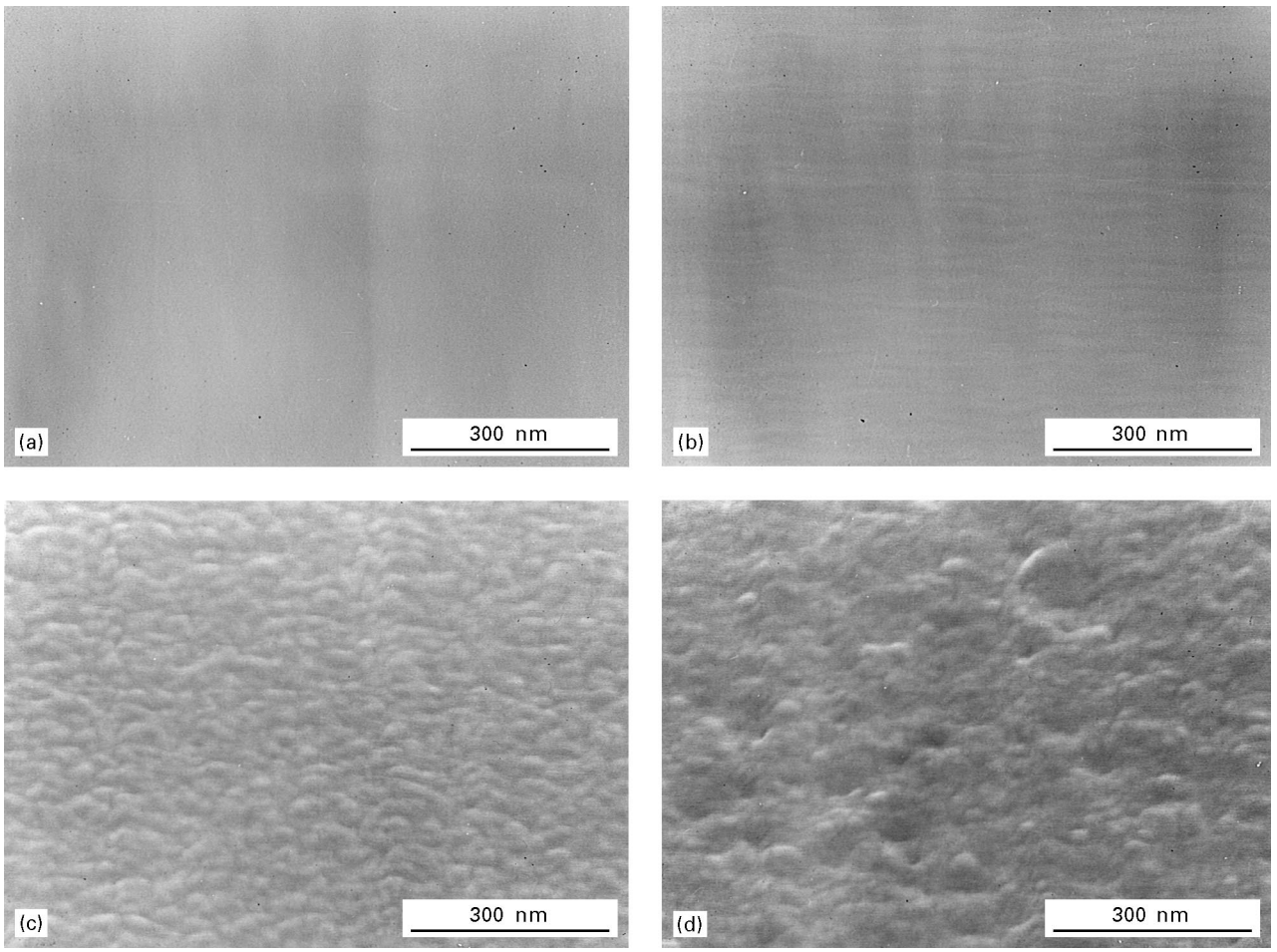

Figure 1 Scanning electron micrographs for Si substrates etched with $CF_4 + O_2$ for (a) 0 min, (b) 2 min at 50 W, (c) 5 min at 50 W, and (d) 5 min at 150 W.

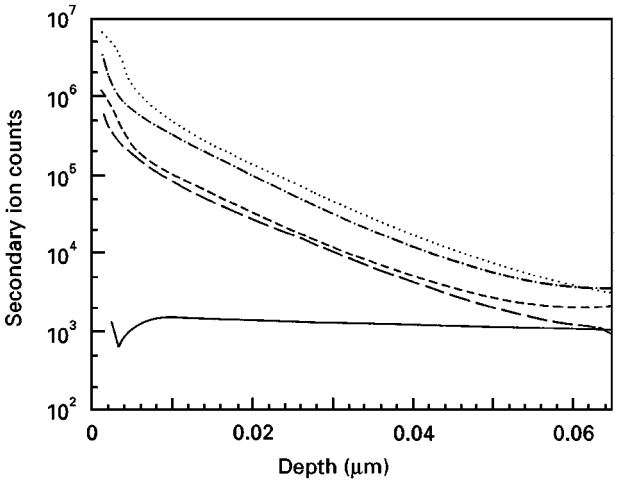

Figure 2 Fluorine depth profiles for RIE-etched Si without (——) and with post-etching annealing (· · · ·) 150 W for 1 h unannealed, (—·—·) 50 W for 1 h unannealed, (— —) 150 W for 1 h, 300 °C for 1 h in N_2, (– – –) 50 W for 1 h, 300 °C for 1 h in N_2.

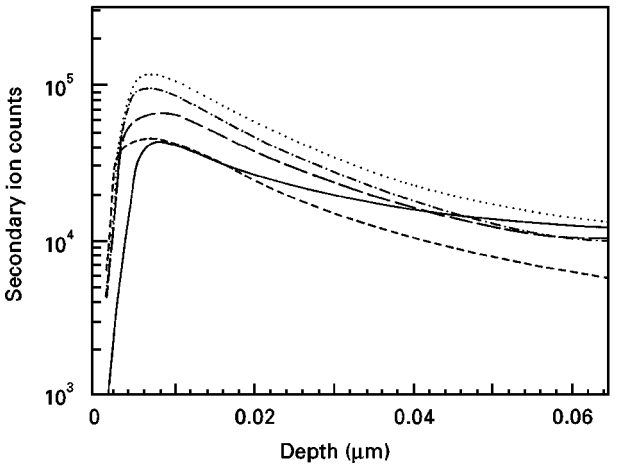

Figure 3 Carbon depth profile for RIE-etched Si without (——) and with post-etching annealing; (· · · ·) 150 W for 1 h unannealed, (—·—·) 50 W for 1 h unannealed, (— —) 150 W for 1 h, 300 °C for 1 h in N_2, (– – –) 50 W for 1 h, 300 °C for 1 h in N_2.

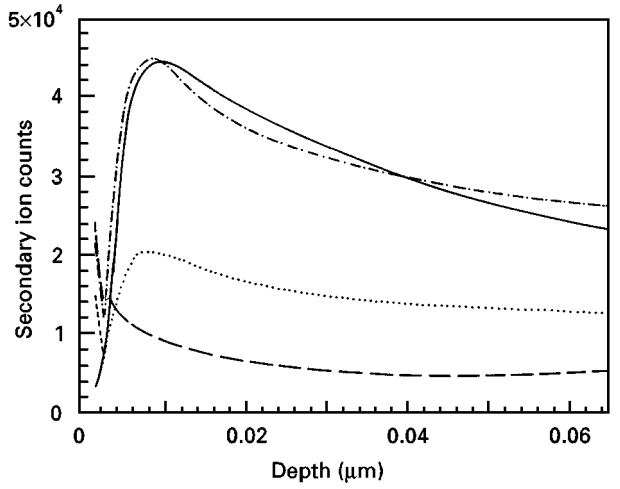

Figure 4 Oxygen depth profile for RIE-etched Si without (——) and with post-etching annealing; (· · · ·) 150 W for 1 h unannealed, (—·—·) 50 W for 1 h unannealed, (— —) 150 W for 1 h, 300 °C for 1 h in N_2.

figures. The concentration of fluorine decreases monotonically from the surface into the substrate, while those of carbon and oxygen show an initial increase followed by a decrease. The concentrations of F and C are higher for Si etched at higher power. In addition, post-etching annealing reduces the concentrations of C, F, and O in the Si wafer.

In RIE a glow discharge was used to generate, from a suitable feed gas by electron-impact dissociation/ionization, the gas-phase etching environment that consists of radicals, positive and negative ions, electrons, and neutrals. For example, the products from $CF_4 + O_2$ are F, F_2, COF_2, CO_2, and CO, in the presence of the Si the products are SiF_4, F, F_2, COF_2, CO_2, and CO [16]. These plasma-generated reactive intermediates diffuse from the bulk of the plasma to the surface of the material and etch the material. Some atoms will then be absorbed into the silicon surface and form defects. As shown schematically in Fig. 5, the damage in the near-surface region of the etched Si includes the surface gas residue layer, the impurity penetration layer, and the lattice damage layer [15, 16]. These damage regions generate interface states which affect the interfacial characteristics between Si and the ITO films.

Fig. 6 shows the *I–V* curve of an r.f. sputtered ITO film on an unetched p-type Si wafer. A linear

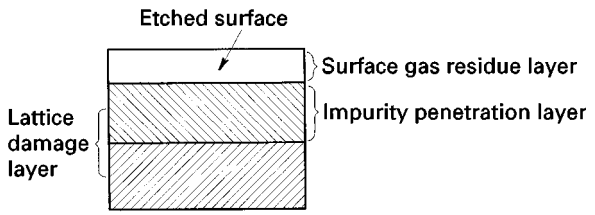

Figure 5 Schematic diagram of RIE-etched substrate.

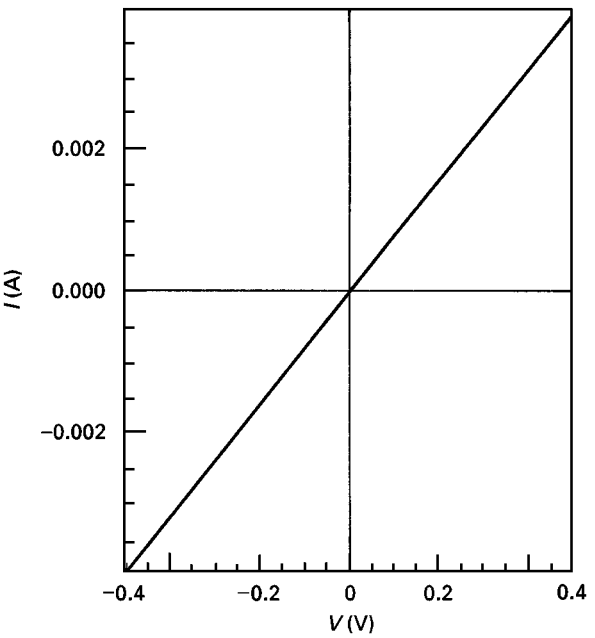

Figure 6 I–V characteristics of r.f. sputtered ITO on unetched p-type Si wafer.

relationship is obtained which suggests an ohmic contact with small barrier height and depletion width. Previous work by Dubow *et al.* [7] reported a rectifying property of ITO/p-Si junctions prepared by ion-beam sputtering. Ashok *et al.* [10] showed that it is the ion beam damage that caused the p-Si to deplete adjacent to the surface and resulted in the rectifying behaviour in sputtered ITO/p-Si junctions. However, the rectifying behaviour is not observed in the ITO/unetched Si junction. The r.f. sputtering of ITO does not cause enough damage to induce the rectifying behaviour reported in the literature.

Figs 7 and 8 give the *I–V* curves of ITO films on Si where Si substrates were etched for various times and powers, respectively. As can be seen from Figs 7 and 8, the ITO/Si junctions become rectifying contacts after an RIE treatment of the p-type Si substrate. At constant etching power, longer etching results in higher currents. Both the leakage current and forward bias current decrease as the etching power increases. The

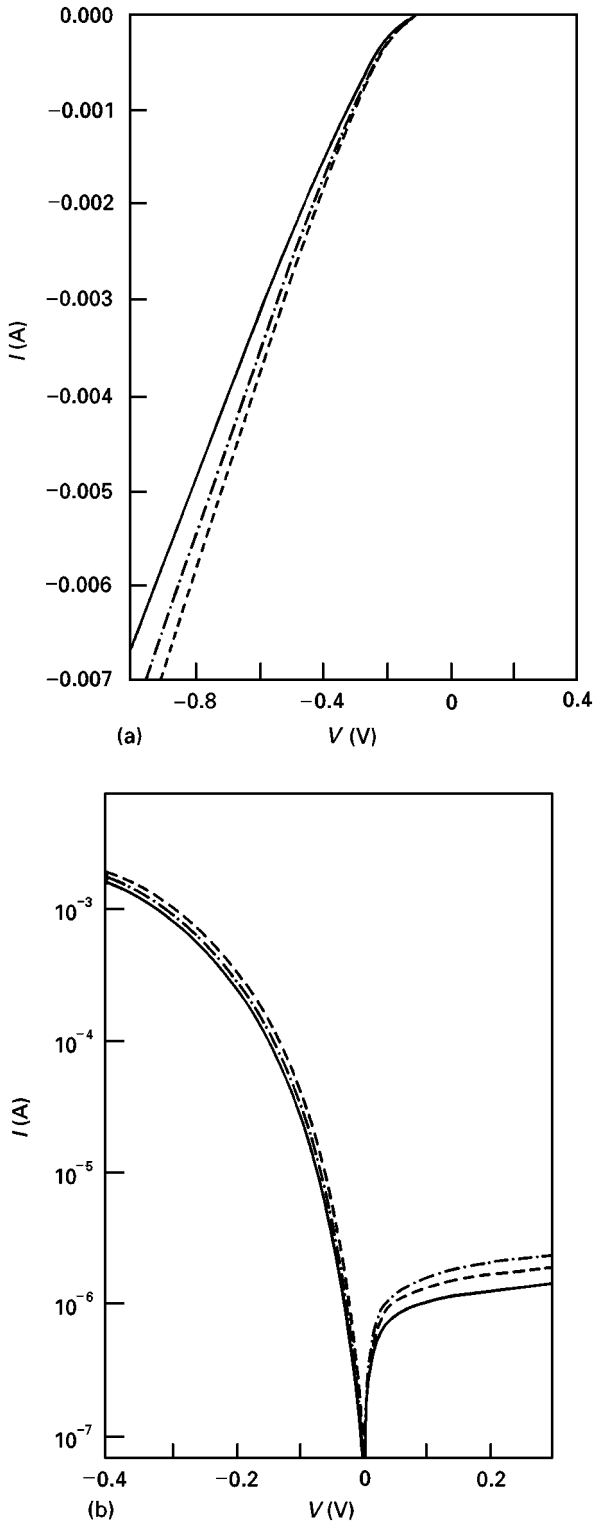

Figure 7 (a) *I–V* curves and (b) *I–V* curves on semi-logarithmic scale of ITO/p-type Si where Si substrates were etched at 50 W for various times: (——) 30 s, (–·–) 1 min, (– – –) 5 min.

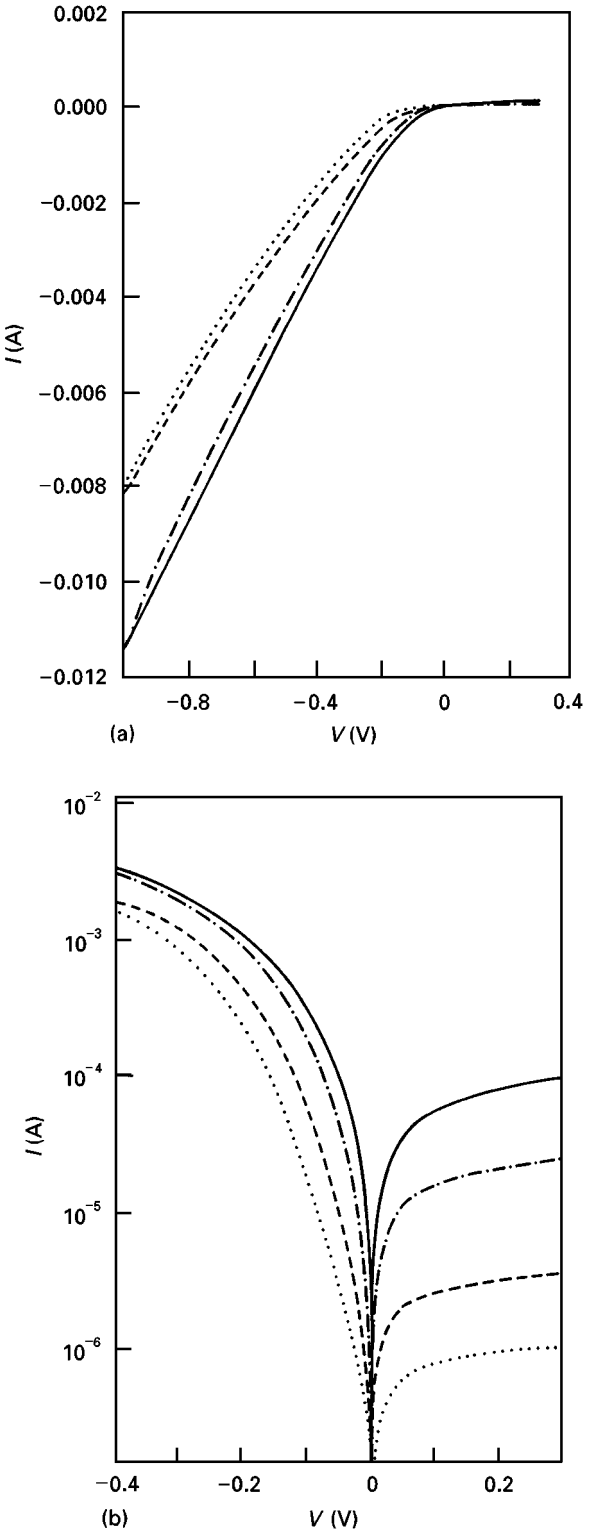

Figure 8 (a) *I–V* curves and (b) *I–V* curves on semi-logarithmic scale of ITO/p-type Si where Si substrates were etched at various powers: (——) 30, (–·–·) 50, (– – –) 100, (· · · ·) 150 W for 3 min.

barrier heights, ideality factor, and series resistance as a function of etching power are calculated and exhibited in Fig. 9. All three parameters increase with RIE sputtering power. These observations indicate that reactive ion-etching of an Si substrate changed the nature of the ITO/Si contact from ohmic to rectifying.

In order further to elucidate the effect of ion-etching on the Si surface, the C–V characteristics of the ITO/Si junctions are studied. In an ideal Schottky diode, a linear $1/C^2$ versus V plot is expected over all voltage ranges, as described in the following equation [12]:

$$\frac{\partial\left(\frac{1}{C^2}\right)}{\partial V} = \frac{-2}{q\varepsilon_s N_D} \tag{1}$$

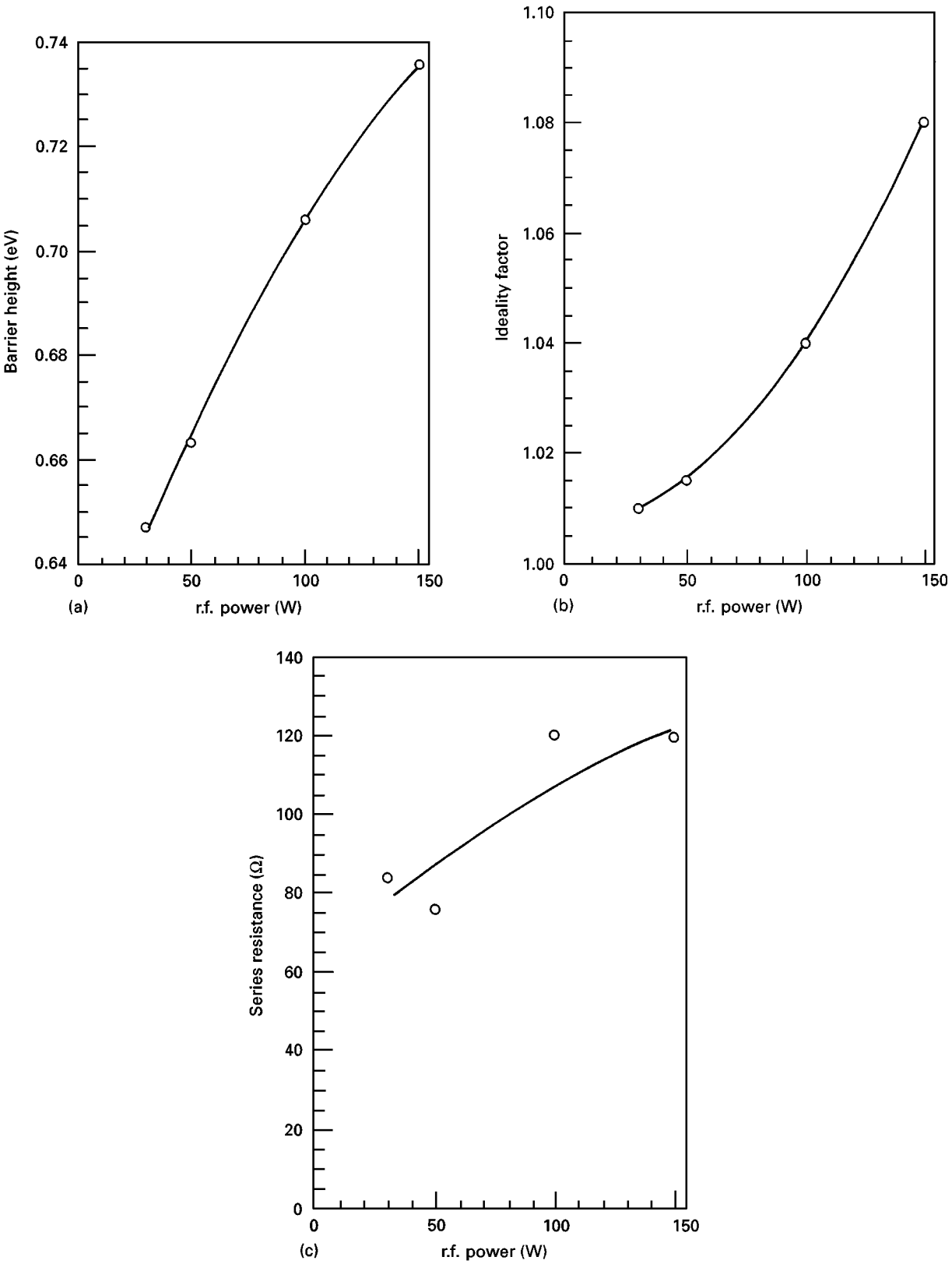

Figure 9 (a) Barrier height, (b) ideality factor, and (c) series resistance of ITO/p-type Si junctions where silicon substrates were subjected to reactive ion etching for 3 min at various powers.

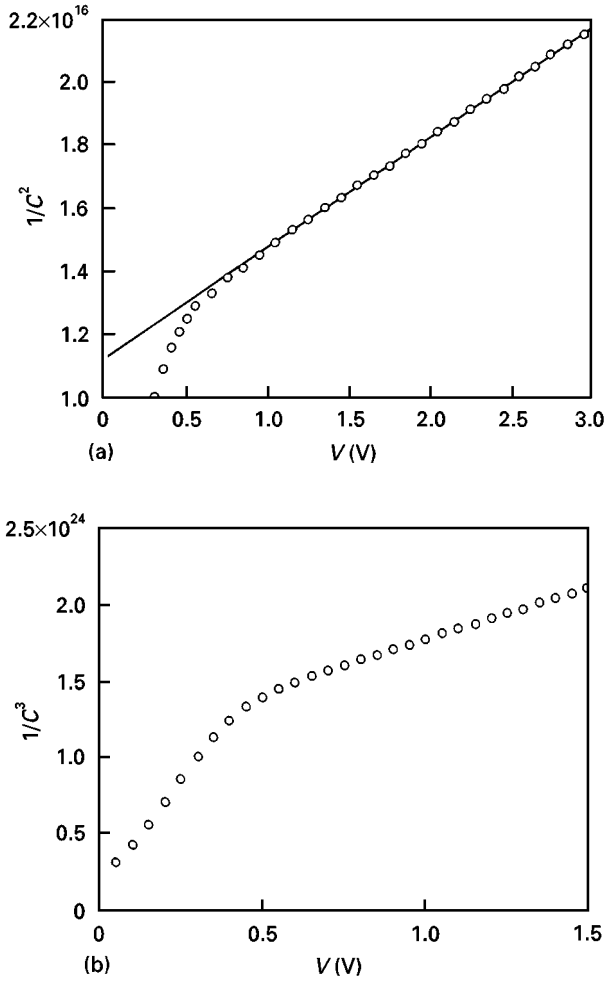

Figure 10 (a) $1/C^2$–V and (b) $1/C^3$–V characteristics of ITO/p-Si junction where Si substrate was subjected to reactive ion etching.

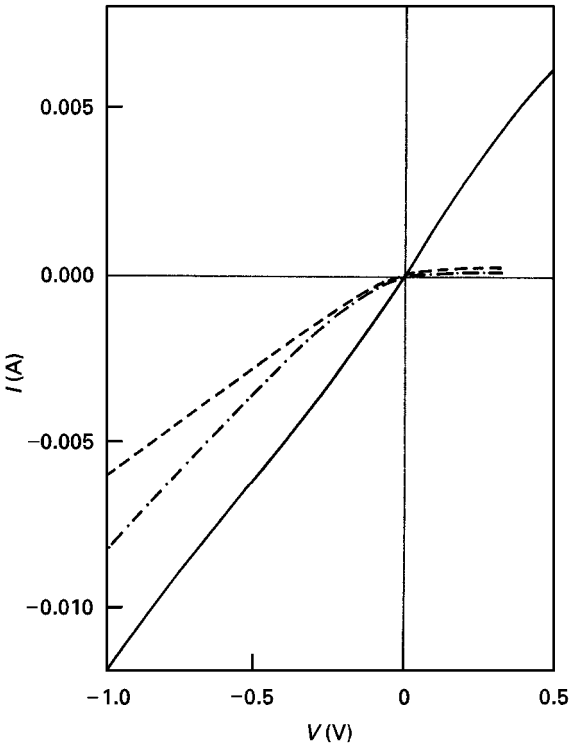

Figure 11 I–V curves of ITO/etched p-Si annealed in N_2 atmosphere at 300 °C for various times; (– – –) 10 min, (– · –) 20 min, (——) 1 h.

However, as shown in Fig. 10, a linear $1/C^2$ versus V plot is seen only for larger voltages, while $1/C^3$ versus V is more linear for smaller voltages. This suggests a quasi-linear-graded dopant profile.

On the basis of the I–V and C–V results, it is argued that the ion etching damage tends to increase the downward bending of the Si band edges adjacent to the interface and results in the increase of the interface barrier. Previous works by Ashok and co-workers [17–19] reported that ion beam damage gave rise to an increase of donor concentration in silicon. These donorlike defects might provide a positive charge layer at the interface which increased the barrier height of p-Si. This is possible if ion beam damage introduces defect levels which are positively charged. The rectifying nature of contacts on ion-etched Si is primarily due to the ion beam damage.

Since the surface properties of Si are degraded by dry etching, a thermal annealing treatment is employed to eliminate the damage. Fig. 11 gives the I–V curves of ITO/etched p-Si annealed in a N_2 atmosphere at 300 °C for various times. The contact becomes more ohmic for increasing sample annealing time. This suggests that annealing is effective in reducing the interface damage. After 300 °C annealing in N_2 for 1 h, most of the defects such as vacancies, divacancies, interstitial Si, vacancy-interstitial complexes and so on can migrate, dissociate, or otherwise disappear [20]. As shown in Figs 2–4, post-etching annealing reduces the concentrations of C, F, and O in the Si wafer, this confirms the removal of impurity defects after annealing.

4. Conclusions

1. Ion-beam etching of silicon roughens the Si surface. SIMS analysis indicates that elements of etching species C, F, and O penetrate into the Si substrate after reactive ion beam etching.
2. The I–V characteristics of ITO/p-Si junctions change from an ohmic contact for an unetched silicon substrate to a rectifying contact for silicon treated with RIE.
3. The barrier height, ideality factor, and series resistance increase with increasing etching power. It is argued that RIE of silicon increases the downward bending of the Si band edges adjacent to the surface and causes the rectifying behaviour.
4. I–V measurements show that annealing in N_2 at 300 °C for 1 h causes the ITO/p-Si junction to revert to ohmic behaviour. SIMS analysis indicates that post-etching annealing reduces the concentrations of C, F, and O in a silicon substrate. It is believed that annealing is effective in reducing the interface damage.

Appendix: The RCA cleaning process

1. Ultrasonic cleaning in trichloroethylene for 10 min.
2. Ultrasonic cleaning in acetone for 10 min.
3. Rinsing in deionized (DI) water for 5 min.
4. Boiling in H_2SO_4:H_2O = 3:1 for 10–20 min.
5. Rinsing in DI water for 5 min.

6. Dipping in $NH_4F:HF = 6:1$ for 10–20 s.
7. Rinsing in DI water for 5 min.
8. Boiling in $NH_4OH:H_2O_2:H_2O = 1:1:5$ for 10–20 min.
9. Rinsing in DI water for 5 min.
10. Boiling in $HCL:H_2O_2:H_2O = 1:1:6$ for 10–20 min.
11. Rinsing in DI water for 5 min.
12. Drying in a N_2 flow.

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