# Characterization of Polysilicon Oxides Thermally Grown and Deposited on the Polished Polysilicon Films

Tan Fu Lei, Juing-Yi Cheng, Shyh Yin Shiau, Tien Sheng Chao, *Member, IEEE*, and Chao Sung Lai

***Abstract*—This work examines the characteristics of polyoxides thermally grown and deposited on polished polysilicon films. A well-controlled chemical mechanical polishing (CMP) process is also presented to achieve a planar surface morphology for polysilicon films. The thermally-grown and deposited polyoxides on the polished polysilicon films exhibit a lower leakage current, higher dielectric breakdown field, higher electron barrier height, lower electron trapping rate, lower density of trapped charges, and markedly higher charge to breakdown ($Q_{\rm bd}$) than the conventional polyoxide. In particular, the deposited polyoxide on the polished polysilicon film has the highest dielectric breakdown field, lowest electron trapping rate, and highest charge to breakdown due to the planar polyoxide/polysilicon interface. In addition, experimental results indicate that the trapped charges of the polished samples are located in the polyoxides' upper portion, which differs from conventional polyoxides. Undoubtedly, the deposited polyoxide on the polished polysilicon film considered herein is the most promising candidate to yield optimum characteristics of polyoxide.**

## I. Introduction

DEVELOPING nonvolatile memories such as EPROM, EEPROM, and Flash EEPROM has received increasing interest [1]–[3]. For double-poly floating gate structure (EPROM or EEPROM), the polyoxides require a low leakage current and high breakdown electric field to obtain adequate data retention characteristics [1]–[3]. However, a nonuniform polyoxide film thickness and rough surface morphology of the polysilicon/polyoxide interface cause polyoxides to have a higher leakage current and lower dielectric breakdown field than those of silicon dioxide grown from a single crystalline silicon substrate [4]-[6]. This occurrence is attributed to local electric-field enhancement in rough polysilicon/polyoxide interface. Moreover, the surface roughness of polyoxide/polysilicon interface would be enhanced after thermal oxidation [6]–[8]. Therefore, how to reduce the roughness of polysilicon/polyoxide interface is a critical issue. To overcome this difficulty, the CVD oxide deposited on the polysilicon films (deposited polyoxide) is a highly attractive inter-polysilicon dielectric [8], [9]. Recently, chemical mechanical polishing (CMP) process has been used for planarization of multilevel interconnect [10], [11], polysilicon-filled trench isolation [12], and oxide-filled trench isolation [13]. CMP process, owing to its planarization properties, has also been used to improve the surface roughness of polysilicon film [14]. However, the insulating properties of polyoxide films thermally grown or deposited on polished polysilicon films have been paid scarce attention [15].

Manuscript received March 21, 1997; revised October 20, 1997. The review of this paper was arranged by Editor C.-Y. Lu. This work was supported by National Science Council of the R.O.C. under Contract NSC 85-2215-E009-051.

T. F. Lei, J.-Y. Cheng, S. Y. Shiau, and C. S. Lai are with the Department of Electronics Engineering Institute of Electronics, National Chiao-Tung University, Hsinchu 30050, Taiwan, R.O.C.

T. S. Chao is with the National Nano Device Laboratory, Hsinchu 30050, Taiwan, R.O.C.

Publisher Item Identifier S 0018-9383(98)02293-X.

This study utilizes a well-controlled CMP process to improve the surface roughness of polysilicon films. Polyoxides are then thermally grown or deposited on them. This work focuses on characterizing thermally-grown polyoxides (TPO) on polished (TPOP)/unpolished (TPOU) polysilicon films and deposited polyoxides (DPO) on polished (DPOP)/unpolished (DPOU) polysilicon films. The removal rate of polysilicon based on a CMP process and the surface morphology of polysilicon films before and after a CMP process are presented. Moreover, the electrical properties of thermally-grown and deposited polyoxides on polished/unpolished polysilicon films are investigated as well.

## II. Experimental

Herein, the removal rate of polysilicon film was evaluated by depositing a 600-nm thick polysilicon layer by low pressure chemical vapor deposition (LPCVD) at 625 °C on a 100-nm thick silicon dioxide layer grown on 6-in p-type (100) silicon wafers by wet oxidation at 980 °C. The polishing slurry (CABOT SC-1) used in this experiment is colloidal silica in an aqueous KOH solution with PH $\sim$ 10.0. The silica particles are uniform in size and the mean particle diameter is 30 nm. The polishing pad is a microporous polyurethane material and the hardness of pad is $52 \sim 62$ Shore D. The flow rate of slurry was 200 ml/min, the plate temperature was set at 37 °C, and the speeds of the polishing plate and wafer carrier were set at 20 and 42 r/min, respectively. Moreover, a pad-conditioning with back pressure of 0.3 psi and speed of 30 r/min was performed prior to CMP.

Following evaluation of the removal rate, $n^+$-polysilicon/polyoxide/$n^+$-polysilicon capacitors were fabricated. Initially, a 200-nm thick silicon dioxide layer was thermally grown on the p-type (100) silicon wafers by wet oxidation at 980 °C. 300-nm thick polysilicon layer (poly-1) was then deposited at 620 °C and doped with $POCl_3$

0018–9383/98$10.00 © 1998 IEEE

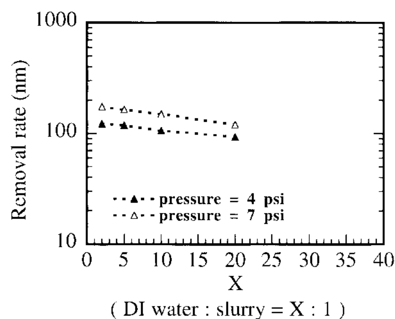


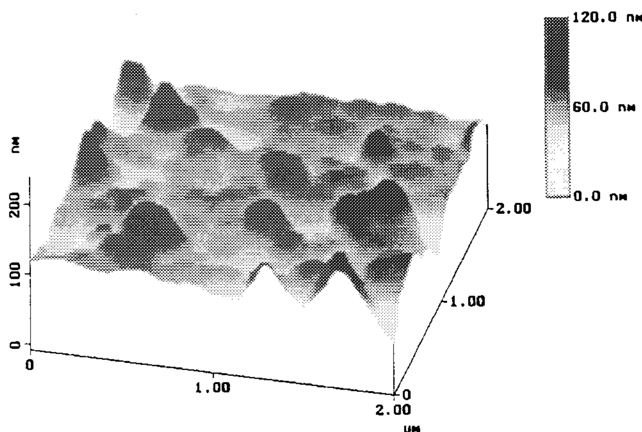

Fig. 1. The removal rates of polysilicon films.

at 950 °C to obtain a sheet resistance of 25 $\Omega/\square$. Next, the poly-1 was polished by a CMP process at 4 psi with a dilute 20:1 slurry for 25 s to improve the surface roughness. After the CMP process, to remove the slurry's particles and metallic contamination, wafers were first cleaned at second plate with a DI water and, then, oscillated by megasonic cleaning equipment with a dilute 50:1 ammonia solution. Next, an additional RCA clean process was performed. The RCA clean process was performed again in the other clean bench and, then, the polyoxides were thermally grown on polished (TPOP) and unpolished (TPOU) polysilicon films simultaneously by dry oxidation at 900 °C. However, the deposited polyoxides were simultaneously deposited on polished (DPOP) and unpolished (DPOU) polysilicon films by a LPCVD system at 700 °C. Subsequently, a second 300-nm thick polysilicon layer (poly-2) was deposited at 620 °C and doped at 950 °C. After the poly-2 was defined, a 100-nm thick oxide was grown on the samples by wet oxidation as passivation layers. Contact holes were opened, and Al was deposited and patterned to form capacitors. Finally, all devices were sintered at 350 °C for 30 min in a $N_2$ ambient.

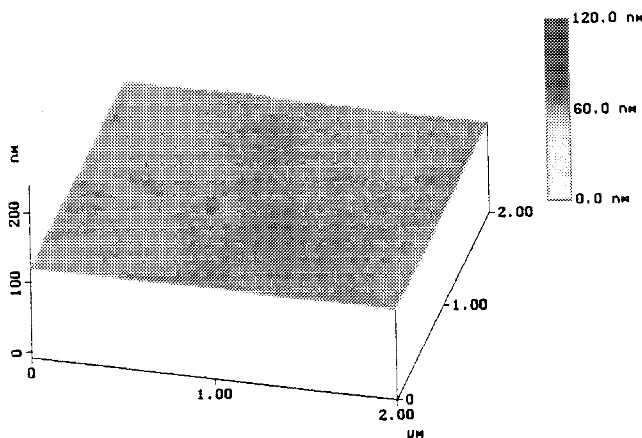
Atomic force microscope (AFM) was used to assess the surface morphology of polysilicon films before and after CMP process. Polyoxides thicknesses were obtained by C-V measurement. For electrically characterizing the polyoxide layer, the $I-V$ characteristics, the charge-to-breakdown ($Q_{\rm bd}$), and the effective electron barrier height ($\phi_b$) were measured by a HP4145B semiconductor parameter analyzer. Also, the electron trapping rate and the centroids of trapped charges of polyoxides were measured by a HP4145B system.

## III. Results and Discussion

Fig. 1 shows the removal rates of polysilicon with pressures of 4 psi (27.2 kPa) and 7 psi (47.6 kPa). According to this figure, the various ratios of water/slurry are used. Obviously, a higher applied pressure implies a higher removal rate [16]. In addition, it is also clear that the extrapolated rate at zero pressure exceeds zero. This phenomenon implies that a large chemical component of polysilicon removal during CMP. For controllability, a low and appropriate removal rate is deemed necessary. Therefore, in this work, we perform surface planarization of the polysilicon films based on a CMP process at the applied pressure of 4 psi with a dilute 20:1 slurry for 25 s where the removal rate was 93 nm/min.




(a)




(b)

Fig. 2. The surface images of the polysilicon films (a) before and (b) after a CMP process.

Fig. 2(a) and (b) displays the surface images of the polysilicon films before and after a CMP process, respectively. Clearly, the surface morphology of the polished polysilicon film (surface roughness $\sim$9 Å) is markedly smoother than that of the unpolished polysilicon film (surface roughness $\sim$90 Å). Therefore, the CMP process is highly attractive for improving the surface morphology of the polysilicon film owing to its planarization properties.

For polished samples and unpolished samples, Fig. 3 presents the growth curves of thermally-grown polyoxides (TPOP/TPOU) and deposited polyoxides (DPOP/DPOU). Theoretically, TPOP's thickness should be nearly the same as that of the TPOU for the same oxidation time due to their simultaneous oxidation. Simultaneously, DPOP's thickness should be nearly the same as that of the DPOU for the same deposition time. However, C-V measurements reveal that TPOU's capacitance exceeds that of the TPOP; in addition, DPOU's capacitance exceeds that of the DPOP. For all samples in this work, the effective thickness ($T_{\rm ox}$) is obtained by using $T_{\rm ox} = \epsilon_{\rm ox}/C$ where $\epsilon_{\rm ox}$ is the dielectric constant of polyoxide and $C$ represents the capacitance per unit area. Therefore, an unpolished sample having a thinner effective thickness is obtained for thermally-grown or deposited polyoxides due to a rougher surface. However,

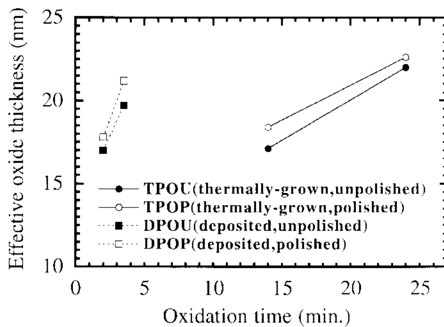
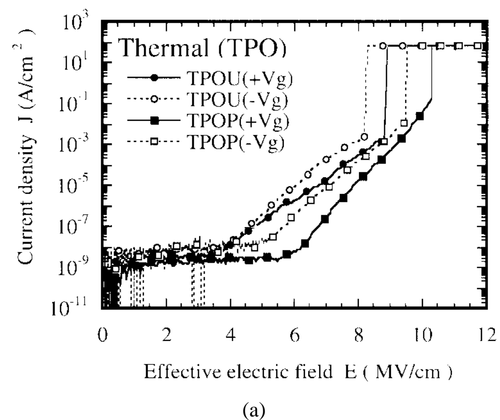



Fig. 3. The growth curves of thermally-grown polyoxides (TPOP/TPOU) and deposited polyoxides (DPOP/DPOU).

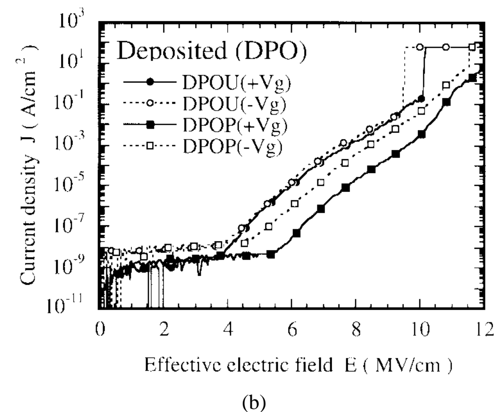
although the surface morphology is so different between the polished and unpolished samples, the effective thickness of the unpolished sample is only slightly smaller than that of the polished sample. This phenomenon is possible owing to that the growth rate of polyoxide on a rough surface is slightly larger than that on a smooth surface. Therefore, the influence of surface roughness on effective thickness is reduced.

As Fig. 4(a) and (b) reveal, the typical J-E characteristics of around 220-Å thick thermally-grown polyoxides and 200-Å thick deposited polyoxides are labeled TPO and DPO, respectively. For all samples in this work, the electric field $(E_{\text{ox}})$ is obtained by using $E_{\text{ox}} = V_{\text{ox}}/T_{\text{ox}}$ where $V_{\text{ox}}$ denotes the applied voltage and $T_{\text{ox}}$ represents the effective oxide thickness, as determined by the C-V measurement. Obviously, for both thermally-grown and deposited polyoxides, the polished sample has a lower leakage current and a higher breakdown electric field than in the case of the unpolished sample when poly-2 is positively-biased $(+V_g)$, where electrons are injected from the polyoxide/poly-1 interface. This phenomenon is owing to that the electric field at the injected interface of the polished sample is more approximate to the average applied field than that of the unpolished sample. Consequently, a smoother surface of the poly-1 leads to a smaller localized current density and better uniformity of localized electric field. Furthermore, the polished sample (TPOP or DPOP) also has a higher current density at dielectric breakdown. For both the polished and unpolished samples, polyoxides exhibit a higher conductance and a lower dielectric breakdown field when poly-2 is negatively-biased $(-V_g)$ than when poly-2 is positively-biased $(+V_g)$. This finding implies that a superior polyoxide/poly-1 interface exists. In addition, for both polished samples (TPOP and DPOP), the thermally-grown polyoxide has a lower breakdown electric field than the deposited polyoxide. Such a discrepancy is owing to that the surface roughness is enhanced during thermal oxidation and/or that the incorporated phosphorous results in traps in the polyoxide [6]–[8], [17], [18].

As Fig. 5 indicates, for both thermally-grown and deposited polyoxides, the effective barrier height of the polished sample at $+V_g$ and $-V_g$ biases exceeds that of the unpolished sample. Therefore, the polyoxides thermally grown or deposited on a smoother surface of polysilicon films have larger effective barrier heights due to a smaller localized electric field. Moreover, for both the polished samples and unpolished samples,




(a)




(b)

Fig. 4. The typical J-E characteristics of about (a) thermally-grown polyoxides (TPO) and (b) deposited polyoxides (DPO).

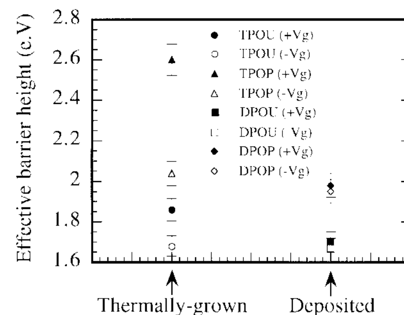



Fig. 5. The effective barrier heights of thermally-grown polyoxides (TPO) and deposited polyoxides (DPO).

the effective barrier heights at $+V_g$ bias exceed those at $-V_g$ bias. This finding suggests that the polyoxide/poly-1 interface is smoother than the poly-2/polyoxide interface.

Fig. 6(a) and (b) depicts the charge trapping characteristics of thermally-grown and deposited polyoxides, respectively. Obviously, the gate voltage shifts of the polished and unpolished samples increase with time at $+V_g$ and $-V_g$ constant current stresses where the capacitor area is $6.2 \times 10^{-4}$ cm$^{-2}$. The stress conditions are 1 mA/cm$^2$ for thermally-grown polyoxides and 10 mA/cm$^2$ for deposited polyoxides. These figures also reveal that the polished sample has a smaller voltage shift than the unpolished sample. This finding implies that the polished sample traps fewer electrons and has a lower electron

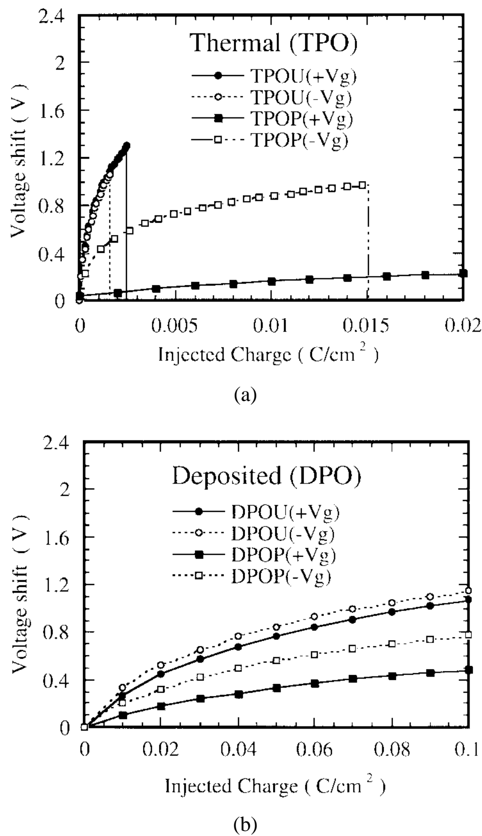



Fig. 6. The charge trapping characteristics of (a) thermally-grown polyoxides (TPO) and (b) deposited polyoxides (DPO).

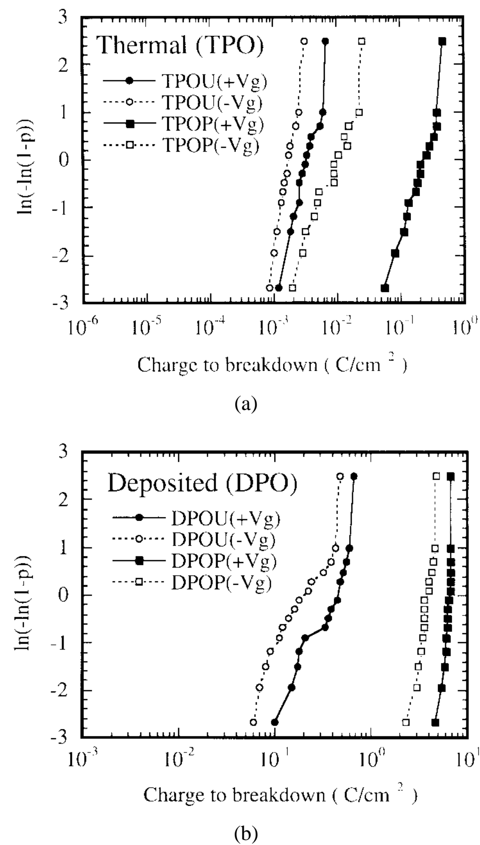



Fig. 7. The charge-to-breakdown ($Q_{\rm bd}$) of (a) thermally-grown polyoxides (TPO) and (b) deposited polyoxides (DPO).

trapping rate than the unpolished sample. Related, the rougher polyoxide/polysilicon interface leads to a smaller conduction area and a higher local current density, subsequently causing a higher electron trapping rate. According to Fig. 6(a) and (b), the thermally-grown polyoxides have a higher electron trapping rate than the deposited polyoxides. This discrepancy is owing to that the incorporated phosphorous results in traps in the oxide and/or the roughness of polyoxide/poly-1 interface is enhanced during thermal oxidation, resulting in a higher local current density, as mentioned earlier.Although the experimental data is based on different stress conditions for thermally-grown and deposited polyoxides (1 mA/cm$^2$ and 10 mA/cm$^2$, respectively), a layer stress current density implies a largert stress electric field.Therefore, deposited polyoxides should exhibit better characteristics if the stress condition is 1 mA/cm$^2$.

In nonvolatile memory cells, the charge-to-breakdown ($Q_{\rm bd}$) is also a critical parameter of interest. Fig. 7(a) and (b) displays the Weibull plots of the charge-to-breakdown for the unpolished samples and polished samples at 1 mA/cm$^2$ stress of TPO's and 10 mA/cm$^2$ stress of DPO's, respectively. According to Fig. 7(a) and (b), the polished sample has a significantly larger $Q_{\rm bd}$ than the unpolished sample. The significantly larger charge-to-breakdown of the polished sample is due to the lower electron trapping rate, as Fig. 6(a) and (b) depict. Moreover, according to Fig. 7(a) and (b), the Qbd's of the thermally-grown polyoxides are markedly smaller than those of the deposited polyoxides. This smaller value is owing to that enhancing the surface roughness of the polyoxide/poly-1 interface during thermal oxidation and/or incorporating phosphorous produce a higher electron trapping rate.

A previous work investigated the centroids of trapped charges ($Xt$) and trapped charge density ($Q_t$) in the polyoxides [19]. By the bidirectional $I-V$ measurement and by the shifts of F-N $I-V$ characteristics before and after stress for both polarities, the effective trapped charge density is calculated from

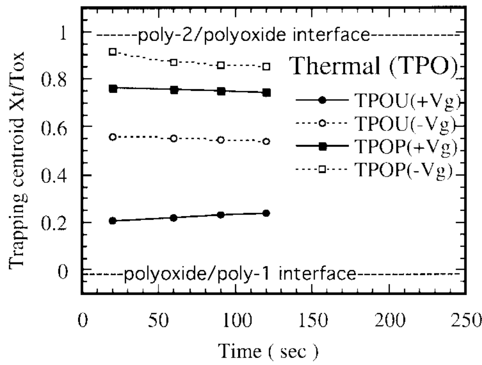
$$Qt = \epsilon_{\rm ox}(\Delta Vg- + \Delta Vg+)/T_{\rm ox} \qquad (1)$$

and the centroids of the trapped charges are calculated from

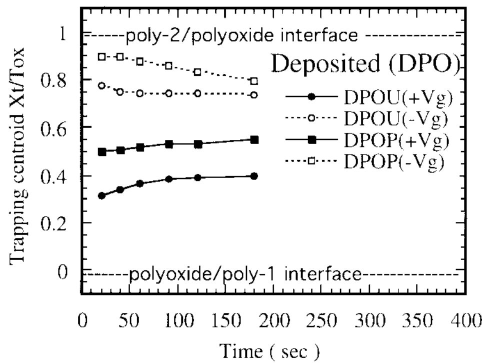
$$Xt = T_{\rm ox}[1 + (\Delta Vg-/\Delta Vg+)]^{-1} \qquad (2)$$

where $Xt$ is measured from the poly-2/polyoxide interface; $\Delta Vg+$ denotes the voltage shift when poly-2 is positively biased; $\Delta Vg-$ represents the voltage shift when poly-2 is negatively biased; and $T_{\rm ox}$ is the polyoxide thickness and $\epsilon_{\rm ox}$ is the dielectric constant of polyoxide.

Moreover, to avert the possible re-emission of trapped charges, we calculate the $\Delta Vg+$ and $\Delta Vg-$ from the shifts of the linear portion of $I-V$ curves at the current level of 1.61 $\mu$A/cm$^2$, i.e., 12.4 times smaller than that of the injection current (20 $\mu$A/cm$^2$) for the thermally-grown polyoxides and 62 times smaller than that of the injection current (100 $\mu$A/cm$^2$) for the deposited polyoxides. Fig. 8(a) and

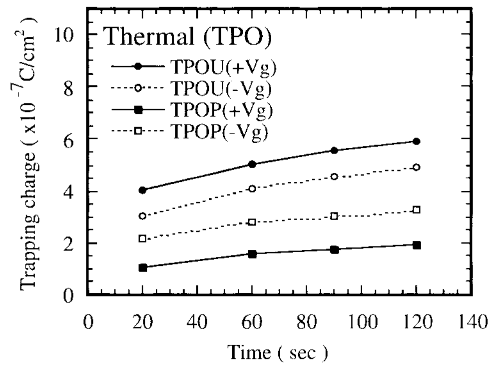



(a)

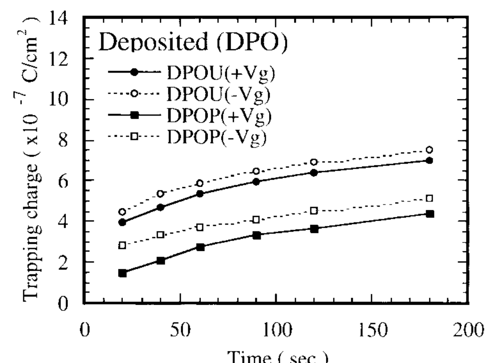



(b)

Fig. 8. The centroids of trapped charges $(Xt)$ of (a) thermally-grown polyoxides (TPO) and (b) deposited polyoxides (DPO) at various $+Vg$ and $-Vg$ injection times.




(a)




(b)

Fig. 9. Trapped-charge densities of (a) thermally-grown polyoxides (TPO) and (b) deposited polyoxides (DPO) at $+Vg$ and $-Vg$ constant current injection.

(b) presents the centroids of trapped charges $(Xt)$ at various $+Vg$ and $-Vg$ injection times for thermally-grown and deposited polyoxides, respectively. For both thermally-grown and deposited polyoxides at $+Vg$ and $-Vg$ constant current injection, the $Xt$ of the unpolished sample is closer to the polyoxide/poly-1 interface than that of the polished sample. This phenomenon is owing to that the surface morphology of polished polysilicon film (poly-1) is much smoother than that of unpolished polysilicon film, therefore, centroids move away from the polyoxide/poly-1 interface.

Fig. 9(a) and (b) depicts the trapped-charge densities of thermally-grown and deposited polyoxides at $+Vg$ and $-Vg$ constant current injection, respectively. Clearly, for both thermally-grown and deposited polyoxides, the trapped-charge density in the polished sample is less than that in the unpolished sample. This finding suggests that the electron trap generation rate and trapping rate are reduced in the polished sample. As Fig. 9(a) reveals, for the polarity dependence of trapping characteristics of thermally-grown polyoxides, the electron trapped-charge density at $-Vg$ constant current injection exceeds that at $+Vg$ constant current injection for the polished sample. Such a discrepancy may be attributed to that the surface of the polyoxide/poly-1 interface is smoother than that of the poly-2/polyoxide interface. Subsequently, the electron trapping rate is reduced at $+Vg$ constant current injection, as shown in Fig. 6(a). Moreover, for the unpolished sample, the electron trapped-charge density at $+Vg$ constant current injection exceeds that at $-Vg$ constant current injection. This phenomenon is owing to that the electron trapping rate at $+Vg$ constant current injection exceeds that at $-Vg$ constant current injection. Moreover, Fig. 9(b) confirms that the electron trapped-charge density at $-Vg$ constant current injection exceeds that at $+Vg$ constant current injection for the deposited polyoxieds. This difference is attributed to the superior polyoxide/poly-1 interface as described about Figs. 6(b) and 8(b). Therefore, the localized current and field at $+Vg$ injection are reduced, thereby causing less trapped charges to be generated.

## IV. Conclusions

This work presents a well-controlled CMP process to improve the surface roughness of polysilicon films. Both thermally-grown and deposited polyoxides on the polished polysilicon films exhibit a lower leakage current, higher dielectric breakdown field, higher electron barrier height, lower electron trapping rate, lower density of trapped charges, and much higher charge to breakdown $(Q_{\rm bd})$ than the conventional polyoxide. In particular, the deposited polyoxide on the polished polysilicon film has the highest dielectric breakdown field, lowest electron trapping rate, and highest charge to breakdown. In addition, the trapped charges of the polished samples are located in the upper portion of polyoxides, which differs from the conventional polyoxides. Undoubtedly, the proposed process is the most promising alternative to yield good characteristics of polyoxide.

## ACKNOWLEDGMENT

Dr. B. T. Dai is acknowledged for valuable discussions.

## REFERENCES

[1] C. Cobianu, O. Popa, and D. Dascalu, "On the electrical conduction in the dielectric layers," *IEEE Electron Device Lett.,* vol. 14, p. 213, 1993.
[2] T. Ono, T. Mori, T. Ajioka, and T. Takayashiki, "Studies of thin poly-Si oxides for E and $E^2$PROM," in *IEDM Tech. Dig.,* 1985, pp. 380–383.
[3] J. C. Lee and C. Hu, "Polarity asymmetry of oxides grown on polycrystalline silicon," *IEEE Trans. Electron Devices,* vol. 35, p. 1063, July 1988.
[4] C. S. Lai, T. F. Lei, and C. L. Lee, "The characteristics of polysilicon oxide grown in pure $N_2O$," *IEEE Trans. Electron Devices,* vol. 43, pp. 1–6, Feb. 1996
[5] L. Faraone and G. Harbeke, "Surface roughness and electrical conduction of oxide/polysilicon interfaces," *J. Electrochem. Soc.,* vol. 133, no. 7, p. 1410, 1986.
[6] M. C. Jun, Y. S. Kim, and M. K. Han, "Polycrystalline silicon oxidation method improving surface roughness at the oxide/polycrystalline silicon interface," *Appl. Phys. Lett.,* vol. 66, no. 17, p. 2206, 1995.
[7] L. Faraone, "Thermal $SiO_2$ films on $n^+$ polycrystalline silicon: Electrical conduction and breakdown," *IEEE Trans. Electron Devices,* vol. ED-33 p. 1785–1794, Nov. 1986.
[8] L. Faraone, R. D. Vibronek, and J. T. Mcginn," Characterization of thermally oxidized $n^+$ polycrystalline silicon," *IEEE Trans. Electron Devices,* vol. ED-32, pp. 577–584, Mar. 1985.
[9] S. Mori, T. Matsuda, T. Yanase, Y. Mikata, M. Sato, K. Shinada, K. Yoshikawa, and H. Nozawa, "Reliable CVD inter-poly dielectrics for advanced E and EEPROM," in *VLSI Symp. Dig. Tech. Papers,* 1985, p. 16.
[10] S. Sivaram, H. Bath, R. Leggett, A. Maury, K. Monnig, and R. Tolles, "Planarization interlevel dielectrics by chemical-mechanical polish," *Solid State Technol.,* pp. 87–91, May, 1992.
[11] C. Y. Chang and S. M. Sze, *ULSI Technology.* New York: McGraw-Hill, 1996, pp. 433–445.
[12] I. Ali, M. Rodder, S. R. Roy, G. Shinn, and M. I. Raja," Physical characterization of chemical mechanical planarized surface for trench isolation," *J. Electrochem. Soc.,* vol. 142, no. 9, pp. 3088–3092, 1995.
[13] P. C. Fazan and V. K. Mathews, "A highly manufacturable trench isolation process for deep submicron DRAM's," *in IEDM Tech. Dig.,* 1993, pp. 57–60.
[14] C. Y. Chang, H. Y. Lin, T. F. Lei, J. Y. Cheng, L. P. Chen, and B. T. Dai, "Fabrication of thin film transistors by chemical mechanical polished polycrystalline silicon films," *IEEE Electron Device Lett.,* vol. 17, p. 100, 1996.
[15] T. F. Lei, J. Y. Cheng, S. Y. Shiau, T. S. Chao, and C. S. Lai, "Improvement of polysilicon oxide by growing on polished polysilicon film," *IEEE Electron Device Lett.,* vol. 18, pp. 270–271, June 1997
[16] J. Y. Cheng, T. F. Lei, and T. S. Chao, "A novel planarization of trench isolation using polysilicon refill and etchback of chemical-mechanical polish," *J. Electrochem. Soc.,* vol. 142, no. 10, pp. L187–L188, 1995.
[17] S. Mori, N. Arai, Y. Kaneko, and K. Yoshikawa," Polyoxide thinning limitation and superior ONO interpoly dielectric for nonvolatile memory devices," *IEEE Trans. Electron Devices,* vol. 38, pp. 270–277, Feb. 1991.
[18] Y. Mikada, S. Mori, K. Shinada, and T. Usami," Low leakage current polysilicon oxide grown by two-step oxidation," in *IEEE IRPS,* 1985, pp. 32–38.
[19] E. Ave, O. Abramson, Y. Sonnenblick, and J. Shappir," Charge trapping in oxide grown on polycrystalline silicon layers," *J. Electrochem. Soc.,* vol. 135, no. 1, pp. 182–186, 1988.

**Tan Fu Lei** was born in Keelung, Taiwan, R.O.C., on September 17, 1944. He received the B.S. degree in electrical engineering from National Chung Keng University, Tainan, Taiwan, in 1967, and the M.S. and Ph.D. degrees in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1970 and 1979, respectively.

From 1970 to 1979, he was with the Fine Producrs Microelectronics Corporation, Taiwan, as an Engineer working on the fabrication of small-signal transistors. From 1980 to 1982, he was the Plant Manager, Photronic Corporation, Taiwan. In 1983, he joined the faculty of National Chiao-Tung University as an Associate Professor in the Department of Electronics Engineering and the Insititute of Electronics. From 1984 to 1986, he was Director of the Semiconductor Research Center. Presently, he is a Professor in that department and the Associate Director of the National Nano Device Laboratory, Hsinchu. His research interests are in semiconductor devices and optoelectronics.

**Juing-Yi Cheng**, photograph and biography not available at the time of publication.

**Shyh Yin Shiau**, photograph and biography not available at the time of publication.

**Tien Sheng Chao** (M'93) was born in Penghu, Taiwan, R.O.C., in 1963. He received the B.S., M.S., and Ph.D. degrees, all in electronic engineering, from National Chiao-Tung University, Hsinchu, Taiwan, in 1985, 1988, and 1992, respectively.

He joined the National Nano Device Laboratory, Hsinchu, as an Associate Researcher in July 1992. He was engaged in developing the ellipsometric measurement on thin films for semiconductor processes. Currently, he is responsible for the development of thin dielectrics and isolation for integrated circuits.

**Chao Sung Lai** was born in I-Lan, Taiwan, R.O.C., on May 20, 1969. He received the B.S. degree in electronics engineering in 1991, from National Chiao-Tung University, Hsinchu, Taiwan, where he is currently pursuing the Ph.D. degree in the Department of Electronics Engineering. His research focuses on the characteristics and reliability of MOSFET's, nitrided thin gate dielectrics, nitrided interpoly dieletrics, and the modeling of dielectrics' reliability.