Low-Resistance Vertical Conduction Across Epitaxially Lifted-Off n-GaAs Film and Pd/Ge/Pd Coated Si Substrate

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Low-resistance ohmic conduction across an epitaxially lifted-off (ELO) thin n-GaAs film and a Si substrate was obtained by attaching the ELO film on the Si substrate coated with a Pd/Ge/Pd multilayer. Good bonding and ohmic contacts to both GaAs and Si were achieved at the same time after annealing. The interface compound formation was studied by secondary ion mass spectroscopy and x-ray diffraction analyses. This ELO technology was used to fabricate an ELO stripe geometry diode laser on Si with the back-side contact on Si substrate. Good laser performance with comparable characteristics as conventional laser diodes on GaAs substrates was obtained.

Key words: Epitaxial lift-off (ELO) method, laser diode, n-type GaAs

INTRODUCTION

Bonding III-V semiconductor thin films with Si substrates using the epitaxially lifted-off (ELO) technique has been a subject of great interest in recent years.[1] Because the lifted-off films are usually very thin, the III-V devices can be more easily integrated with Si devices using this technique than using other wafer bonding methods. To date, a number of devices such as solar cells, light emitting diodes (LEDs), laser diodes, heterojunction bipolar transistors (HBTs), metal semiconductor field-effect transistors (MESFETs), and high electron mobility transistors (HEMTs) have been fabricated on Si substrates using this technique.[2–7] However, the ELO technique relies on Van der Waals bonding between the film and the substrate. It often suffers from poor mechanical and electrical properties. To improve bonding, Yablonovitch et al. and Fathollahnejad et al. used Pd[8] or Pd/Ge[9] coated Si substrates and good bonding was formed between the GaAs thin film and the substrate after annealing. The metal layer also provided good ohmic contact to the GaAs layer.[8,9] For all approaches mentioned above, however, the vertical conduction between the III-V semiconductor film and the Si substrate was poor. A good conduction between the two would greatly simplify the wiring requirement and the integration process. So, in this study, we set out to investigate a metal structure that can be used in the ELO process to provide ohmic contact to both the lifted-off GaAs thin film and the Si substrate.

It has been reported that Pd/Ge can penetrate the surface native oxide of GaAs during annealing and provides low-stress ohmic contact to GaAs.[10] On the other hand, palladium silicide makes a good ohmic contact to Si.[11,12] The silicide contact is shallow and smooth and does not cause spiking behavior which is commonly seen with aluminum contacts. So, a Pd/Ge/Pd metallic structure is used in this study. The electrical behavior of the interface between the GaAs film and the Si substrate was examined by the current-voltage (I-V) measurement at various temperatures. Secondary ion mass spectrometry (SIMS) and x-ray diffraction (XRD) analyses were used to study the interface compound and the formation of the metallurgical bonding. Finally, we fabricated an ELO strip-geometry diode laser on n^+-Si substrate with the back side contact on Si to demonstrate the feasibility of this technique.

EXPERIMENTS

The GaAs film, which was to be lifted off, was grown by molecular beam epitaxy (MBE). The layer was 1 μm thick with a Si doping of 2×10^{18} cm^{-3} and was grown on top of a 100Å thick AlAs sacrificial layer. Rectangular 500×350 μm^2 mesa structures with a

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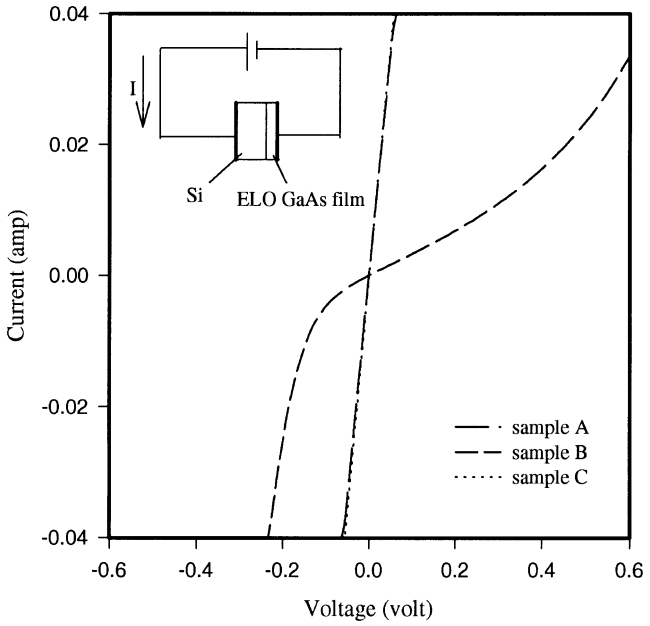

Fig. 1. Current-voltage (I-V) characteristics of samples A, B, and C. Low-resistance ohmic conduction is observed for samples A and C, whereas non-ohmic behavior is observed for sample B.

Table I. Structure of Metallic Multilayers Between ELO n-GaAs Film and Si Substrate and the Series Resistance Measured from I-V Curves

Sple.	Substrate	Metallic Structure	Series Resistance (Ω)
A	GaAs		1.47
B	(100)n^+Si	1000Å Pd/1250Å Ge	rectification
C	(100)n^+Si	1000Å Pd/ 1250Å Ge/2500Å Pd	1.4

6000Å etched depth were formed. Au-Ge contact with dimensions of 120×120 μm^2 was then defined on the mesa top. The samples were annealed by rapid thermal annealing (RTA) at 400°C for 10 s. The samples were then covered with Apiezon W black wax, which was used to protect the samples surface and provide mechanical support in later processes.[1] A (100) n^+-Si substrate with a resistivity of 0.01-1 Ω-cm was used as the host substrate in the ELO process. Multilayer metal structures of Pd(1000Å)/Ge(1250Å) and Pd(1000Å)/Ge(1250Å)/Pd(2500Å) were deposited on separate Si substrates by an electron-gun deposition system under a base pressure $<8 \times 10^{-7}$ Torr. The metal coated Si substrates were dipped in dilute HCl solution before being attached with the ELO film. The GaAs film was lifted from the substrate by soaking in dilute HF solution. Before the bonding process, the preprocessed n-GaAs film with black wax was dipped in HCl and HF. Then the GaAs film and the Si substrate were bonded together by Van der Waals bonding. A proper pressure was applied on these samples to squeeze out the deionized (DI) water at the interface. After the bonding process, the black wax

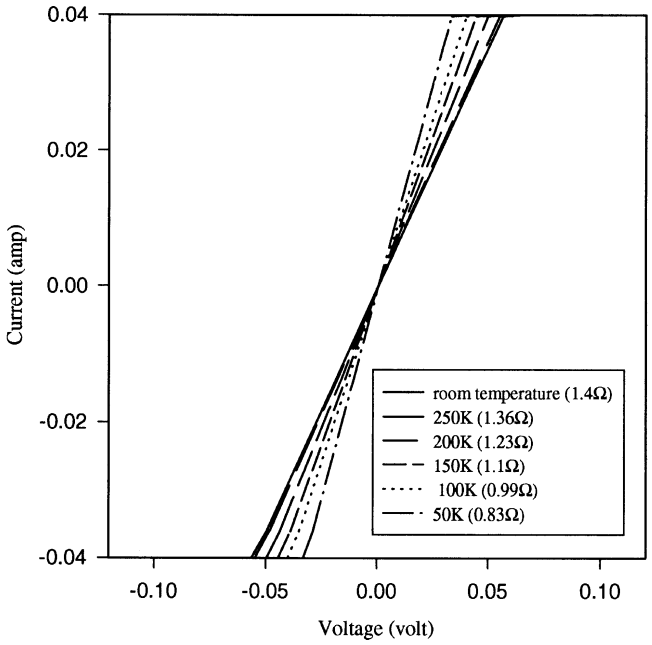

Fig. 2. I-V characteristics of sample C at various temperatures.

was removed and then a 4000Å Al layer was evaporated on the back of the Si substrate for ohmic contact. The samples were then annealed at 400°C for 30 min under a forming gas ambient. This annealing procedure caused the formation of metallurgical bonding between the grafted film and the Si substrate and at the same time sintering of the backside Al contact. These samples were diced into ~5×5 mm^2 for electrical measurement.

RESULTS AND DISCUSSION

Electrical Characterization

For I-V measurement, three different samples were used. Sample A was the reference sample with the GaAs film on GaAs substrate without being lifted off. For samples B and C, Pd/Ge and Pd/Ge/Pd were used as the bonding agents, respectively, in the bonding process. Figure 1 shows the I-V curves measured at room temperature for samples A, B, and C. While samples A and C show good vertical conduction, sample B is non-ohmic. The series resistance of the three samples are shown in Table I. The resistance for the sample with Pd/Ge/Pd interlayer is comparable to that of the reference sample. So an additional layer of Pd between Pd/Ge and Si causes the formation of ohmic contact to Si. Since the bonding and the contact formation are caused by the Pd/Ge/Pd metal layer, the I-V characteristics are independent of crystal orientation. No precise alignment between the ELO film and the host substrate is needed. Figure 2 shows the temperature dependence of the vertical conduction behavior. Good ohmic behavior is maintained even for temperatures as low as 50K.

Material Structural Characterization

The interface reaction between the Pd/Ge/Pd layer

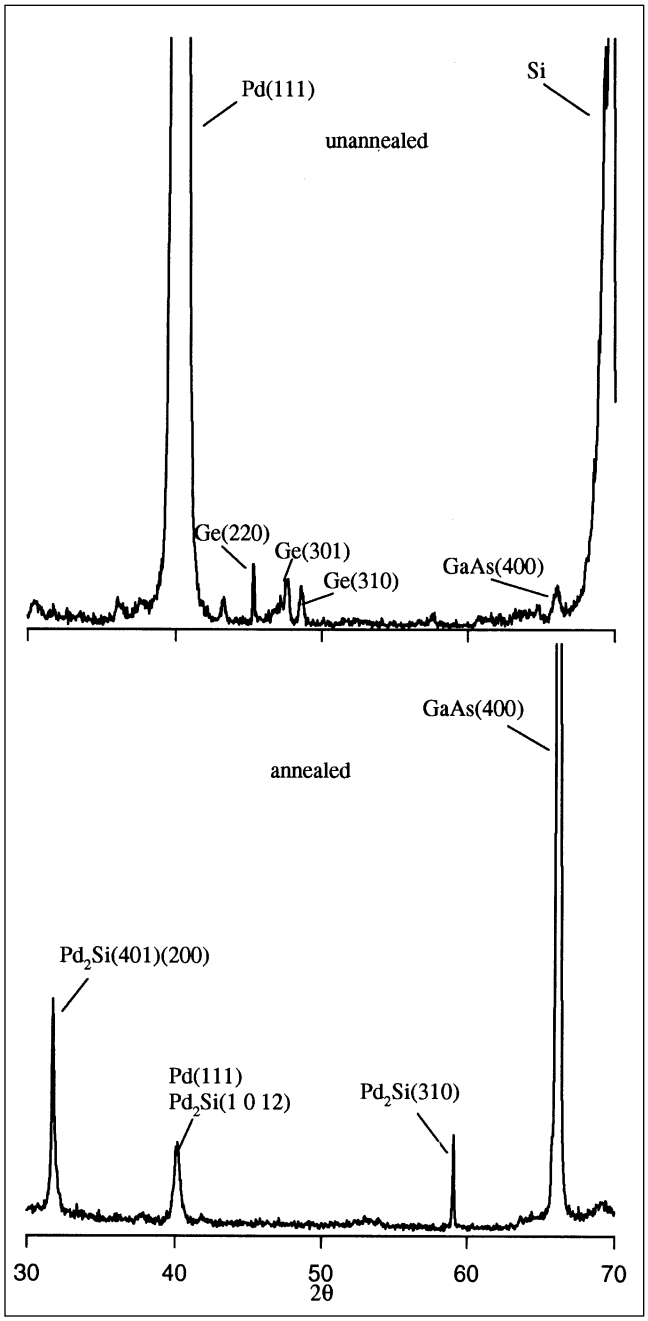

Fig. 3. XRD patterns of an ELO n-GaAs/Pd/Ge/Pd/n$^+$-Si sample before and after 400°C, 30 min annealing.

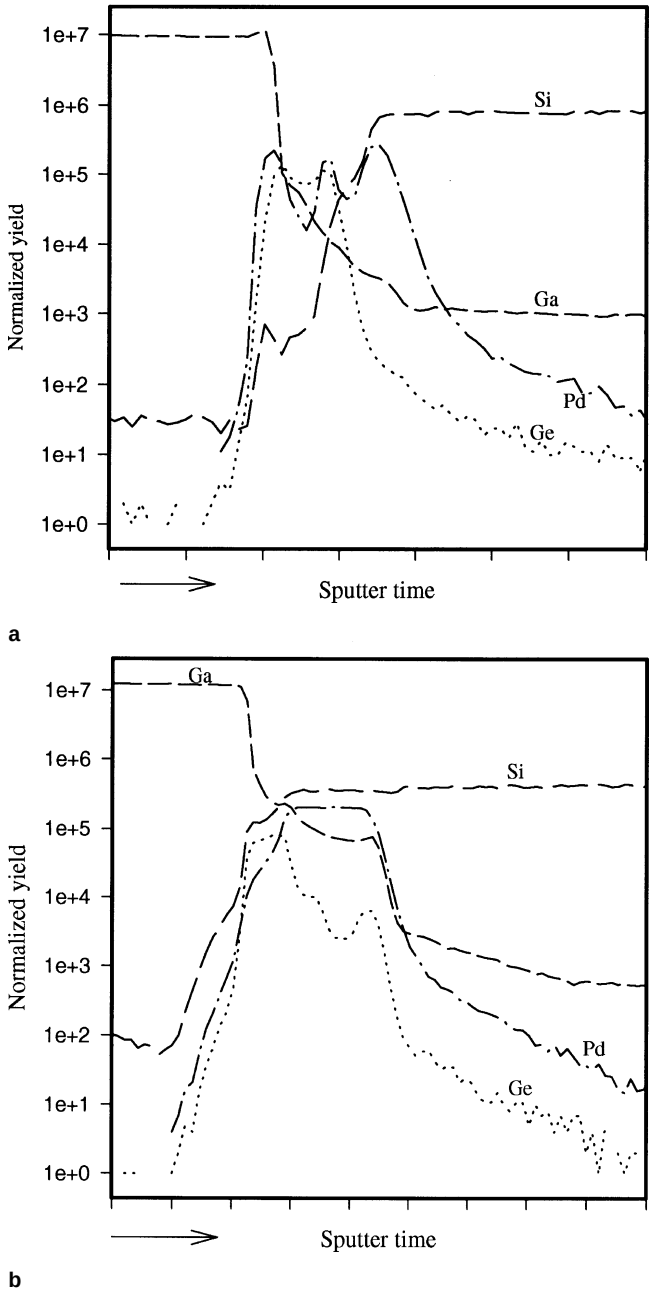

Fig. 4. SIMS profiles of an ELO n-GaAs/Pd/Ge/Pd/n$^+$-Si sample (a) before annealing, and (b) after annealing.

and the two semiconductors was studied by XRD. The measurement was made on samples before and after annealing. The XRD patterns are shown in Fig. 3. Before annealing, the only peaks observed are due to GaAs, Si, Pd, and Ge. After annealing, a compound of Pd_2Si is identified by the diffraction peaks. The formation of Pd_2Si is the key to the ohmic contact to Si. The depth profiles of the constituent elements were measured by a Cameca IMS-5F SIMS spectrometer using an O_2^+ ion beam at normal incidence. Figure 4a and 4b are the measured results for samples before and after annealing, respectively. After annealing, the Si atoms move into the metal layer and together with Pd form a plateau region. This is a good evidence of the formation of Pd silicide, which is observed by the XRD measurement. While Pd_2Si makes ohmic contact to Si, the Si atoms and Ge atoms move toward the metal/GaAs interface to heavily dope the GaAs interface region to make ohmic contact to GaAs. Figure 5 shows the scanning electron microscopy (SEM) photomicrograph of the cross section of a sample after annealing. A well bonded GaAs/metal/Si structure with smooth interfaces was observed.

APPLICATION

In order to demonstrate the good electrical and mechanical properties of the bonded structure, we

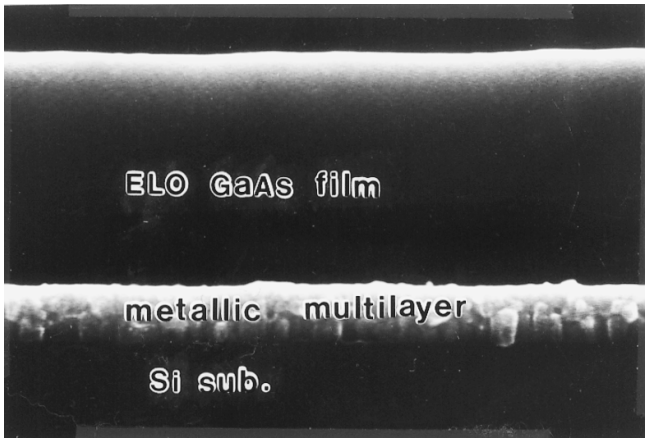

Fig. 5. SEM photograph of a bonded ELO n-GaAs /Pd/Ge/Pd/n⁺-Si sample.

fabricated an ELO GaAs/InGaAs laser on a Si substrate with the back-side contact on Si. Figure 6a shows the schematic diagram of the final structure. The laser diode has a cavity length of 800 μm and a stripe width of 5 μm. The detailed fabrication process has been described in Ref. 13. A typical light output vs current curve is shown in Fig. 6b. A threshold current of 23 mA and a differential quantum efficiency ~0.33W/A from a single facet was obtained. This performance is comparable to that of a conventional laser diode on GaAs substrate. This result also shows that the quality of the lifted-off film is maintained after the ELO process and the metal bonding does not cause any material problems.

CONCLUSION

Low-resistance ohmic conduction across an epitaxially lifted-off n-GaAs thin film and a Si substrate has been obtained by inserting a Pd/Ge/Pd interlayer between them. Good bonding and ohmic contact to both Si and GaAs were achieved after annealing. While Pd/Ge, Si forms smooth ohmic contact to GaAs, Pd_2Si formed at the interface provides a smooth and shallow ohmic contact to Si. This technique gives the ELO process an added capability of vertical conduction through the substrate and provides more flexibility in hybrid integration.

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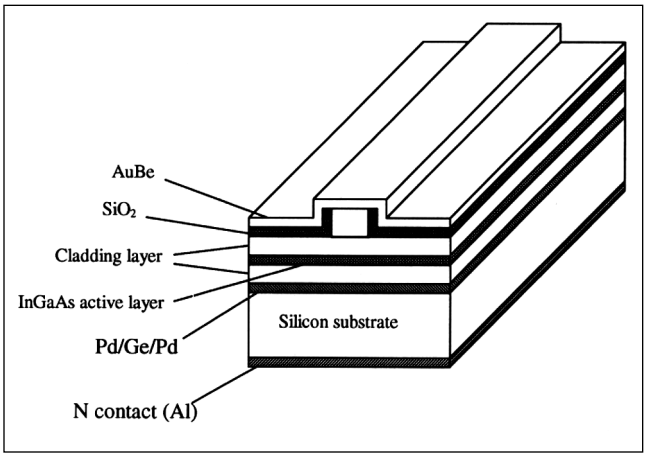

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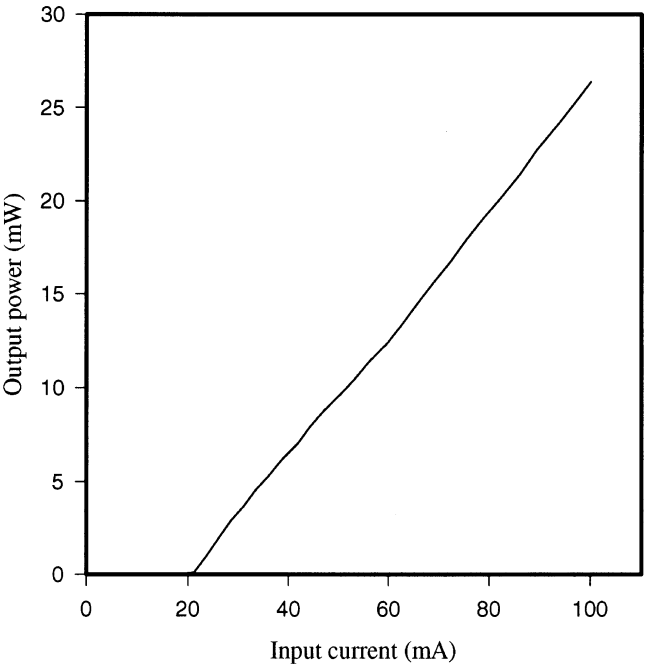

b

Fig. 6. (a) The schematic diagram of an ELO stripe-geometry InGaAs/GaAs/AlGaAs GRIN-SCH lasers diode on n⁺-Si substrate with the back side contact on Si, and (b) the measured light-current curve of the ELO stripe-geometry laser on Si.

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