Evaluation of Plasma Charging Damage in Ultrathin Gate Oxides

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***Abstract*—Monitoring of plasma charging damage in ultrathin oxides (e.g., <4 nm) is essential to understand its impact on device reliability. However, it is observed that the shift of several device parameters, including threshold voltage, transconductance, and subthreshold swing, are not sensitive to plasma charging and thus not suitable for this purpose. Consequently, some destructive methods, such as the charge-to-breakdown measurement, are necessary to evaluate plasma damage in the ultrathin oxides.**

***Index Terms*— Dielectric breakdown, plasma materials-processing applications, semiconductor device reliability.**

THE plasma charging damage has attracted much attention in recent years [1]–[9]. As gate oxide thickness is scaled down, the plasma charging damage can potentially degrade oxide integrity significantly. Therefore, how to monitor and minimize the damage becomes important. To this date, most reported studies characterized the charging damage induced in gate oxide which is thicker than 4 nm. In these oxides, Fowler–Nordheim (F–N) tunneling current is the conduction mechanism during high field stressing. Under such situations, electron current injected into the oxide may deposit energy in the oxide and lead to trap creation and interface state generation. These events may shift the device parameters such as threshold voltage ($V_{\rm th}$), subthreshold swing (S_S), transconductance (G_m), etc. Consequently, those device parameters can be used as indicators in monitoring the charging damage. As gate oxide is scaled below 4 nm, however, the situation may change since direct tunneling process replaces the F–N tunneling if oxide voltage ($V_{\rm ox}$) is smaller than the barrier height of electron at the Si/SiO$_2$ interface (~3.2 V). Therefore, the effectiveness of using those device parameters in characterizing the damage should be carefully examined.In this letter, we investigate this issue by performing measurements on devices with 2.6-nm gate oxide. MOS capacitors and n-channel transistors were fabricated on 6-in wafers. Gate oxides were grown after LOCOS isolation, followed by n+ poly-Si deposition which was employed as the gate electrode. Oxide thickness was determined by fitting the current–voltage characteristics with theory [10] and verified by high resolution TEM [11]. Metal antenna structures attached to the gates were used to monitor the damage. After definition of metal patterns, the photoresist is stripped off in a down-stream type asher. Detailed description of the asher can be found in our previous reports [4]–[6]. Finally, wafers received a 400 °C anneal in forming gas for 20 min. Electrical characterization was then performed with an HP 4145 parameter analyzer.

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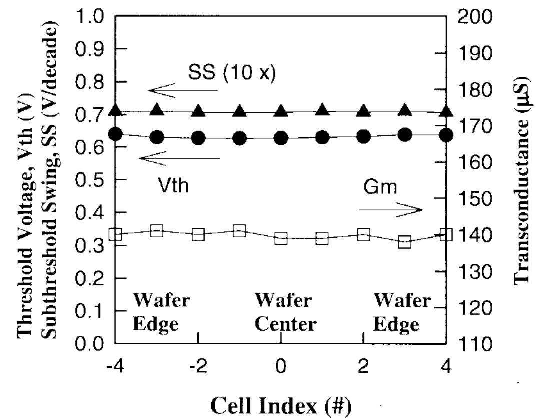

Fig. 1. Threshold voltage, subthreshold swing, and transconductance as a function of cell position. Antenna area ratio of the devices is 15 000.

Fig. 1 shows the $V_{\rm th}$, S_S, and G_m of transistors as a function of cell location. The measurements were performed on nine cells along a line that lies across the wafer. The measured devices have a channel length and width of 1.7 and 10 μm, respectively; and antenna area ratio (AAR) value of 15 000. It is seen that, even with a large AAR value, these parameters vary only slightly across the wafer. In addition, no significant difference is found among transistors with various AAR values. Based on these results, one would tend to conclude that the plasma damage is negligible. However, significant damage is actually identified by the charge-to-breakdown ($Q_{\rm bd}$) measurements, as illustrated in Fig. 2. Transistors with AAR of 500 and 15 000 were measured and compared. Distinctive difference between the two types of devices is found at the wafer center, in which the $Q_{\rm bd}$ of devices with AAR of 15 000 drops to 0, indicating that severe damage has been induced. The damage region is similar to that found in previous reports [3]–[6], and has been identified to be induced during ashing treatment. Comparing the results

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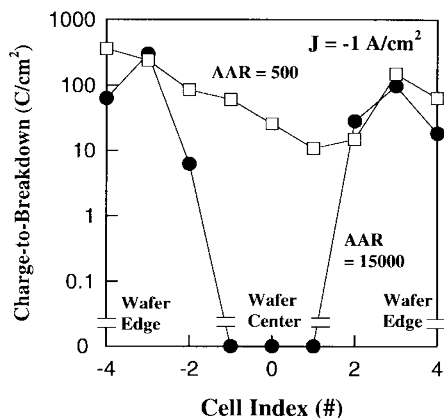
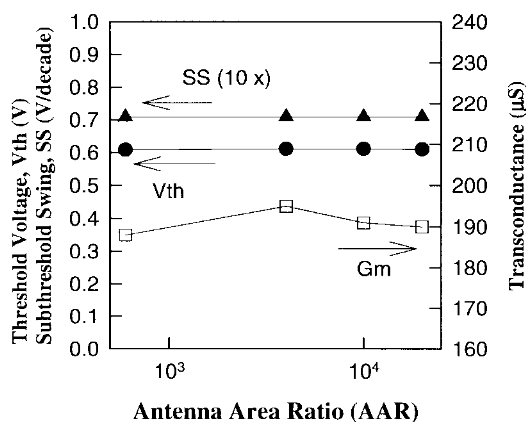
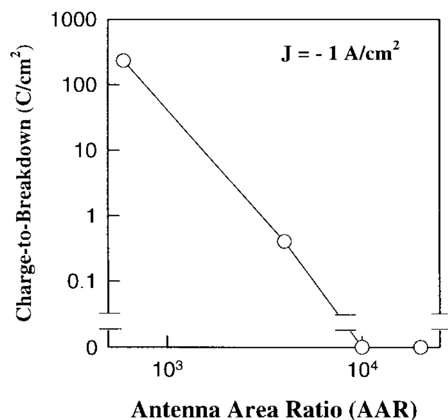


Fig. 2. Charge-to-breakdown values as a function of cell position.



(a)

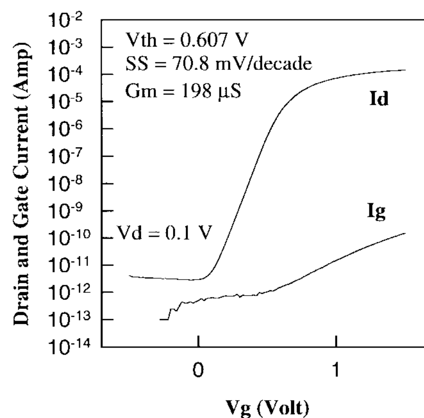


(b)

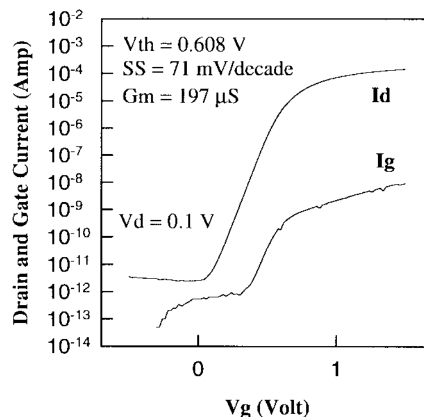
Fig. 3. (a) Threshold voltage, subthreshold swing, and transconductance, and (b) charge-to-breakdown values as a function of antenna area ratio. The test cell is located at the wafer center.

shown in Figs. 1 and 2, it becomes obvious that the parameters used in Fig. 1 are not appropriate to serve as the indicators for monitoring charging damage in ultrathin oxides.

In order to make this point even more clear, we also measured the aforementioned parameters of transistors with various AAR values from a cell located in the wafer center. The results are shown in Fig. 3, in which the channel length and width of the measured devices are 1.2 and 10 μm, respectively. From Fig. 3(a), it is observed that the $V_{\rm th}$, S_S, and G_m are independent of the AAR values. Nevertheless, distinctive antenna effect can be seen from the $Q_{\rm bd}$ measurement [Fig. 3(b)], consistent with the results shown in Fig. 2. Therefore, it can be concluded that $Q_{\rm bd}$ is more reliable and sensitive than those device parameters in evaluating charging damage.



(a)



(b)

Fig. 4. Drain and gate current as a function of gate voltage measured (a) before and (b) after charge-to-breakdown test. Channel length and width of the measured transistor are 1.2 and 10 μm, respectively.

Such a finding is reasonable, since the rates of trap creation and interface state generation under high-field stressing decrease significantly as oxides are scaled down [12]. In fact, we also found that the subthreshold characteristics of a transistor with such thin oxide depict little changes even after the charge-to-breakdown test. An example is shown in Fig. 4, in which the $V_{\rm th}$ only shifts 1 mV after oxide breakdown, while S_S and G_m remain almost unchanged. The only parameter that depicts significant changes shown in the figures is the gate leakage (I_g), which increases significantly after oxide breakdown. The resultant excessive I_g could prevent the device from practical applications. However, without actually monitoring the I_g, the failed device may possibly be regarded as "good". This point has been raised previously [9], and becomes significant as oxide thickness is scaled.

In summary, we have shown that traditional method of monitoring the transistor parameters, including $V_{\rm th}$, S_S, and

G_m, may not be appropriate for detecting the charging damage in gate oxides as thin as 2.6 nm. In order to access the real damage situation, some destructive measurements, such as charge-to-breakdown, time-dependent dielectric breakdown (TDDB), or breakdown field measurement, maybe indispensable. It is noted that, long-channel devices (e.g., 1.7 and 1.2 μm) have been commonly used for characterizing the charging damage to eliminate uncertainties due to channel length variations. However, as devices' dimensions enter the deep submicron regime, the situation may probably become more complicated due to the presence of short-channel and short-width effects, which could make the shift of device's parameters significant.

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