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LOW-FREQUENCY NOISE CHARACTERISTICS OF HOT CARRIER-STRESSED BURIED-CHANNEL PMOSFETs

SHENG-LYANG JANG[1], HENG-KUEN CHEN[1] and KOW-MING CHANG[2]

[1]Department of Electronic Engineering, National Taiwan Institute of Technology, 43 Keelung Road, Section 4, Taipei 106, Taiwan, R.O.C.

[2]Institute of Electronics, National Chiao Tung University, Hsin-Chu 300, Taiwan, R.O.C.

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Abstract—Prestress and poststress low-frequency noise characteristics of buried-channel LDD pMOSFETs have been studied. The devices were stressed at low gate and high drain bias, and the poststress drain current increases due to the hot-electron induced channel shortening effect. The noise measurements were carried out between 10 Hz and 100 kHz, $1/f^{1.2}$ and generation–recombination current noises have been found in the drain current noises. The poststress $1/f^{1.2}$ drain current noise increases in both the linear and saturation regime. This behavior is attributed to the increase of interface states and oxide electron charges after stress. © 1998 Elsevier Science Ltd. All rights reserved

1. INTRODUCTION

MOSFETs are finding more and more important applications in the area of analog integrated circuits. The capability of integrating low-noise analog circuits and high-speed digital circuits on the same chip is crucial to the production of a wide range of high-performance MOS integrated circuits such as A/D converters, memories and telecommunication circuits. The use of buried-channel (BC) MOSFETs results in improved performance both in digital and analog circuits. This is due to several properties such as lower excess noise in low frequencies, lower gate capacitance, and higher channel mobility compared to a standard MOS transistor. A BC MOSFET is usually realized by implanting the channel region of a MOS transistor, with impurities of opposite type to the substrate doping. When BC MOSFETs are operated with the conducting channel away from the $Si–SiO_2$ interface, the $1/f$ noise is greatly reduced. Since minority carrier transport now occurs aways from the interface, the charge fluctuation in interface states and consequently $1/f$ (or more generally $1/f^{\gamma}$) noise may be reduced[1,2]. In this mode of operation, not only a thermal noise but other low level noise sources are revealed[3]. The bulk channel MOSFET has a $1/f$ noise Hooge parameter α among the lowest values ever reported in the literature for silicon MOSFETs[4]. Furthermore α is two order of magnitude lower than that of a surface channel device. Experimental analyses have yielded evidence of at least an order of magnitude improvement of noise performance in the ion implanted nMOSFETs over standard surface channel MOSFETs of equivalent geometry.

It has been recognized that hot-carrier reliability in submicron p-MOSFETs can also impose as severe constraints as in nMOSFETs. It was found by several authors such as Wang *et al.*[5] that the degradation of the linear drain current of pMOSFETs proceeds logarithmically in time. They attributed their observation to the trapping of electrons in gate oxide layers. It was reported by Tsudiya *et al.*[6] that interface states generated by the hot hole injection also contribute to the degradation of quarter-micrometer pMOSFETs. Woltjer *et al.*[7] also observed generation of the interface states during the hot carrier stress of LDD pMOSFETs by the charge pumping method. Pan[8] reported that the degradation of the LDD saturation drain current proceeds logarithmically in stress time while the linear current gradually saturates. The hot-electron-induced-punchthrough (HEIP) effect[9,10] is most significant in pMOSFETs because of their buried channel nature, which makes them more vulnerable to drain induced barrier lowering (DIBL) and consequently source–drain punchthrough. Two approaches may be useful to mitigate the HEIP effect: first, the effective channel length may be increased by using shallow source/drain diffusion, and secondly hot electron generation may be minimized by reducing the channel electric field. These two approaches are satisfied simultaneously by employing an LDD (lightly doped drain) structure.

Up to now no hot-carrier stress effect on the low-frequency noise performance of BC LDD pMOSFETs has been reported in literature, and beacuse the BC MOSFET has the lower $1/f$ noise of various MOSFETs, therefore in this paper we study the hot-carrier-stressed low-frequency noise performance of these devices.

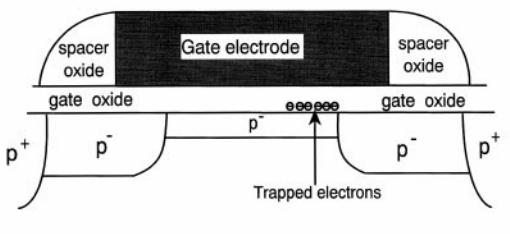

Fig. 1. Schematic diagram of a stressed LDD MOSFET.

2. EXPERIMENTAL DETAILS AND DISCUSSION

In this section we describe the low-frequency noise performance of fresh and poststressed normally-off buried-channel LDD pMOSFETs. The devices were mounted on a probe station, and were shielded in a metal box to avoid external interference. The DUTs were biased in series with a metal-film resistor, the noise across the devices were feedback to a low-noise amplifier and the spectrum analyzer was used to measure the noise spectrum output from the amplifier. The noise measurements were carried out between 10 and 100 KHz at room temperature.

Figure 1 shows the schematic of a damaged pMOSFET, the channel is divided into two regions, one is the undamaged region near the source and the rest is the damaged region. For pMOSFETs, the electron gate current at low V_{GS} is larger than the hole gate current at high V_{GS}, hence the hot-electrons can be trapped in the gate oxide, attract the holes to the semiconductor surface, and cause channel shortening, which increases the poststress drain current. Figure 2 shows the fresh and poststress current–voltage characteristics of a pMOSFET. The devices used in this study were buried-channel LDD pMOSFETs, the gate-oxide thickness is $t_{ox}=9$ nm, the gate length is $L = 0.60\ \mu$m. The transistor was stressed under maximun hot-electron injection conditions: $|V_{DS}| = 7$ V, $|V_{GS}| = 1.2$ V and stress time = 23000 s.

Figure 3(a) and (b) are two typical fresh drain current noise spectral densities. Figure 4(a) and (b) are the poststress drain current noise spectral densities. These figures show that the noises consist of $1/f^{1.2}$ and generation–recombination (G–R) noises. G–R noise is easily distinguishable from the flicker noise component, with the G–R power spectrum having a Lorentzian shape with pleateau and steep $1/f^2$ regions. G–R noise shows up in the measured current noise spectrum as the trap energy level crosses the quasi-Fermi level. It results from the carrier transitions between the conduction/valence band and the trap energy levels. The transition is a thermal activated process[9]. We have found we can use Equation (1) to extract the noise components in all regions of operation

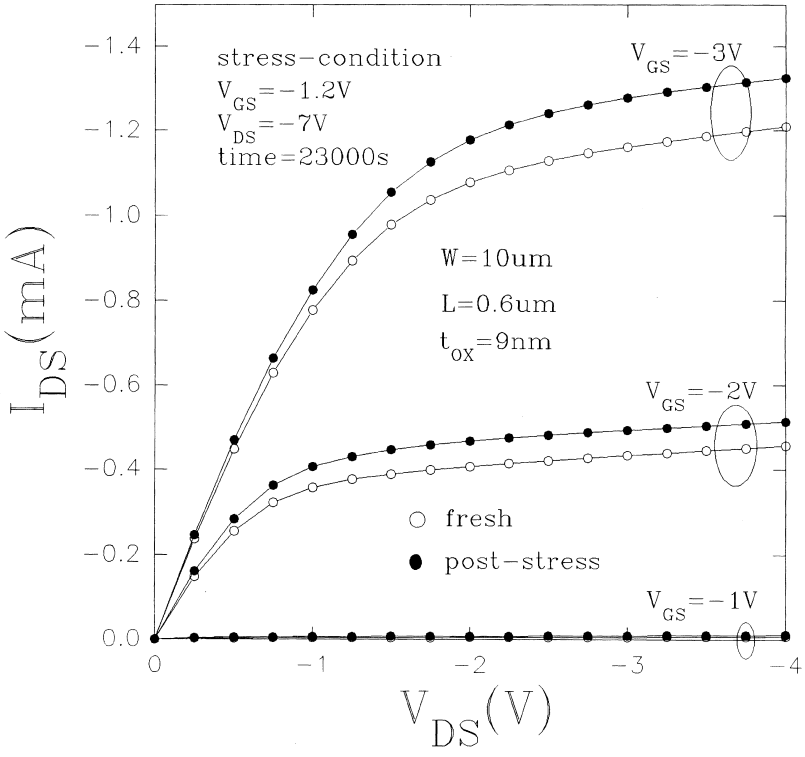

Fig. 2. Measured fresh and poststress *I–V* characteristics of a p-type buried-channel LDD MOSFET with $W = 10.0\ \mu$m, $L = 0.60\ \mu$m and $t_{ox}=9$ nm.

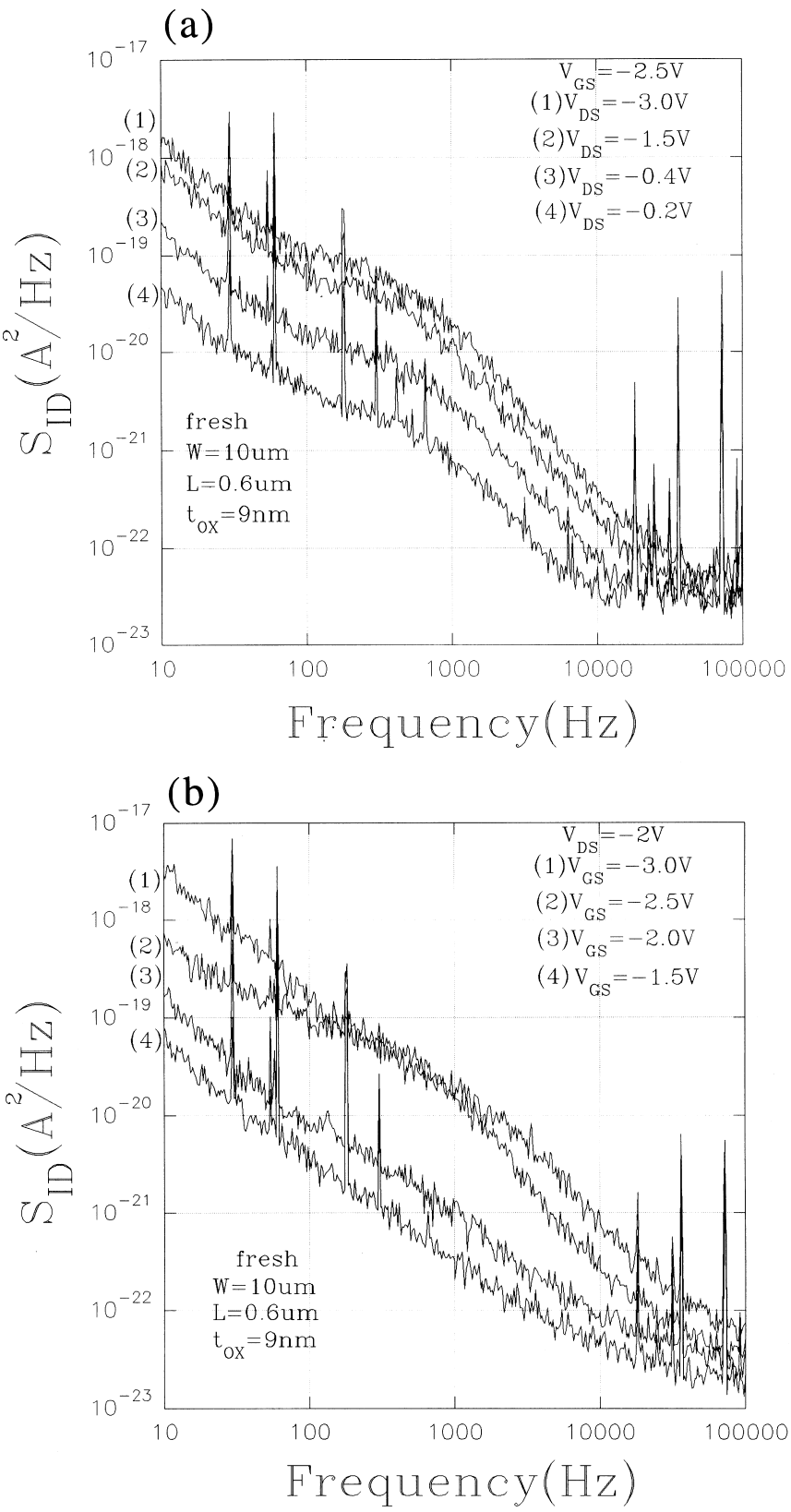

Fig. 3. Measured fresh drain current spectral densities of a p-channel LDD MOSFET.

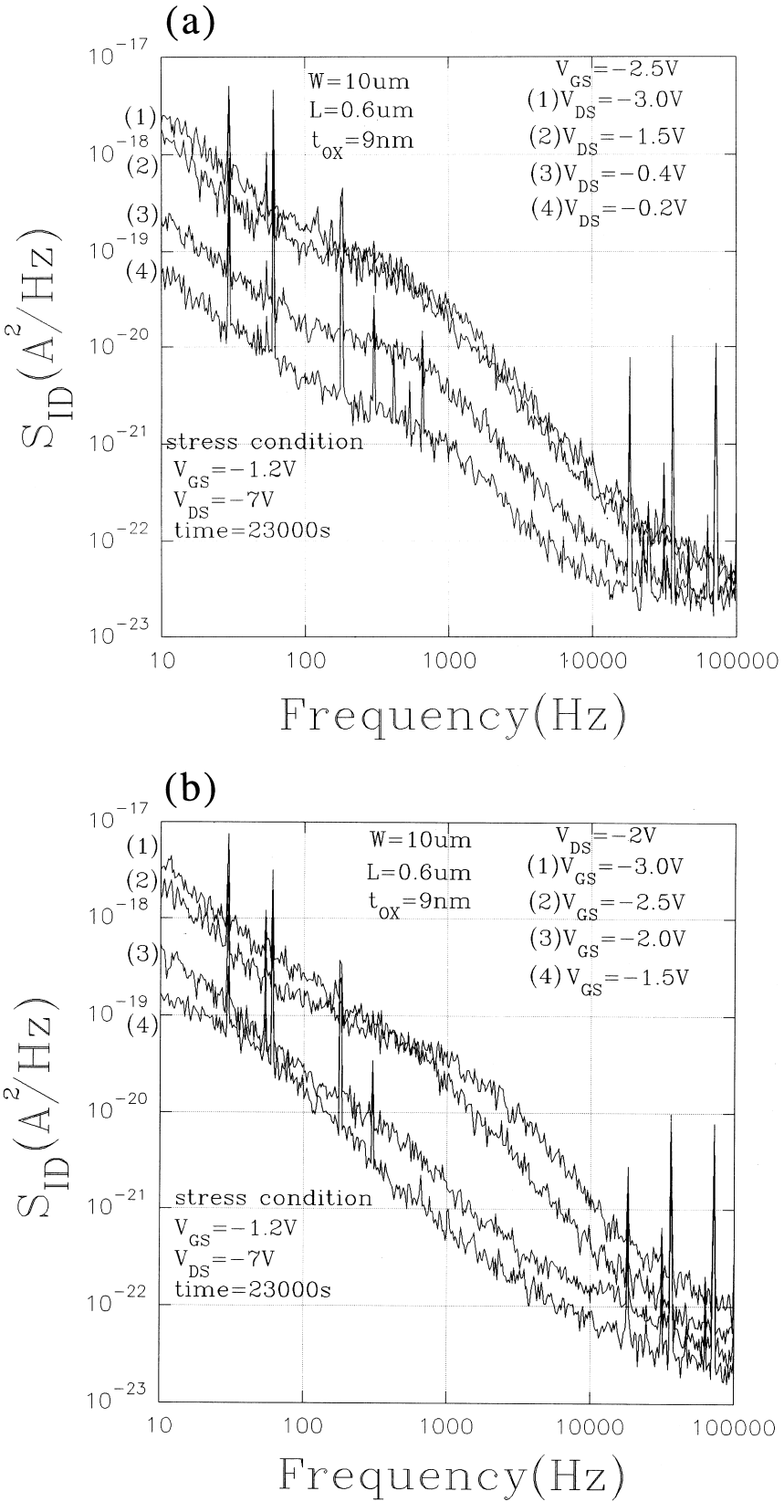

Fig. 4. Measured poststress drain current spectral densities of a p-channel LDD MOSFET.

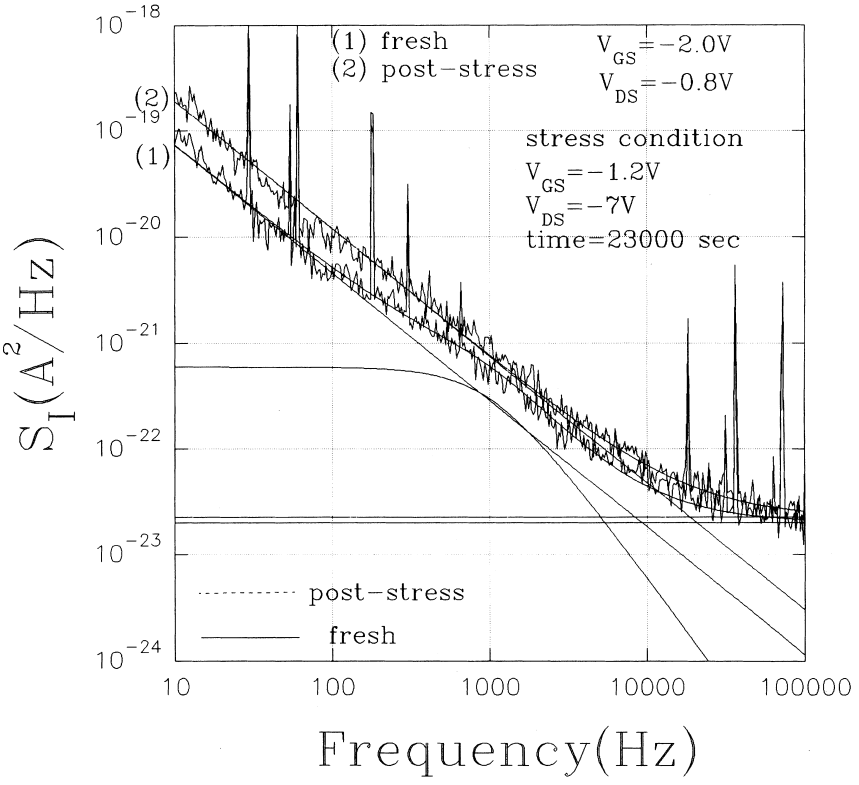

Fig. 5. Decomposition of the measured current noise in terms of its components.

$$S_{I_{DS}}(f) = \frac{C_1}{f^{1.2}} + \frac{g_1}{1+(f/f_t)^2} + C_x \qquad (1)$$

where f_t is the roll-off frequency. C_1, g_1 and C_x are fitting constants.

Figure 5 shows the fitting fresh and poststress results of a device under the same bias condition. It indicates that the poststress noise current consists of a pure $1/f^{1.2}$ noise and a white noise, the fitting parameters are $C_1 = 3.0 \times 10^{-18}$, and $C_x = 2.2 \times 10^{-23}$, which were measured at $V_{GS} = -2.0$ V and $V_{DS} = -0.8$ V. In the fresh noise curve we found an additional G–R noise component, the fitting parameters are $C_1 = 1.15 \times 10^{-18}$, $g_1 = 6.0 \times 10^{-22}$, $f_t = 1000$ Hz, and $C_x = 2.2 \times 10^{-23}$. Because the poststress $1/f^{1.2}$ current noise increases, we can not see the original G–R noise of the fresh device in the poststress noise spectrum. The calculated relative current noise $S_{I_{DS}}/I_{DS}^2$ also increases after stress. Similarly we can obtain the values of parameters at other bias. The bias V_{GS} changes the level of the quasi-Fermi potential, hence the magnitude of G–R noise increases with V_{GS}, then decreases as shown in Fig. 3(b) and Fig. 4(b).

Figure 6(a) is a comparision of the fresh and poststress drain current noise spectral densities with a pronounced G–R noise spectrum with $f_t = 500$ Hz. This indicates that this G–R center is not affected by the stressing. This can be further supported by the results shown in Fig. 6(b), the extracted fresh and poststress f_t associated with $V_{GS} = -2.5$ V have a similar V_{DS}-dependence. The G–R center may locate in the oxide near the interface as in the interpretation of random telegraph signals (RTSs) in small MOSFETs[11], it is a localized G–R center. A channel electron can be captured into the border trap. The G–R noise may be due to random emission of electrons and holes at the defect centers in the depletion regions[12]. The information is not sufficient at this stage to identify the location of this G–R center due to the lack of analytical buried-channel noise model. As the device is turned on, the semiconductor surface is in accumulation condition, the variation of V_{GS} will change the band bending of the oxide and the trap energy level and affect the generation–recombination rate. In our device, in above-threshold, the conduction-band edge at the interface lies near the quasi-Fermi level, the depleted bands in the bulk semiconductor are screened by the surface accumulation layer and shift by much less. The G–R noise may be due to a border trap. Figure 6(b) also shows the V_{DS}-dependence of f_t for the fresh and the poststress device biased at $V_{GS} = -1.5$ V. The extracted fresh f_t remains constant as the device is operated in the saturation mode, it indicates this trap is uniformly distributed along the channel, as V_{DS} increases the location for the trap with trap energy crossing the quasi-Fermi level also moves toward the source. However the extracted poststress f_t becomes smaller

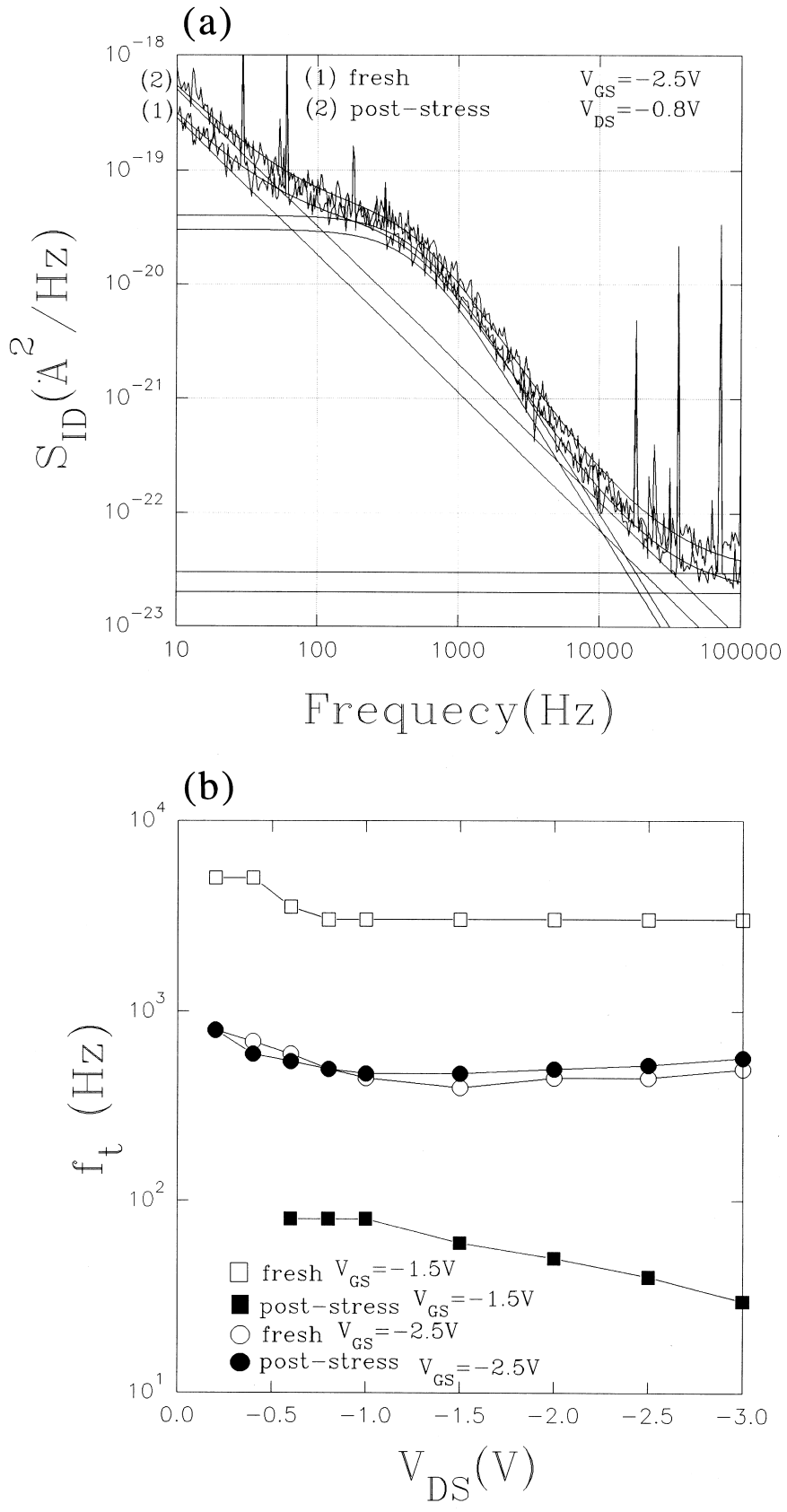

Fig. 6. (a) Comparision of the fresh and poststress drain current noise spectral densities with a pronounced G–R noise spectrum with $f_t = 500$ Hz. (b) The V_{DS}-dependence of f_t for the fresh and the poststress device biased at $V_{GS} = -1.5$ V and $V_{GS} = -2.5$ V.

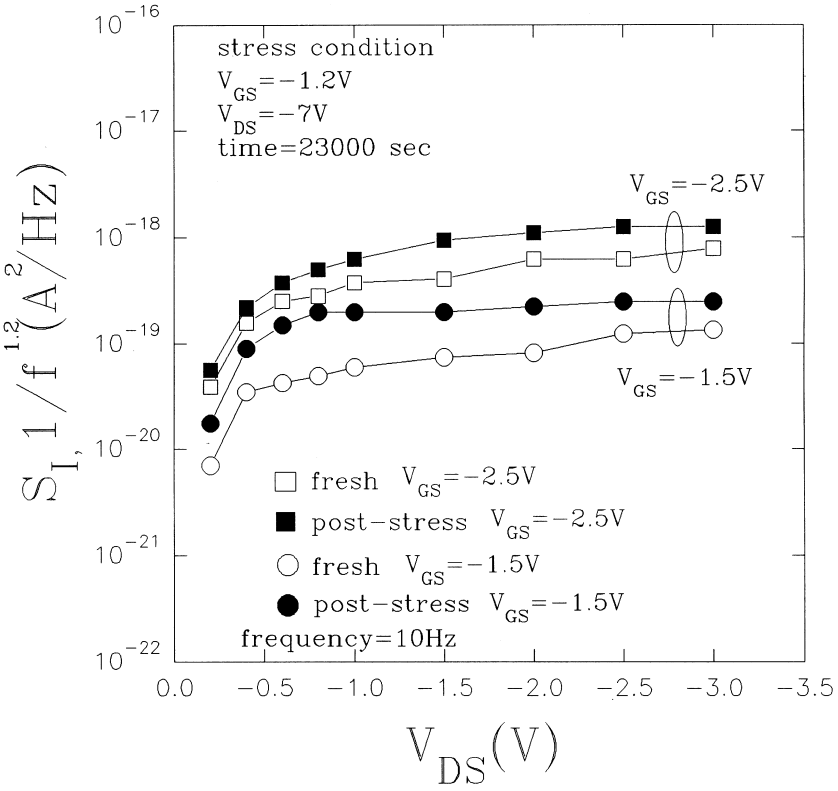

Fig. 7. Extracted $1/f^{1.2}$ drain current noise current.

as the device is operated in the saturation mode and as V_{DS} increases. This indicates the stress-generated traps are nouniformly distributed along the channel and possibly these traps are different in their trap energies.

Figure 7 is a comparision of the fresh and poststress $1/f^{1.2}$ current noise spectral densities. The stressing increases the nonuniform distribution of interface states which directly affect the bias-dependent $1/f^{1.2}$ noise, however the hot-carrier induced negative oxide charges increase the drain current, these two mechanisms interact to produce the results as shown in this figure. Generally traps are distributed over space inside the oxide as well as in energy over the bandgap. The $1/f^{\gamma}$-frequency dependence instead of $1/f$ can be explained by a nonuniform spatial distribution of traps in the oxide[13]. For a trap distribution that increases away from the interface, there are a great number of low-frequency traps leading to $\gamma > 1$.

The $1/f$ noise in the drain current of nMOSFETs has been extensively studied for many years. Although it is generally agreed that the current fluctuations are due to trapping/detrapping of channel carriers, the exact origins and nature of the traps are still subjects of debate. In view of the fact that high-frequency RTS's have been found to arise from interface traps[14], and the $1/f$ noise is believed to be a superposition of numerous RTS's, it would be surprising if the $1/f$ noise was indeed not affected by the density of interface states D_{it}. Todsen *et al.*[15] presented the results of linear region $1/f$ noise and D_{it} measurements performed on pMOS transistors subjected to high electric field stressing of the gate oxide. High electric field imposed across the oxide allows electrons to tunnel through the oxide via Fowler–Nordheim (FN) tunnelling. These tunnelling electrons create additional traps in the oxide. For the pMOS transistors studied, the $1/f$ noise increases during the high field stressing. By plotting the $1/f$ noise as a function of D_{it}, a direct relationship between the increase in these two parameters is observed. It is believed that the low-gate hot-carrier stress in this work plays the role to increase the trapped oxide charges and generate interface states. This results in an increase of poststress $1/f^{1.2}$ current noise.

3. CONCLUSION

In this paper we have carried out detailed experimental study on the low-frequency noises of fresh and poststress buried-channel LDD pMOSFETs. The devices were stressed at low gate bias, and the hot-electron-induced channel shortening is responsible for the increase of the poststress drain current. Generation–recombination and $1/f^{1.2}$ noise components have been found in the drain current noise for the devices operated both in the linear and saturation regions. From the bias-dependence of the

roll-off frequecy of G–R noise we found G–R centers are spatially uniformly distributed along the channel for the fresh device, however new generation–recombination centers have been generated after the stressing, these newly-generated G–R centers are possibly nonuniformly distributed in energy and space, and they affect the noise-performance of poststress MOSFETs. The increase in $1/f^{1.2}$ current noise after stress is due to the stress-induced channel shortening and interface states.

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