observed which results from the combination of high sheet charge density in the channel and low access resistance. The low-field source-drain resistance at V_{GS} = 0V is 0.45 Ω mm. The devices display a good pinchoff at V_{GS} = –1.6V and a negligible kink effect.

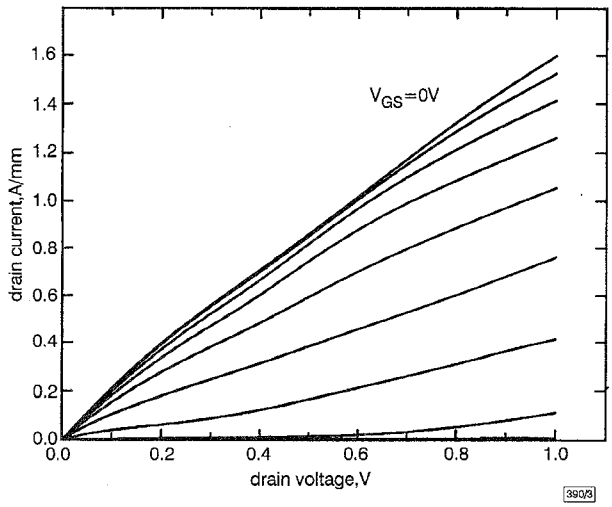

Fig. 3 *HEMT drain characteristics*
L_G = 0.5μm, L_{SD} = 1.2μm, W_G = 28μm, V_{GS} = 0.2V/step

A maximum DC transconductance above 1S/mm is measured at V_{GS} = 0.5V. The S-parameters of the HEMTs were measured on-wafer from 1 to 40GHz. Based on the usual 6dB/octave extrapolation, the device exhibits an f_T and f_{max} of 45 and 70GHz, respectively, at V_{GS} = 0.4 and V_{GS} = –1.1V. At this bias condition, the microwave transconductance and output conductance were 600 and 100mS/mm, respectively, and the gate leakage current was 40μA. An equivalent circuit of the HEMT was developed by fitting the measured S-parameters to a commonly-used circuit topology. After removal of the gate bonding pad capacitance from the equivalent circuit, an f_T of 60GHz was obtained, which corresponds to an $f_T L_g$ product of 30GHz μm. At higher drain voltages, the effects of impact ionisation become apparent with the gate leakage current increasing and the low-frequency unilateral gain decreasing significantly. HEMTs with a 0.4μm gate length were also fabricated in material with a similar layer design and sheet charge density, except that a composite GaSb/InAs cap layer was employed. The overall behaviour of these HEMTs was found to be similar to those HEMTs previously described. However, they exhibited a slightly improved performance due to the shorter gate length, yielding an extrinsic f_T and f_{max} of 75 and 100GHz, respectively, at V_{DS} = 0.5V.

These initial results demonstrate that Si-doping in a thin InAs layer located adjacent to the AlSb barrier can be used to produce HEMTs with high sheet charge density. Optimisation of the present growth process will lead to higher sheet densities and channel mobilities. To realise the performance potential of AlSb/InAs HEMTs, the combination of this doping approach with improved buffer and barrier layer designs is needed to minimise leakage current, improve modulation efficiency, and more effectively manage the holes generated by impact ionisation.

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Effects of N_2O-annealed sacrificial oxide on the short-channel effects of *n*MOSFETs

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The authors report the effects of N_2O-annealed sacrificial oxide on *n*MOSFETs. It is demonstrated that by adding an N_2O-annealing step to the sacrificial oxide which was stripped off before growing the final gate oxide, the reverse short-channel effects (RSCE) can still be effectively suppressed.

Introduction: Recently, the reverse short-channel effect (RSCE) has received much attention [1 – 6]. Unlike the conventional normal short-channel effect (NSCE), in which the threshold voltage (V_{th}) decreases with decreasing channel length, RSCE involves an increase in V_{th} with decreasing channel length. It has now been generally agreed that RSCE is caused by the non-uniform lateral distribution of channel surface concentration near the source/drain region. This lateral non-uniformity in surface dopant concentration can be attributed to several processing steps, including oxidation-enhanced diffusion (OED), vacancy injection during source/drain salicidation, or fluorine enhanced boron diffusion, for example. It has also been reported that by nitriding the gate dielectric (i.e. final gate oxide), or by performing the after-gate re-oxidation in an N_2O ambient, RSCE can be suppressed [7, 8]. In this Letter we report, for the first time, that RSCE can also be effectively suppressed by performing the nitridation process on the sacrificial oxide, which is stripped off before the final gate oxide is grown.

Fabrication process and results: A typical 0.8μm, double-level-polysilicon CMOS process was used. After LOCOS processing, the pad oxide was stripped off, and a 25nm sacrificial oxide was grown. The sacrificial oxide is usually employed in a typical MOS process flow for reducing the LOCOS-related gate oxide defect, and for improving the integrity of the final gate oxide by allowing the performance of the V_{th}-adjust implant and anti-punchthrough implant through the sacrificial oxide, which is then stripped off prior to growing the final gate oxide. In this study, the 25nm sacrificial oxide in the control split was grown by a conventional dry O_2 oxidation. For the N_2O-annealed split, the 25nm sacrificial oxide was first grown by a dry O_2 oxidation, followed by an N_2O-annealing for 15mm at 925°C, to produce a final thickness of 25nm. Wafers were then combined to receive an anti-punch-through implant (boron, 160keV, 2.5 × 10^{11}cm^{-2}) and a V_{th}-adjust implant (BF_2, 90keV, 2.2 × 10^{12}cm^{-2}) by implanting through the

sacrificial oxide. Afterwards, the sacrificial oxide was stripped off in buffered HF, and a 20 nm final gate oxide was grown in dry O_2 ambient at 950°C. A polysilicon layer was subsequently deposited, $POCl_3$-doped, and patterned to form the gate of the transistor.

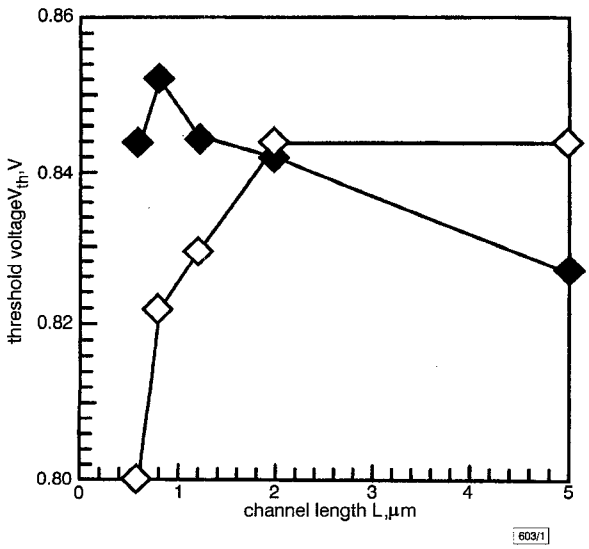

Fig. 1 *Threshold voltage against channel length for control devices with conventional SiO_2 sacrificial oxide and devices with N_2O-annealed sacrificial oxide*

◆ SiO_2 sacrificial oxide
◇ N_2O-annealed sacrificial oxide

Threshold voltage (V_{th}) against channel length for all *n*MOSFETs is shown in Fig. 1. It is interesting to note that while the control devices with conventional SiO_2 sacrificial oxide depict RSCE (i.e. V_{th} increases first before finally decreasing with decreasing channel length), the devices with N_2O-annealed sacrificial oxide depict NSCE (i.e. V_{th} decreases monotonically with decreasing channel length). This result indicates that, similar to growing the final gate oxide in an N_2O ambient, or performing the after-gate re-oxidation in an N_2O ambient [7, 8], performing the sacrificial oxide in an N_2O ambient prior to growing the final gate oxide is also effective in suppressing the oxidation-enhanced diffusion, resulting in a more uniform lateral surface concentration in the channel, and thereby suppressing the RSCE. To account for the observed phenomenon, it is speculated that even though the N_2O-annealed sacrificial oxide was stripped off prior to growing the final gate oxide; the nitrogen which is incorporated at the Si/SiO_2 interface remains, serving to suppress enhanced boron diffusion during later processing. This is plausible because the buffered HF solution used to strip off the sacrificial oxide is known to be ineffective in etching silicon nitride. The effects of substrate bias are shown in Fig. 2. Our results confirm previous reports that RSCE subsides with the applied substrate bias [9]. Since substrate bias modulates the depletion width of the source/drain junction, RSCE diminishes with increasing substrate bias. The corresponding drain-induced barrier lowering (DIBL) effects are shown in Fig. 3. Devices with N_2O-treated sacrificial oxide indeed depict slightly larger DIBL, consistent with the observed NSCE in these devices (i.e. more severe V_{th}-lowering, compared to devices which depict RSCE).

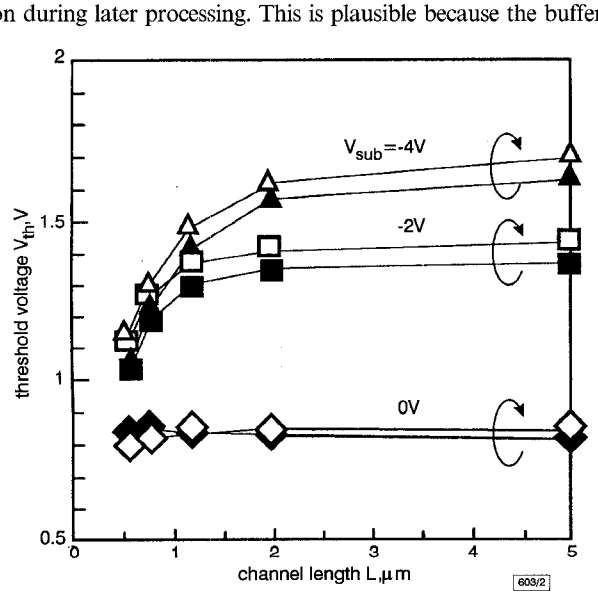

Fig. 2 *Substrate bias effects on threshold voltage against channel length for control devices with conventional SiO_2 sacrificial oxide and devices with N_2O-annealed sacrificial oxide*

▲, ■, ● SiO_2 sacrificial oxide
△, □, ◇ N_2O-annealed sacrificial oxide

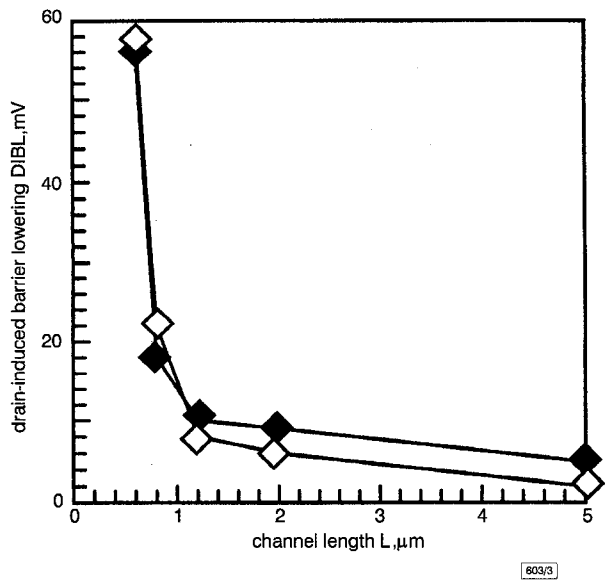

Fig. 3 *Drain induced barrier lowering against channel length for control devices with conventional SiO_2 sacrificial oxide and devices with N_2O-annealed sacrificial oxide*

● SiO_2 sacrificial oxide
◇ N_2O-annealed sacrificial oxide

Conclusion: We have reported, for the first time, that RSCE can be effectively suppressed by employing an N_2O-annealed sacrificial oxide. Even though the sacrificial oxide is stripped off before growing the final gate oxide, our data indicate that the incorporated nitrogen at the Si/SiO_2 interface remains and acts to suppress enhanced boron diffusion during subsequent thermal processing. Our results suggest that the growth condition of sacrificial oxide can also affect the short-channel effects of the resultant submicron transistors, and should therefore be carefully considered in desigining the transistor process flow.

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GaInP/AlInP tunnel junction for GaInP/GaAs tandem solar cells

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A GaInP/AlInP tunnel diode has been grown by a gas-source molecular beam epitaxy method. A high conductance of 15mA/cm² at 2.7mV has been achieved. Using closely optimised growth conditions, very high carrier concentrations, both in GaInP and AlInP, have been obtained.

A GaInP/GaAs tandem solar cell consisting of a thin GaInP top cell and a GaAs bottom cell has a significantly higher conversion efficiency than conventional single-junction solar cells [1]. One of the critical issues in the growth of such a two-terminal monolithic tandem cell is a tunnel junction for the inter-cell connection. The tunnelling interconnect must not only pass the device current with minimal electrical loss but also transmit the appropriate portion of the optical spectrum to the underlying subcell. The GaInP/AlInP tunnel junction may provide the desired interconnect. It tends to increase the quantum efficiency of the bottom cell by eliminating the absorption loss typical of the GaAs tunnel layer [1]. Conversely, the p^+-n+ GaInP junction is difficult to prepare for example by metal organic chemical vapour deposition (MOCVD), which is the most commonly used method for the growth of solar cells, because of the rapid diffusion of p-type dopants (Zn).

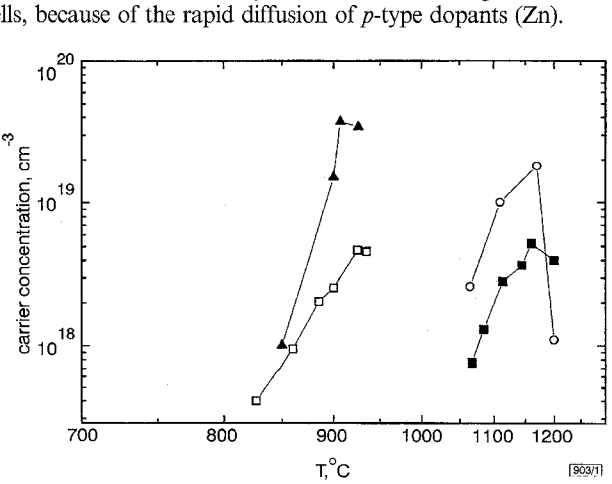

Fig. 1 *Net carrier concentrations in AlInP and GaInP layers grown by GSMBE against Be and Si oven temperatures*

□ AlInP: Be
▲ GaInP: Be
■ AlInP: Si
○ GaInPi:Si

Recently, we have shown that it is possible to prepare GaInP/GaAs tandem cells by means of gas source molecular beam epitaxy (GSMBE) [2]. Compared to MOCVD, GSMBE yields a higher p-type doping efficiency and less severe diffusion of the p-type dopant (Be). In this Letter, we present a p^+-n^+ GaInP/AlInP tunnel diode grown by GSMBE. In GSMBE, elemental solid sources are used to produce the group-III beam fluxes, while As_2 and P_2 are produced from cracked AsH_3 and PH_3. The growth temperature in our experiments was ~500°C.

Fig. 1 shows the net carrier concentrations in Si and Be-doped GaInP and AlInP, as deduced from Hall-effect measurements. The doping characteristics of AlInP differ significantly from those of GaInP. Doping with Si resulted in the maximum electron concentration of 1.8×10^{19}cm^{-3} in GaInP and 5.3×10^{18}cm^{-3} in AlInP. A further increase in Si concentration caused a decrease in carrier concentration, due to the amphoteric nature of Si. Doping with Be yielded the maximum hole concentration of 3.7×10^{19}cm^{-3} for GaInP and 4.7×10^{18}cm^{-3} for AlInP. The hole concentrations are limited by a non-homogeneous redistribution of Be in the doped layer [3]. The above-mentioned doping levels are among the highest obtained to date by any growth method.

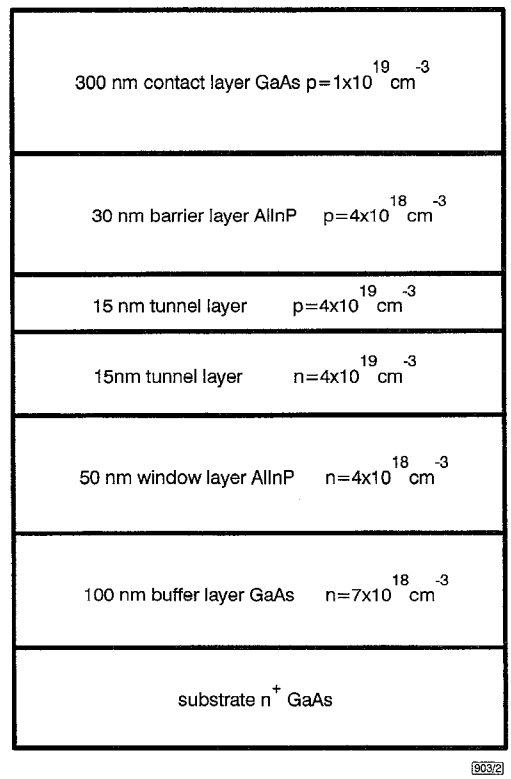

Fig. 2 *Schematic structure of GaInP/AlInP tunnel diode*

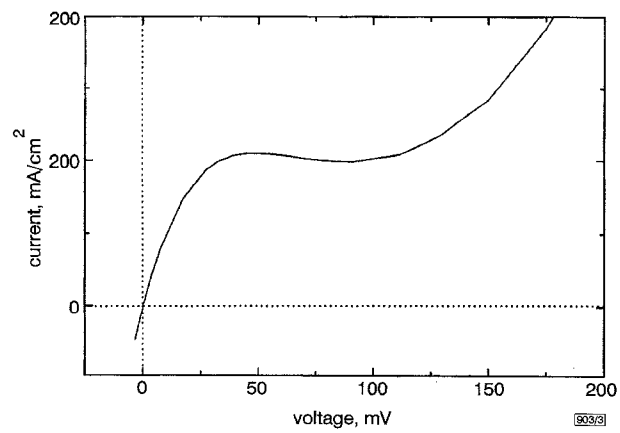

Fig. 3 *I-V characteristics of GaInP/AlInP tunnel diode*

The schematic structure of a GaInP/AlInP tunnel diode suitable for use in a GaInP/GaAs tandem cell is shown in Fig. 2. We have made the GaInP and AlInP layers lattice-matched to a GaAs:Si (001) substrate within a range of accuracy from $\Delta a/a = -600$ to 200ppm. The diodes were fabricated by alloying Ti/Pt/Au contacts to the p^+ GaAs layer and etching photolithographically defined