the implanted region. At 900 and 1050 °C, D_{it} increases steadily with anneal time and at a faster rate at 1200 °C. Since all samples were loaded into and unloaded from the furnace in about the same time, a higher heating rate was achieved as the anneal temperature was increased. More D_{it} could be induced at 1200 °C because of the higher stress introduced by the higher heating rate during loading and unloading. However, longer anneals at lower temperatures still result in an increase of interface charges. Relatively decent quality interfaces can be obtained with low resistivity source/drain regions after anneals at 1200 °C for 3 to 5 min.

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Correlation of Stress-Induced Leakage Current with Generated Positive Trapped Charges for Ultrathin Gate Oxide

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***Abstract*— In this work, the evidence of the stress-induced leakage current related with the stress-generated positive trapped charges is presented and investigated. It is shown that the centroid of the positive trapped charges, which depends on the polarity of the stress current, affects the magnitude of the leakage current. And the trapping density of positive charges, which is determined by the final stress applied on the oxide, determines the final level of the leakage currents.**

I. INTRODUCTION

The stress-induced leakage current (SILC) is a critical factor in limiting down-scaling the oxide thickness for MOSFET devices. For thin oxide films, the low-level pre-Fowler–Nordheim tunneling current increases after the high field stress [1]. This leakage will cause a serious problem in charge retention for the floating gate of EEPROM's and introduce excess power dissipation for the device operation. Hence, much work had been dedicated to studying this leakage current for hoping to improve the gate oxide reliability. It was reported that this leakage current increases with the stressing field [2] and with the injected charges [3]–[6], and depends on the stress polarity [4]–[7] and the measurement temperature [1]. The inducing mechanisms of this leakage current were attributed to stress-induced weak spots with a lowering barrier height [2], [8]–[9], to trap-assisted tunneling by the electron trap filling and emptying process [1], [3]–[5], [10]–[11], and to the positive charge-assisted tunneling [7], [12]–[17]. For an example, Liang *et al*. pointed out that the SILC is related with the positive trapped charges near the SiO_2/Si interface during their studying the trapping/detrapping of different types of charges in the oxide during dynamic stress [7]. Nevertheless, the real and detail mechanisms are generally considered to be not yet fully understood and confirmed.

Previously, a method was proposed to monitor and investigate quantitatively the trapped charge generation for gate oxide under stress [18]. Since the method can clearly differentiate generated trapped negative charges and positive charges, in this work, it was used to investigate the relationship between the leakage current and the positive trapped charges induced by electrical stresses. In the work, it was clearly shown that the centroid of the positive trapped charges, which depends on the stress polarity, affects the magnitude of the leakage current. When the centroid was shifted under different bipolar stress, the induced leakage current also transformed accordingly. Moreover, it was also shown that since the steady-state trapping density is determined by the oxide field [18]–[19], the leakage current changed to a smaller magnitude when an additional stress of a lower current density was applied to disturb the distributions of the positive

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charges in the oxide. This also gives the evidence of the close relationship between the excess leakage current and the generated positive trapped charges.

II. Experiments

The samples used in this study were $POCl_3$-doped silicon gate MOS capacitors, with an area of 2.33×10^{-4} cm^2, fabricated on a p-type Si wafer. The 80 Å gate oxide was grown in diluted dry O_2 ($O_2/N_2 = 1/6$) and annealed in N_2 (for 15 min) at 900 °C. The poly-Si gate was metallized with Al and then annealed at 400 °C in N_2 for 30 min.

An HP4145B was used to perform the electrical measurement. During measuring leakage currents, we chose a medium stepping speed on the sweeping voltage in order to minimize the line frequency noise and to avoid disturbing trap distributions in the oxide film. We limited the maximum gate current density to 10^{-6} A/cm^2 in order to avoid additional stresses. Also, because positive trapped charges are easy to be neutralized by a low reverse bias stress [7], [18], [20], leakage currents with the same polarity as that of the stress voltage were first measured for every measurement, and then the leakage currents of the reverse polarity were measured.

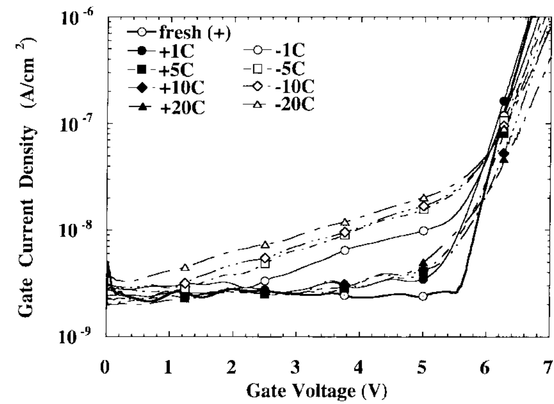
III. Results and Discussion

First, capacitors were stressed by $+10$ and -10 mA/cm^2 stresses with different injected charges, respectively. Fig. 1(a) and (b) show the induced low-level pre-Fowler–Nordheim-tunneling positive and negative leakage currents, respectively, for these capacitors. In the figures, the black dot curves are those of the positively stressed samples, and the open dot curves are those of the negatively stressed samples. It is seen that leakage currents have strong dependence on the stress polarity and the polarity of J-V measurement. For the J-V of the positive polarity measurement [Fig. 1(a)], the negatively stressed capacitors have higher leakage currents while the positively stressed capacitors have much lower leakage currents. And for the J-V of the negative polarity measurement [Fig. 1(b)], the positively stressed capacitors have higher leakage currents while the negatively stressed capacitors have much lower leakage currents. Also, for the stressed capacitors having higher leakage currents, the more the stressing injected charges, the higher the leakage currents.

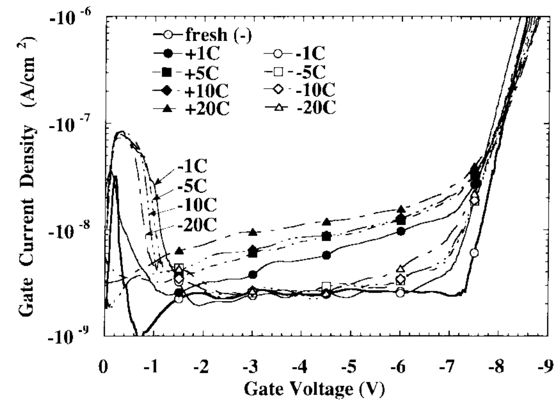
The above polarity dependence of induced leakage currents can be related with the generated positive trapped charges by the stress. Both positive and negative trapped charges are normally generated near the anode upon high field stresses [18], [21]. For $-V_g$ stress, generated positive charges were trapped near the oxide/silicon interface. While for $+V_g$ stress, they were trapped near the gate/oxide interface. Those positive trapped charges modified, i.e., lowered the energy barrier near each interface, thus assisted tunneling when electrons were injected from this interface upon measuring the J-V characteristics. While when the J-V were measured on the other polarity, they did not affect the tunneling barrier since they were far away from the other respective injection interfaces.

In both Fig. 1(a) and (b), the induced leakage currents increase fast for the initial 1 °C stress but their increment gradually decrease after the stressing charges reach 10 °C. This is consistent with the above discussion since the generated positive trapped charges decreases with the injected stressing charges [18], the less generated positive charges after the injected stressing charges reached 10 °C induced less leakage current increment.

In Fig. 1(b), negative differential resistance regions are observed at the initial stage of J-V curves, especially for the $-V_g$-stressed curves. They were caused by neutralization of both inversion charges and interface state charges when the silicon surface was shifted from



(a)



(b)

Fig. 1. Comparison of the (a) positive and (b) negative leakage currents induced by $+10$ and -10 mA/cm^2 stresses with 1, 5, 10, and 20 Coul./cm^2 of total charges injected.

inversion to accumulation [1], [5] during the measurement. For $-V_g$ stresses, they generated charges of which their net charges were positive near the SiO_2/Si interface [18], [21] and caused negative flat-band voltage shift. These net positive charges made the p-type silicon substrate be more inverted at the zero bias. Hence, more currents were resulted to neutralize the inversion charges and the charges of occupied interface states at the initial stages of the negative polarity J-V measurements.

Positive trapped charges are very unstable and easy to be neutralized by a low reverse bias stress [7], [18], [20]. The sequence of the applied stresses of different polarities and magnitudes is very important in determining the generated positive trapped charges [18]–[19]. In consequence, the leakage current is also dependent on the sequence of applied stresses. In the following study, an experiment was done to demonstrate this: capacitor samples were first stressed by a -500 mA/cm^2 with -0.5 Coul./cm^2 of total injected charges, which was to generate some trapped charges in the oxide film, then each of them was re-applied a second ± 1 or a ± 0.1 mA/cm^2 stress, also of the same ± 0.5 Coul./cm^2 of total injected charges.

Fig. 2 shows the gate voltage shifts (ΔV_g) corresponding to the above ± 1 and ± 0.1 mA/cm^2 stresses, respectively, where the results of fresh samples, i.e., the samples which were not applied the first -500 mA/cm^2 stress, are also included. For fresh samples, the voltage shift curves declined first and then increased gradually for the second ± 1 and ± 0.1 mA/cm^2 stresses. These ΔV_g's were determined by the combined effects of both positive and negative trapped charges generated by the stresses in which the positive charges initially dominated and caused ΔV_g to decrease. The amount

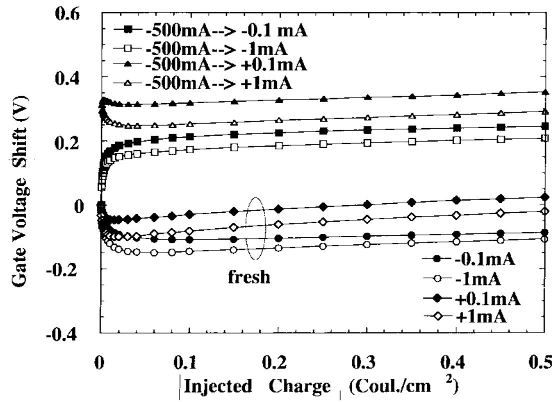


Fig. 2. The gate voltage shifts corresponding to the constant currents ± 1 and ± 0.1 mA/cm^2 stresses. Some samples were pre-stressed by -500 mA/cm^2 with -0.5 Coul./cm^2 of total charges injected. And the latter smaller stresses were added to modify the pre-created trapped charges' distributions.

of positive charges then saturated, while the negative charges kept increasing and caused ΔV_g to increase henceforth [18]. For samples which had been applied the first -500 mA/cm^2 stress, the voltage shift curves behaved quite differently. They were resulted from the disturbance of the existing pre-generated positive charges, in addition to the newly generated trapped charges [18]. Fig. 3, which represents the roughly assumed corresponding changes of both positive and negative trapped charge distributions in the oxide film for the above stressing conditions, can be used to explain the above curves. In the figure, both positive and negative charges were generated and trapped near the anode, i.e., the SiO_2/Si interface [7], [18], [21] for samples stressed by the first -500 mA/cm^2 stress. After the following -0.1 mA/cm^2 stress, the lower field disturbed the trapping and detrapping of positive charges [18], [19], caused some positive charges to recombine with the injected electrons and at the same time generated a small additional amount of negative trapped charges. Thus, in Fig. 2, the -0.1 mA/cm^2 stress curve increased rapidly initially due to recombination of the positive charges with the injected electrons and then increased slowly due to generation of negative trapped charges. For the -1 mA/cm^2 stress curve, the same situation occurred except that a smaller amount of the positive trapped charges were neutralized [18]. This was the reason why its ΔV_g curve had a smaller initial increment than that of the -0.1 mA/cm^2 stress curve. In Fig. 3, for the $+0.1$ mA/cm^2 stress case, since electrons were injected from the SiO_2/Si interface, all the positive charges near this SiO_2/Si interface were neutralized but with the negative charges nearly undisturbed [18]. This neutralization caused their ΔV_g curves in Fig. 2 to rise up abruptly at the very initial stressing stage. In addition, at the same time, some extra positive and negative charges were generated near the gate/SiO_2 interface, which led the ΔV_g curves to behave just like those of the fresh samples stressed by $+1$ or $+0.1$ mA/cm^2 only.

Fig. 4(a) and (b) shows the corresponding positive and negative leakage currents, respectively, induced by the above stressing conditions, where the leakage currents of the fresh sample, i.e., no stress at all, are also included. Just after the first -500 mA/cm^2 stress, the induced leakage current was only observed at the positive J-V measurement curve due to the generated positive charges trapped near the SiO_2/Si interface. However, after the second reverse $+1$ or $+0.1$ mA/cm^2 stress, this positive leakage current disappeared due to neutralization of positive charges [14]. However, for the negative J-V measurement curves, those samples showed the induced negative leakage currents due to the newly generated positive charges trapped near the gate/SiO_2 interface. As for the samples applied with the

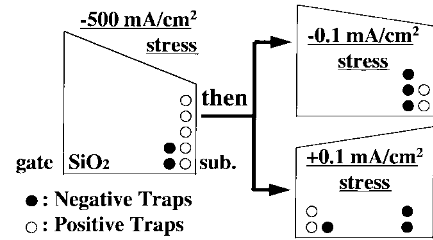
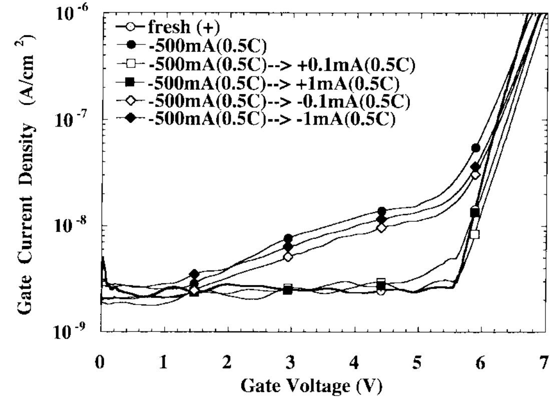
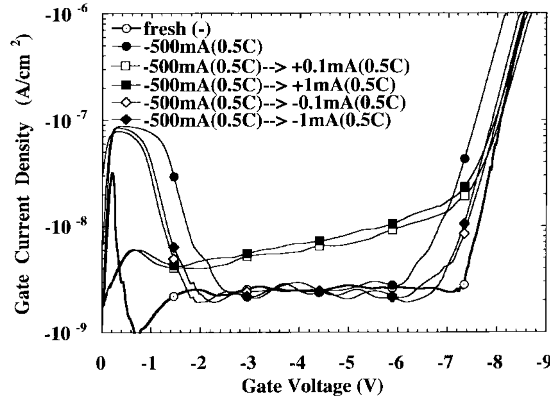


Fig. 3. The assumed variation of both positive and negative trapped charges' distributions in the oxide film, with samples pre-stressed by -500 mA/cm^2 and then by ± 0.1 mA/cm^2, all with 0.5 Coul./cm^2 of total injected charges.



(a)



(b)

Fig. 4. The transformations of (a) positive and (b) negative leakage currents before and after the ± 1 or ± 0.1 mA/cm^2 stresses. The leakage currents were pre-induced by -500 mA/cm^2 stresses. And each stressing steps had 0.5 Coul./cm^2 of total charges injected.

second -1 or -0.1 mA/cm^2 stress, since these stresses neutralized only part of the positive trapped charges and did not generate positive charges trapped near the interface at the other end of the oxide, the positive leakage currents only declined a little as compared to the original -500 mA/cm^2 stress curve, and no newly induced negative leakage currents are observed except for positively parallel shifts of the J-V curves.

IV. Conclusions

In this work, it has been shown that the excess pre-Fowler–Nordheim leakage current induced by the electrical stress is related with the generated positive trapped charges. It has been demonstrated that the centroid of the positive trapped charges, which depends on the polarity of the stress current, affects the

magnitude of the leakage current. In addition, it has been shown that the leakage current depends on the magnitude of the final applied stress because the final trapping density of positive charges is determined by the final applied field on the oxide. When the positive charges are neutralized, the leakage current decreases.

The above results give a good understanding on the origin of the excess stress-induced leakage current and offer a way to control the leakage current by suppressing the stress generated positive charges.

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