Numerical Simulation of the Hysteresis in the Sidegating Effect in GaAs MESFET's—The Effect of Schottky Contacts

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Abstract—**Two-dimensional simulation of the sidegating effect in GaAs MESFET's has been performed. The result confirms that Schottky contacts on semi-insulating substrate cause serious high substrate leakage current and drain current reduction in GaAs MESFET's. The competition between the currents or biases of the contacts is found to be the cause of the S-type negative differential conductivity (S-NDC) or hysteresis observed when measuring the sidegating threshold.**

HYSTERESIS and S-type negative differential conductivity (S-NDC) are commonly observed when measuring the threshold behavior of the sidegating effect in GaAs MESFET's in the voltage-controlled condition and the current-controlled condition, respectively. These features have been explained based on impact ionization of deep traps in the substrate by Li *et al.* [1], [2]. However, recent studies [3]–[5] have recognized that Schottky contacts on the semi-insulating substrate play an important role in the sidegating effect in GaAs MESFET's. Our previous simulation results have also shown that the Schottky contact can cause, enhance, or shield the sidegating effect [6]. Therefore, the effect of the Schottky contacts should be considered in the observed hysteresis or S-NDC in the sidegating effect, as in the simulations to be presented in this letter.

For numerical simulation, a two-dimensional, two-carrier, steady-state device simulation program based on the drift-diffusion formulation was developed. In this program, transport of free carriers is calculated by solving current continuity equations and the Poisson's equation. The emission and capture of free carriers through deep traps in the substrate follow the Shockley–Read–Hall model. Constant electron mobility at low fields and velocity saturation beyond a critical field were used for the velocity-field relationship in simulation.

The semi-insulating substrate was assumed to contain deep donors that compensate for shallow acceptors, similar to the case of undoped LEC stubstrates. The properties of the traps in the substrate, which include the capture cross sections and energy levels of the deep traps, are summarized in Table I. The capture cross sections used are the same as those used by Goto and Ohno [4]. In addition to the EL2 like deep donors which act as electron traps, deep levels acting as hole traps were also included. The existence of hole traps has been found essential to the sidegating effect [4], [6], although similar results can be obtained if the hole traps were deep acceptors instead of deep donors.

In the simulation, a true sidegate configuration is adopted, where the sidegate is placed at the top surface of the substrate along with all other contact terminals as shown in Fig. 1. The FET had a 1-μm gate with a 3-μm source-to-drain spacing. The FET channel was 0.12 μm thick and was uniformly doped to 10^{17} cm^{-3}. The sidegate was placed 8 μm away from the FET. A 1-μm-wide Schottky bar contacting the semi-insulating substrate (i-substrate) was placed in between the sidegate and the FET, 4 μm away from the sidegate. This Schottky bar, which may be regarded as a part of the Schottky gate that extrudes out of the active region and contacts the i-substrate or any interconnection metal that contacts the substrate, has been found to be essential to the sidegating effect [3]–[6].

The calculated drain current I_{dss} and sidegate leakage current I_{bg}, as functions of the negative sidegate voltage with different drain biases V_{ds}, are shown in Fig. 2(a) and (b), respectively. The gate, source, and the Schottky bar are all grounded. This corresponds to the voltage-controlled condition. It can be seen in these plots that a significant reduction of the drain current and an abrupt increase of the sidegate leakage current occur when a threshold voltage is reached. The drain current continues to drop and the leakage current continues to increase after the threshold. However, when the negative sidegate voltage is reduced after the onset of the sidegating, the sidegating characteristics (Fig. 2(a) and (b)) follow different paths and show apparent hysteresis. There are no sudden increase in the drain current and sudden decrease in the leakage current. The threshold voltages are also smaller. Both the negative threshold voltage and the amount of hysteresis increase with the drain bias. These features are in qualitative agreement with the commonly observed experimental results [1], [2]. (Although the structures in those experimental studies may not purposely include a Schottky contact, the gate contact pad, the part of the Schottky gate that extrudes out of the active region,

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TABLE I
PROPERTIES OF TRAPS IN THE SUBSTRATE

Category	Concentration (cm^{-3})	Electron Capture Cross Section (cm^2)	Hole Capture Cross Section (cm^2)	Energy Level E_c-E_t (eV)
electron trap	10^{16}	1×10^{-13}	3×10^{-16}	0.715
hole trap	10^{15}	3×10^{-16}	1×10^{-13}	0.745
shallow acceptor	10^{15}	—	—	—

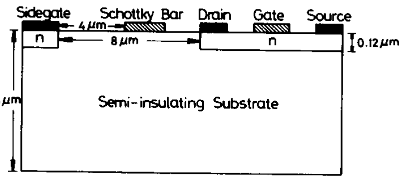
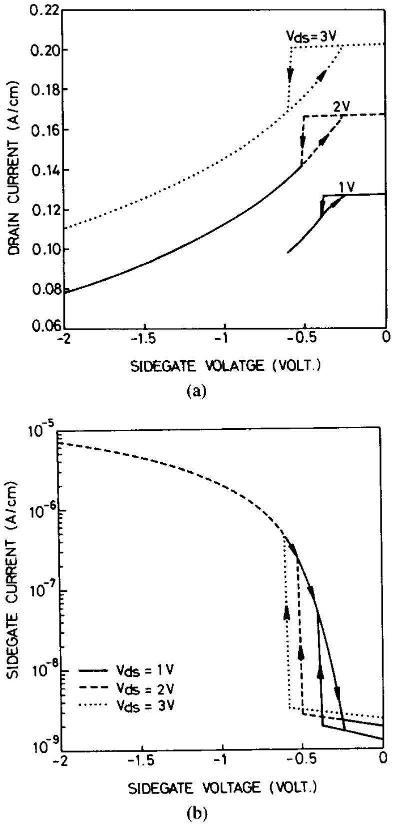


Fig. 1. The device structure used for numerical simulations. Donor concentration of the n-doped regions is 10^{17} cm^{-3}.



(a)

(b)

Fig. 2. (a) Calculated FET drain current and (b) sidegate current as functions of the sidegate voltage with the drain of the FET biased at 1 V (solid lines), 2 V (dashed lines), and 3 V (dotted lines). The gate, source, and the Schottky bar are grounded.

or any interconnection metal which contacts the substrate can be regarded as the Schottky contact used in the simulation.) Besides, the sidegate currents increase with the drain bias before the onset of sidegating effect and become independent of the drain bias after the abrupt increase at sidegating threshold (see Fig. 2(b)). When the negative sidegate bias is decreased again, the sidegate currents follow the same curve until their respective current levels before the onset of sidegating is reached.

Based on the above simulation results, the observed hysteresis can be explained as the result of the competition between the contact currents or biases. 1) The potential of the i-substrate around the Schottky bar is affected by the positive bias applied to the drain of the FET, the negative voltage applied to the sidegate, and the bias applied to the bar itself. 2) Before the application of negative sidegate voltage, the current flow through the Schottky contact is the reverse saturation current of the n(FET)-i-Schottky structure. When the applied negative sidegate voltage is small, the potential around the Schottky bar is dominated by the effect of the drain bias (the Schottky bar current remains to be the small reverse saturation current from the FET side) and the sidegate current is dominated by the n(FET)-i-n(sidegate) current. Only when the negative bias applied to the sidegate is large enough to overcome the effect of the drain bias of the FET does the current between the Schottky contact and the sidegate begin to flow as it should in a forward-biased Schottky-i-n(sidegate) structure. After the onset of forward Schottky-i-n current, the Schottky bar current reverses sign, increases very rapidly, and dominates the sidegate current as shown in Fig. 3. It has been shown in [6] that holes injected from this Schottky contact can be transported through the substrate to the FET side with the aid of hole traps. This extension of hole accumulation region causes the potential profile to be nearly flat in the whole i-substrate region with most of the voltage drop across the FET's channel–substrate interface junction and results in the sidegating effect. 3) When the negative sidegate voltage is reduced after the onset of the sidegating effect, the potential around the Schottky bar is predominantly affected by the sidegate bias. Therefore, the sidegate characteristics continue to follow those of the forward-biased Schottky-i-n(sidegate) structure until the current levels are reduced to those of the n(FET)-i-n(sidegate) current before sidegating.

To explain the S-type negative differential conductivity (S-NDC) in the sidegating characteristics in the current-controlled measurement [1], [2], the current–voltage characteristics of the n(FET)-i-n(sidegate) were simulated with the Schottky bar (in Fig. 1) floating and the drain biased at 2 V (see Fig. 3). It is found that the resultant n(FET)-i-n(sidegate) current is several orders lower than the forward Schottky-i-n(sidegate) current after the onset of the

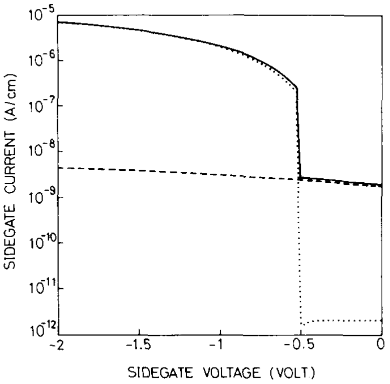


Fig. 3. Calculated sidegate current (solid line) and the value of the Schottky current (dotted line) as functions of the sidegate voltage with the Schottky bar grounded. The calculated sidegate current (dashed line) with the Schottky bar floating is also shown for comparison. The drain of the FET is biased at 2 V.

sidegating effect at the same sidegate voltage. Therefore, the S-NDC can be explained as follows: when a negative current (flowing out of the electrode) I_{sg} is applied to the sidegate as in the current-controlled measurement, the current–voltage characteristics of the sidegate would initially follow those of the n(FET)-i-n(sidegate) structure when the driving sidegate current is low. The Schottky bar remains reverse biased by the positive drain bias of the FET. After the driving source (I_{sg}) has been increased to a critical level, the Schottky-i-n(sidegate) structure starts to conduct, shunts most parts of the n(FET)-i-n(sidegate) path, and dominates the sidegate current. Since the current level of the forward Schottky-i-n current is much higher than that of the n-i-n current at the same sidegate voltage, when the sidegate current is continuously increased as in the current-controlled measurement, there would be an abrupt decrease in the sidegate voltage at the sidegating threshold. Therefore, it is the transition of the sidegate current from the n-i-n current to the Schottky-i-n current that causes the S-NDC feature.

The recent experimental study by Liu *et al.* on the Schottky contact effects on the sidegating characteristics [7] has also shown results and conclusions which agree well with the above pictures of hysteresis and S-NDC drawn from our simulations.

In conclusion, we have performed two-dimensional simulations on sidegating effect in GaAs MESFET's with a realistic configuration, where both the FET and the sidegate are placed on the surface of the substrate. The simulated results are in good agreement with the observed features of hysteresis or S-NDC in the sidegating effect. The hysteresis or S-NDC associated with the threshold behavior of the sidegating effect is found to be related to the leakage current of the Schottky-i-n(sidegate) structure under the influence from the biases of the FET.

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