Characteristics of Poly-Si Nanowire Transistors with Multiple-Gate Configurations

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INTRODUCTION

Si nanowire (NW) has recently received considerable attentions owing to its great potential in device applications. NW structure features a high surface-to-volume ratio, making it extremely sensitive to the variation of surface conditions, suitable for a number of device applications, including NW FETs [1], nonvolatile memories [2], and sensors [3]. Preparations of NW structures can be divided into bottom-up and top-down categories. The former is flexible in preparing the NW composition and structure, but lacks of controllability over precise positioning and alignment of NW patterns, thus not suitable for manufacturing. On the other hand, top-down methods typically employ advanced but costly lithography tools like e-beam technique or DUV steppers to generate the NW patterns. To address these issues, we've recently proposed and developed a simple NW EFT fabrication method which used sidewall spacer etching technique to define poly-Si NWs serving as the device channel [4][5], and demonstrated that most advantages pertaining to the NW structure could be retained with the new scheme. However, our proposed devices are with poly-Si NWs as the channels. Defects contained in the poly-Si material may impede carrier transport and degrade device performance. This concern may be relaxed with multiple-gate (MG) configuration. In this work, we fabricate and characterize two types of MG devices. Adjustment of device threshold voltage with independent gate control scheme is also investigated.

DEVICE STRUCTURE AND FABRICATION

The two types of device structures are illustrated in Figs.1 and 2. The device fabrication shown in Fig.1 is similar to that described in our previous work, except that the formation of a top gate is added. The second type of structure shown in Fig.2 applied twice the lithography/etching process to form an inverse-T gate, followed by the formation of NW channels. Note that the height of upper step of the inverse-T gate was designed to be higher than the lower one, so in the process we could control the etching time to allow only two NW channels to remain on the upper-step corners of the inverse-T gate. The remaining process sequence is the same as that for the former structure. TEM pictures of the devices are shown in Fig. 1(c) and Fig. 2(c). Thickness of gate oxide is about 20nm. Dimensions of the NW structures are different in the two cases, owing to the difference in step height and profile of the sidewall.

RESULTS AND DISCUSSIONS

Transfer characteristics of the two types of devices under single-gate (SG) or double-gate (DG) modes of operation are shown in Figs. 3(a) and (b). It can be seen clearly that the characteristics are dramatically improved as the two gates are tied together, thanks to the enhancement of gate controllability over the NW channels. Under the DG mode, subthreshold swings of 130 and 90 mV/dec. are achieved for the two types of devices. The latter case shows better characteristics. This is ascribed to its thinner body as well as the use of inverse-T gate. From the TEM image shown in Fig. 2(c), the NW channel is almost fully surrounded by the inverse-T gate and the top-gate, ensuring a good gate coupling during the DG mode of operation.

Separate gates in an MG configuration can increase the flexibility in device operation. Figure 4 shows the ability of the device in modulating the threshold voltage by the bias ranging form -3 to 3 V applying to the top gate. In the figures, the transfer characteristics are clearly shifted by varying the gate voltage. Threshold voltage and subthreshold swing as a function of top gate bias are shown in Fig. 5. The phenomena and trends we observed are basically consistent with those presented in previous work [6]. However, the device with inverse-T gate clearly shows stronger gate-to-gate coupling effect.

CONCLUSIONS

In this work, two types of poly-Si nanowire (NW) transistors with multiple-gate (MG) configuration were fabricated and characterized. The devices are equipped with two independent gates to increase the gate controllability and device operation flexibility. With such MG configurations, excellent device performance is demonstrated, despite the use of poly-Si NW. For one of the MG configuration featuring an inverse-T gate, subthreshold swing as low as 90 mV/dec is achieved. The adjustment of threshold voltage with top-gate bias control is also explored in this work.

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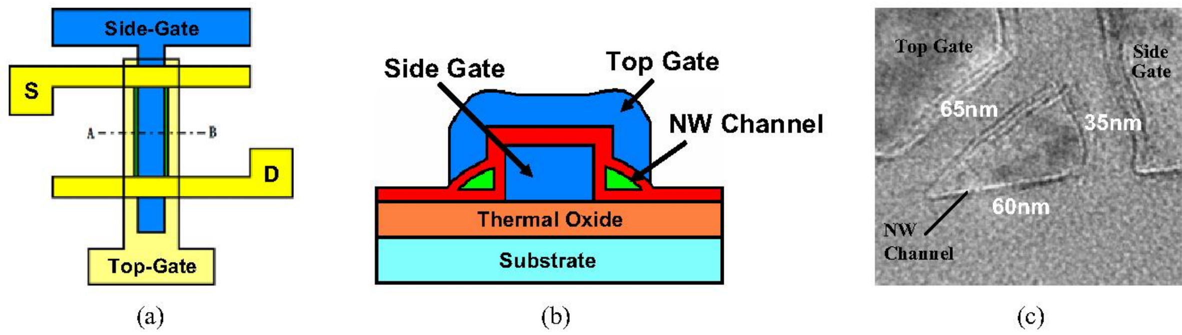


Fig. 1 (a) Top view, (b) cross-sectional structure and (c) cross-sectional TEM view of the NWTFT with side-gate and top-gate structure.

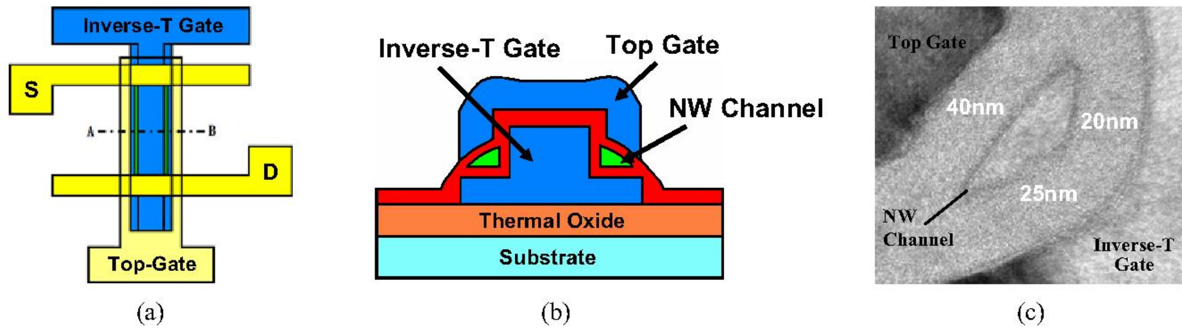
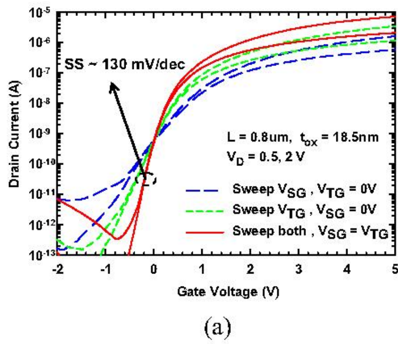
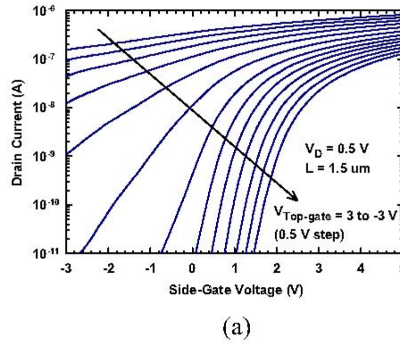


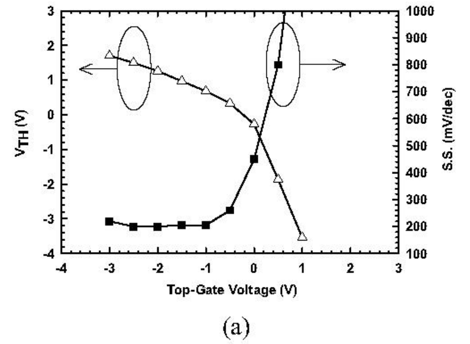
Fig. 2 (a) Top view, (b) cross-sectional structure and (c) cross-sectional TEM view of the NWTFT with inverse-T-gate and top-gate structure.



(a)



(a)



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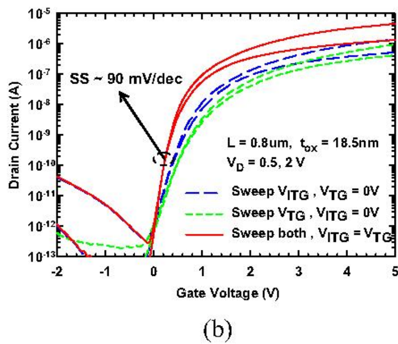
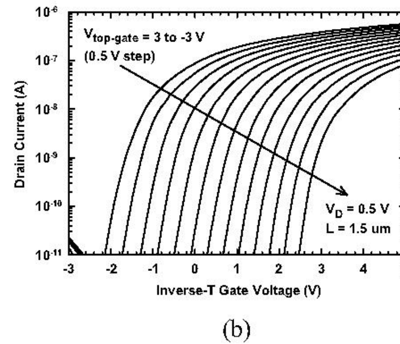
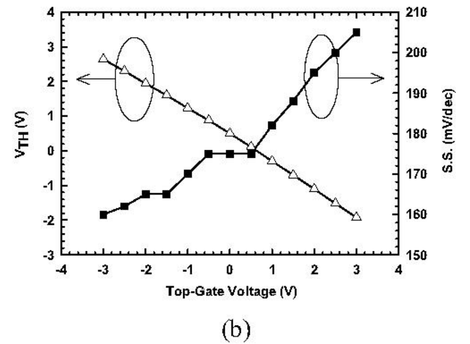


(b)



(b)



(b)

Fig. 3 Transfer characteristics of (a) type-I (Fig.1) and (b) type-II (Fig.2) devices.

Fig. 4 Transfer characteristics of (a) type-I and (b) type-II devices with various top-gate biases.

Fig. 5 Extracted V_{TH} and S.S. as a function of top-gate biases for the results shown in Fig.4.