High Charge Storage Characteristics of CeO_2 Nanocrystals for Novolatile Memory Applications

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ABSTRACT

This paper presents the formation of CeO_2 nanocrystals on SiO_2 tunneling layer and its annealing effect to the nonvolatile memory device. The characteristics including the program/erase behaviors, data retention, and endurance of Silicon-Oxide-Nitride-Oxide-Silicon type memories embedded with cerium oxide (CeO_2) nanocrystals were studieded to demonstrate its advantages as a nonvolatile memory device.

Ⅰ. INTRODUCTION

Si and metal nanocrystals (NCs) are widely studied as potential solutions to overcome the scaling limitations of the conventional flash memories for future nonvolatile, high density, and low power memory devices[1]. Cerium dioxide (CeO_2) has been extensively studied as an electrolyte material of solid oxide fuel cells[2]. The properties of CeO_2 such as lattice nearly matched to silicon (a=0.5411nm) and sufficiently high dielectric constant (~26)[3] lead to the high thermal stability on silicon and high scaling capacity. Recently, high-κ dielectric NCs on the SiO_2 tunnel layer for SONOS-type memories have been proposed. Lin *et al*[4]. reported a method of co-sputtering Hf and Si in oxygen followed with high-temperature annealing to form the high-κ NCs for SONOS-type memory devices. However, the HfO_2 nanocrystal memory exhibit saturation windows in channel-hot-electron (CHE) program mode. You *et al*[5]. have proposed the sol-gel spin-coating method to form the high-κ NCs. This method may increase thickness of tunnel oxide and results in high operation voltage.

In this work, the CeO_2 NCs were formed by thermal annealing in different ambients. SONOS-type memories were fabricated, and the electrical properties, including the P/E speed and data retention characteristics were investigated.

Ⅱ. EXPERIMENT

An nMOSFET with CeO_2 nanocrystal flash memory structure is schematically shown in Fig. 1. A thin CeO_2 layer was then deposited on SiO2 tunneling layer by an electron-beam evaporator at 10^{-6} Torr. The samples subsequently underwent RTA at 900 °C for 1 min in either O_2 or N_2 ambient to form CeO_2 NCs (RTO and RTN samples), respectively. Finally, the CeO_2 NC memory devices were completed after the substrate contact patterning and metallization. The electrical properties of such devices were measured using HP 4156B semiconductor parameter analyzer and HP 41501A pulse generator. The charge pumping measurement was performed with Keithley 4200 semiconductor parameter analyzer and HP 8110 pulse generator.

Ⅲ. RESULTS AND DISCUSSION

The cross-sectional transmission electron microscopy (TEM) images of the CeO_2 NCs embedded in the SiO_2 matrix for RTO and RTN samples are shown in Fig. 2. No obvious different in microstructure in terms of NC size and disturbution are formed between annealed samples. They showed a NC density of $3\sim7\times10^{11}$ /cm^2. The average NC size was 8-10 nm. Crystallized NCs with obviously visible lattice fringes were evident in the insets.

Figure 3 shows the I_{ds}-V_{gs} curves of CeO_2 nanocrystal memory cell with different programming and erasing conditions. The device is programmed by CHE injection and erased by band-to-band hot-hole (BBHH) injection. The programming speed of the CeO_2 NCs memory devices with RTN and RTO annealing is shown in Fig. 4. When the program voltage increases to 10 V, the V_{th} shift increases rapidly and a memory window greater than 5 V is achieved within 1 ms. This large memory window make the multilevel operation possible. The fact the programming speed is indepentent of annealing condition of the charge trapping centers, indicating that the programming speed is primarily dependent on the tnunneling oxide. Figure 5 shows the erasing speeds characteristics at different voltages with a fixed V_d of 10 V. As observed, an increase in the negative gate bias resulted in a high erasing speed due to the higher electrical field for BBHH injection. A fully erased state was fulfilled within 1 ms at V_g = -7 V and V_d = 10 V.

Figure 6 shows the data retention characteristics of the CeO_2 NC memory devices at two programming states. The RTN sample showed a smaller amount of charge loss than the RTO at room temperature for retention time up to 10^4 s. It is conjectured that the bulk traps of RTN sample is deeper than RTO sample so that the charge loss of RTN sample is less than RTO sample. The electrons can be either trapped in these bulk defects or stay in the conduction band of the CeO_2 NCs and/or in the interface states between the CeO_2 NCs and SiO_2[6]. Figure 7 shows the endurance characteristics of the CeO_2 NC memory devices after 10^4 P/E cycles. It is found that the memory window of the NC devices is not narrowing even after 10^4 P/E cycles. The narrowing mainly comes from charge gain when the electron distribution does not completely match that for the hole. Each P/E cycle will leave a few electrons in the trapping layer[5]. The charge-pumping[7] mesurement by change base voltage at fixed pulse amplitude was conducted to determine the defect density and states shown in Fig. 8. The RTN sample has larger charge-pumping current than the RTO sample, which can be attributed to the more trapping defect states in the RTN sample. This is consistent with the better data retention of the RTN sample observed in Fig. 6.

Ⅳ. CONCLUSION

We have demonstrated P/E window (5V within 1ms at V_g = 10V) of CeO_2 NCs memory devices. The RTN CeO_2 NCs trapping layers have a larger charge storage capacity and a longer retention time than the RTO sample due to deeper trap center. It is concluded that CeO_2 NCs can be used as discrete charge trapping sites for the SONOS-type memories.

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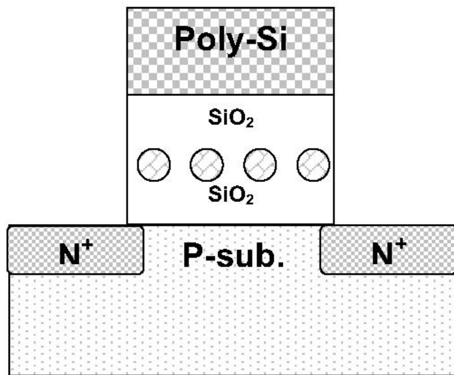

Fig. 1. Schematic structure of CeO_2 nanocrystal memory cell.

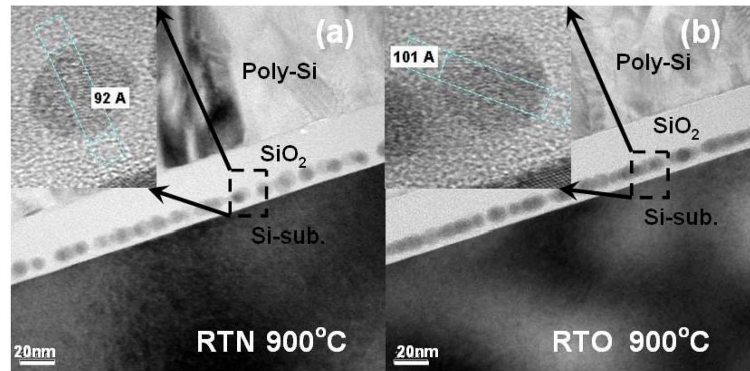

Fig. 2. Cross-sectional TEM image of the CeO_2 nanocrystals embedded in SiO_2 dielectric matrix : (a) with N_2 annealing 900℃ for 1min and (b) with O_2 annealing 900℃ for 1min.

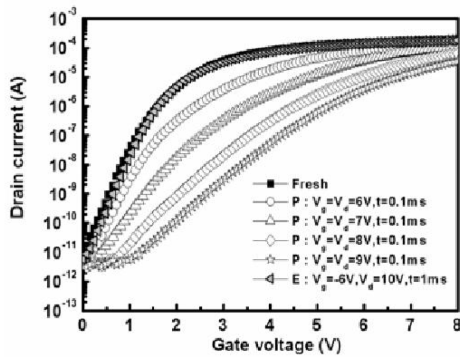

Fig. 3. I_{ds}-V_{gs} curves of the memory cell with different programming conditions. V_{th} is defined as the applied voltage at which the drain current is 0.1 μA.

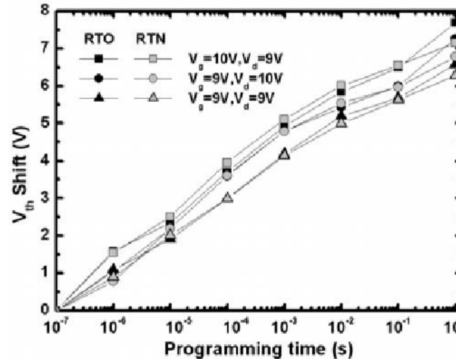

Fig. 4. Programming speed characteristics of CeO_2 nanocrystal memory devices with different programming conditions.

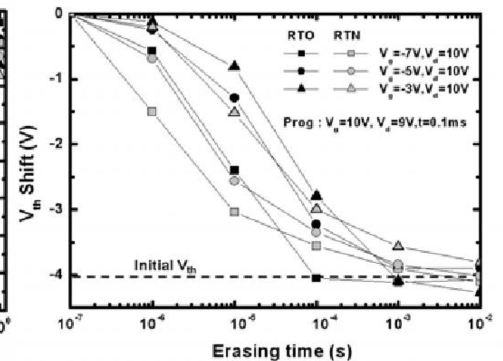

Fig. 5. The erasing speed characteristics of the CeO_2 nanocrystal memory cell at different erasing voltages.

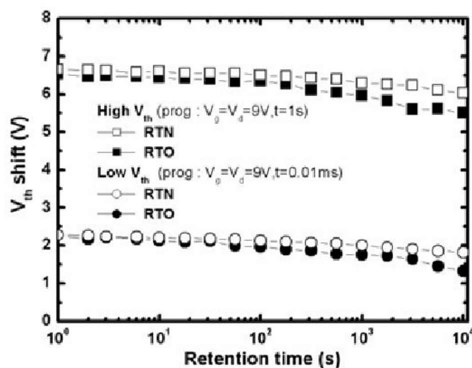

Fig. 6. Data retention of CeO_2 nanocrystal memory devices with different RTA treatments.

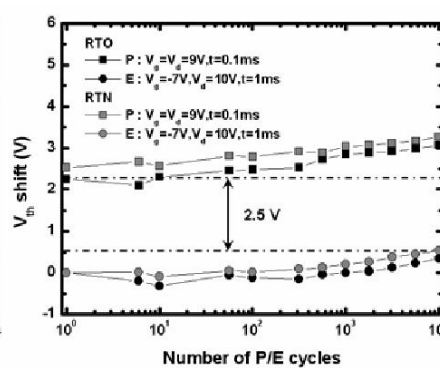

Fig. 7. The endurance characteristics of CeO_2nanocrystal memory devices with two different treatment devices.

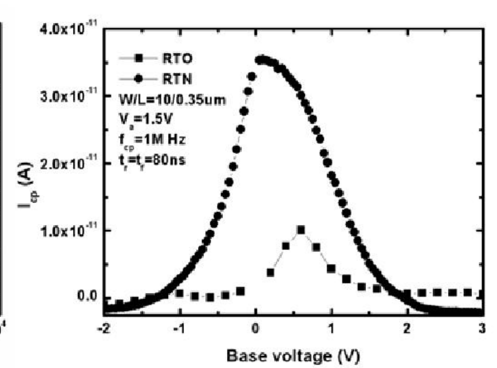

Fig. 8. Charge pump current (I_{cp}) of CeO_2 NC device as a function of base voltage at fixed pulse amplitude.