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IMAGE INTERPOLATION BY ANALOGUE CIRCUIT

H.-C. Hsieh and W.-T. Chang

Indexing terms: Image processing, Analogue computers, Circuit design

An analogue computation circuit is proposed for image interpolation. This circuit is designed to maximise the smoothness of the interpolated data. With this circuit, high speed interpolation can be easily achieved.

Introduction: Interpolation is widely used in image processing. Various methods have been proposed [1]. However, most of those methods are limited in speed and are not efficient for real-time applications. Recently, high speed interpolation has become desirable in many real-time applications such as visual communication, advanced television systems, etc. For high speed computation, analogue computation has been an attractive approach [2, 3]. In this Letter, an analogue computation circuit is proposed for image interpolation.

In classical interpolation methods, lowpass filtering is commonly used for smoothing the interpolated data. In the proposed method, instead of lowpass filtering, an optimisation process is used to maximise the smoothness of the interpolated data. The advantage of maximising the global smoothness is that a set of simultaneous equations can be derived. This set of equations can be transformed to the node equations of a resistive circuit. By this, an analogue computation circuit for interpolation can be derived.

Analogue computation circuit: Let us first consider the interpolation of a one-dimensional sequence and denote it as v_i for $i = 0, 1, \ldots, N$. Without loss of generality, let $N = kM$ where k is an integer. Assume those samples v_i, for $(i \bmod M) = 0$, are known and the others are to be interpolated.

The global smoothness of the interpolated sequence can be maximised by minimising the following variation function:

$$v = \sum_{i=0}^{N} [v_{i-1} - 2v_i + v_{i+1}]^2 \tag{1}$$

where the second order finite difference is used to measure the variation of the sequence. Note that those two samples v_{-1} and v_{N+1} may not be defined. In such a situation, they can be defined as $v_{-1} = 2v_0 - v_1$ and $v_{N+1} = 2v_N - v_{N-1}$.

Because v is a quadratic convex function, its minimum is obtained under the Euler condition

$$\frac{\partial v}{\partial v_i} = 0 \tag{2}$$

for all $(i \bmod M) \neq 0$. With this, a set of equations are obtained

$$\begin{cases} -2v_0 + 5v_1 - 4v_2 + v_3 = 0 & i = 1 \\ -2v_N + 5v_{N-1} - 4v_{N-2} + v_{N-3} = 0 & i = N-1 \\ v_i = v_i & i \bmod M = 0 \\ v_{i-2} - 4v_{i-1} + 6v_i - 4v_{i+1} + v_{i+2} = 0 & \text{otherwise} \end{cases} \tag{3}$$

These equations can be rewritten as

$$\begin{aligned} &2(v_0 - v_1) + 4(v_2 - v_1) - (v_3 - v_1) = 0 && i = 1 \\ &2(v_N - v_{N-1}) + 4(v_{N-2} - v_{N-1}) - (v_{N-3} - v_{N-1}) = 0 && i = N-1 \\ &v_i = v_i && i \bmod M = 0 \\ &-(v_{i-2} - v_i) + 4(v_{i-1} - v_i) + 4(v_{i+1} - v_i) - (v_{i+2} - v_i) = 0 && \text{otherwise} \end{aligned} \tag{4}$$

These equations can be transformed to the node equations of a resistive circuit. Therefore, a resistive circuit can be constructed to solve the desired sequence. The graph of this circuit is shown in Fig. 1. The connection of this circuit is regular except at the two ends. The labels in Fig. 1 indicate the conductance values of the connecting resistors. In the implementation, voltage inverters can be used for negative conductances.

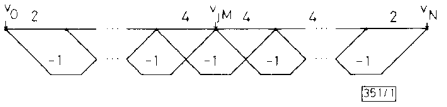

Fig. 1 *Graph of proposed circuit*
Labels indicate conductance values of connecting resistors

The usefulness of this circuit is that the interpolation process can be achieved within an instant. Each node of the circuit is related to one sample of the interpolated sequence. To interpolate a sequence, the known samples are applied as a voltage source at corresponding nodes. The solution of the interpolated sequence can be accessed from the other nodes as soon as the input is applied. For image interpolation, the data can be interpolated row by row first and then column by column.

To investigate its performance, image data are interpolated by this circuit via computer simulation. For comparison, the same data are also interpolated by the conventional *sinc* interpolation. A truncated Hamming-*sinc* lowpass filter is used in the *sinc* method. For both methods, the data are interpolated first row by row and then column by column. The results of the experiment are shown in Fig. 2. The original image is first decimated by two and then interpolated by both methods.

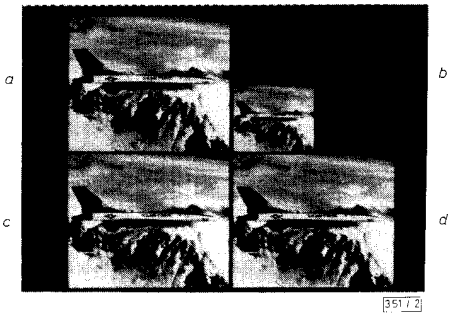

Fig. 2 *Original image, decimated image, image interpolated by proposed method, and image interpolated by sinc method*
a Original
b Decimated ($M = 2$)
c Interpolated by proposed method
d Interpolated by *sinc* method

Another experiment with a decimation factor of four is shown in Fig. 3. It can be seen that the performance of the proposed method is compatible with that of the conventional method.

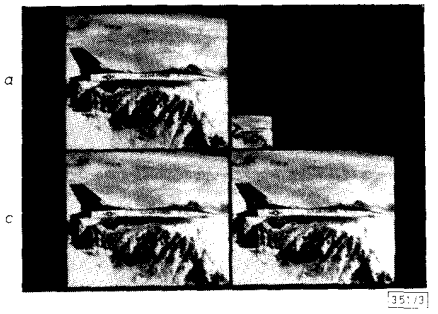

Fig. 3 *Original image after preprocess of lowpass filter, decimated image, image interpolated by proposed method, and image interpolated by sinc method*

a Original
b Decimated ($M = 4$)
c Interpolated by proposed method
d Interpolated by *sinc* method

Conclusion: An analogue circuit has been derived for image interpolation. Experimental results show that this circuit yields acceptable performance. With its regular structure, it is suitable for integrated circuit implementation to achieve high speed interpolation.

10th March 1992

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GRADUALLY-ON STRUCTURE FOR SCAN DESIGN

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Indexing terms: Built-in selftest, Integrated circuits

A new structure named the gradually-on (GO) structure for the full/partial scan design of sequential circuits is proposed. Because this structure allows the scan cells to be turned on gradually, the total test application time can be dramatically reduced.

Introduction: Design for testability (DFT) is a method for simplifying the testing problem of sequential circuits. Among DFT techniques, scan design approaches now attract the most attention. The proposed scan design approaches can be classified into full scan design [1] and partial scan design [2–5].* No matter which approach is adopted, a considerable proportion of the actual testing time is spent in scanning in/out the content of the scan chain, an operation which requires a number of clock pulses equal to the length of the scan chain.

In this letter, the gradually-on (GO) structure is introduced to reduce the test application time by adding a small amount of extra hardware. To indicate the superiority of the GO structure over conventional structures, it is convenient to classify the faults in a circuit under test (CUT) into four types. By investigating the influence of scan design on each type of fault, it is easy to conclude that the total test application time of the GO structure is less than that of conventional structures.

GO structure: For traditional scan structures, all the scan cells would be turned on (or off) simultaneously. Usually, it is not necessary for a certain fault to be detected by scanning so many flipflops. For these approaches, the test application time for the test sequence of length $|T|$ by scanning n flipflops is

$$TAT = (n + 1) \times |T| + n \quad (1)$$

If the number of n could be adjusted to fit the requirement of detection of the target fault, the test application time could be reduced dramatically. The basic idea of the GO structure is to allow the scan cells of the scan chain to be turned on gradually.

The topology of the GO structure is shown in Fig. 1. Without increasing the number of I/O pins, an extra shift register, named the mode control register (MCR), as shown in the shaded block, is added to control the mode of each traditional scan cell such that the scan chain can be turned on gradually. The extra multiplexer-like function block is added to choose the scan-out path from the last turn-on scan cell and the select lines of this block are composed of the outputs of the MCR.

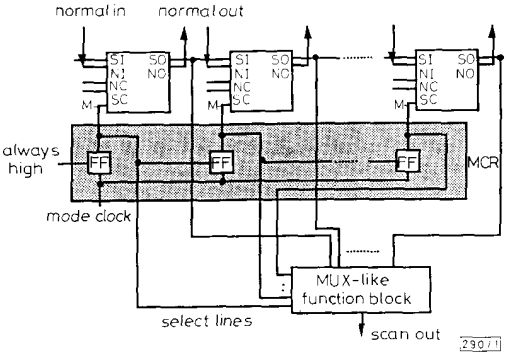

Fig. 1 *Topology of GO structure*

SI: scan input, NI: normal input, NC: normal clock, SC: scan clock, M: mode (on/off), SO: scan output, NO: normal output, FF: flipflop

Test scheme for GO structure: Because the GO structure allows the scan cells to be turned on gradually, the test sequence will be divided into n groups if there are n scan cells in the scan chain. Let T_i represent the test sequence while i scan cells are turned on. Initially, all scan cells are off. T_0 is applied to the CUT and the mode and scan clocks are held. After T_0 is finished, the mode clock should be active to turn on the first scan cell in the scan chain, then the scan data can be scanned into the scan cell by triggering the scan clock. In the meantime, the contents of the scan cell are also scanned out. Now, the first vector in T_1 can be applied to the CUT. The procedure for testing this type of circuit is described as follows:

(1) initially, the MCR is 0

(2) apply T_0 to the CUT

(3) send a mode clock to turn on the ith scan cell (initially, $i = 1$)

(4) scan out the contents of the turn-on cell(s) while scanning data into the turn-on scan cell(s)

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