x and *y* directions can be aribtrarily adjusted by combining the variation of *B* and *C*.
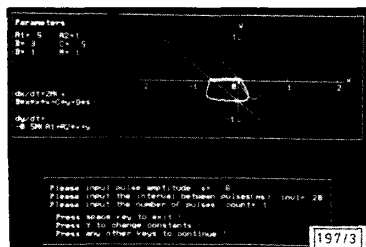

Fig. 3 *Effect of parameter B on shape of x-nullcline*

The effect of parameter *M* can be clearly observed from the curves of *x* and *y* against time, as shown in Fig. 4. Parameter *M* only affects the refractory period, and exerts no influence on the amplitudes of *x* and *y* and the threshold. When *M* increases, the refractory period is linearly shortened, otherwise it is extended.
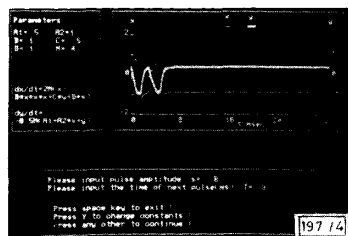

Fig. 4 *Effect of parameter M on refractory period*

Refractory period can be arbitrarily adjusted by varying *M*

Discussion: A neuron model with dynamically adjustable threshold, refractory period and response amplitude is proposed, which meets the needs of pulse-stream neural nets. The above analysis shows that the parameters in eqns. 1 and 2 have an obvious impact on the performance of the model. We can adjust the parameter values to make the model satisfy any given performance, whereas it is impossible to do so in the FitzHugh-Nagumo model. For example, parameters *B* and *C* are first adjusted to guarantee the amplitudes of *x* and *y*. Next, A_1 and A_2 are adjusted to select suitable equilibrium point. We can then adjust *D* to select any given threshold. Finally, *M* can be adjusted to select the required refractory period.

There are still problems in the learning of pulse-stream neural nets. It was noted that reinforcement learning is suitable for training this type of neural network [10]. The authors think that evolutionary learning or genetic algorithms are potential candidates. We have applied nets composed of the neurons described by eqns. 1 and 2, trained through evolutionary learning, to solve the XOR problem. In the experiment, the input and output are encoded into pulses, '1' is represented by pulse signal of a certain frequency, and '0' is represented by a signal without pulses. The experiment shows promising results.

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INTERACTION OF COBALT AND FIELD OXIDE DURING LOW TEMPERATURE FURNACE ANNEALING

B.-S. Chen and M.-C. Chen

The interaction of cobalt and thermally grown field oxide (5000 Å) during low temperature furnace annealing (600–800°C) is described. It is found that the isolation function of oxide becomes unreliable and *s*-pit clusters from in the silicon substrate when the annealing temperature exceeds 700°C. Therefore, it is essential to limit the first annealing temperature of the selfaligned silicide scheme below 600°C.

Introduction: Metal silicides selectively formed on the source/drain regions have received much attention because they can alleviate many problems encountered in submicrometre CMOS process and because of their selfaligned nature. Among the silicides, $CoSi_2$ is one of the most promising candidates for salicide (selfaligned silicide) schemes due to its low resistivity and high temperature stability [1]. In addition, the absence of Co-As or Co-B pair formation [2], ease of selective etching and good chemical stability during processing offer further attractive reasons for the employment of cobalt silicide in CMOS technology. The thermal stability of cobalt on oxide during heat treatment is one of the decisive factors in determining the first annealing temperature of the salicide scheme. The interaction of Co with SiO_2 has been reported [3-5]. It was concluded that Co does not react with SiO_2 below 900°C in accordance with several material analysis techniques, such as AES and TEM. In this work, the interaction of Co and oxide at a lower temperature (≤ 800°C) was examined by the delineation of saucer pits (S pits). In addition, the electrical property of the field oxide was evaluated using current-voltage (I-V) characteristics.

Experiment: The starting material was (100)-oriented, phosphorus-doped *n*-type silicon wafers with 17–50 Ω-cm nominal resistivity. Immediately after RCA cleaning, a 5000 Å oxide layer was thermally grown by pyrogenic oxidation. After oxidation, four different processes were performed to prepare the samples. Sample set A was deposited with 500 of cobalt film in an *e*-beam evaporation system at a base pressure less than 5×10^{-6} torr and with a deposition rate of 1 Å/s. Without breaking the vacuum, a 50 Å of *α*-Si film was deposited on top of the Co film to serve as a passivation layer for the subsequent heat treatment. The preparation of the sample set B was the same as that of sample set A except that cobalt film of 40 Å thick with a deposition rate of 0·5 Å/s was deposited. For sample set C, only 50 Å of *α*-Si was deposited

on the oxide. Sample set D was used as a control and no deposition process was performed after oxidation. The four sample sets were then annealed in an N_2 ambient for 600, 700 and 800°C. The annealing time was 30 min.

To investigate the electrical and material properties of the systems, all sample sets were divided into two categories. One half of each sample was used to prepare MOS diodes for studying the electrical properties of the oxide. Unreacted Co and/or cobalt silicide were removed by wet etching and the MOS diodes were fabricated by the deposition of Al dots. The other halves of the samples were processed as follows. First, all the deposited films and the thermally grown field (500 Å) oxide on the silicon substrate were removed by various appropriate etching solutions. The samples were then sent through a 1025°C pyrogenic oxidation cycle for 2 h after standard RCA cleaning. It has been reported that S pits can be observed after oxidation if the silicon substrate is contaminated by cobalt metal [6]. The S pits can be observed after the oxide is stripped and the silicon substrate is given a delineation etch such as in Secco [7–8]. In this study, the samples were delineated by Secco etch for 5 min with ultrasonic agitation. The surface after Secco delineation was inspected by SEM.

Results: Fig. 1a and b present SEM micrographs of the silicon surface after Secco etching for sample set A with annealing at performed 700 and 800°C, respectively. Several etch pits with irregular shape are observed, and the 800°C annealed samples exhibit a higher density of etch pits than the 700°C annealed ones. One of the etch pits with 5000 times magnification is shown in Fig. 1c; the etch pit can be seen to be composed of several locally assembled S pits. In other words, the observed etch pits are S pit clusters near the silicon surface. For sample set B, which is deposited with 40 Å cobalt, similar results were observed. This implies that the formation of S-pit clusters is independent of the thickness of cobalt film. To confirm that the origin of S-pit clusters is due to the presence of cobalt film, sample sets C and D, which are absent of cobalt film, were processed with the same heat treatment along with sample sets A and B in an identical process run. No S-pit clusters were observed for the sample sets C and D in all cases. Therefore, we conclude that the presence of S-pit clusters after Secco etching is due to the presence of cobalt film on the oxide layer. Because no obvious interaction of Co and oxide was observed from AES analysis, the above phenomenon can be explained by local penetration of cobalt atoms through weak spots of the oxide after 700 and 800°C annealing. For the 600°C

annealing, no S-split cluster was found for all four sets of samples. The above results indicate that the temperature for the first annealing should be limited to 600°C.

The current-voltage (I-V) characteristics of the MOS diodes were measured on 30 test sites, with a diode area of $0.01\,cm^2$, for sample set A. The results are summarised in Table 1. It is obvious that higher temperature annealing leads to unreliable oxide isolation properties. The failure sites typically exhibit significant leakage current as shown in Fig. 2. This result indicates that the leakage paths in the oxide have been constructed by the penetration of cobalt atoms. The instability of the isolation function of oxide will cause the problem of lowering the device yield. Therefore, the first annealing temperature of the salicide scheme exceeding 700°C is an obstacle to maintaining the integrity of the isolation function of the field oxide.

A modified process was used to evaluate the influence of ion implantation. Following a 200 Å Co and a subsequent 50 Å α-Si deposition on the $SiO_2(5000\,Å)/Si$ substrate, As^+ ions were implanted into the α-Si/Co(SiO_2)/Si structure to a dose of $5 \times 10^{15}\,cm^{-2}$ at 80 keV. Ion implantation was employed to intermix cobalt and oxide at the interface. The implanted samples underwent the same process sequence as that of sample set A for MOS fabrication and S-pit cluster delineation. No evidence of oxide deterioration and S-pit cluster

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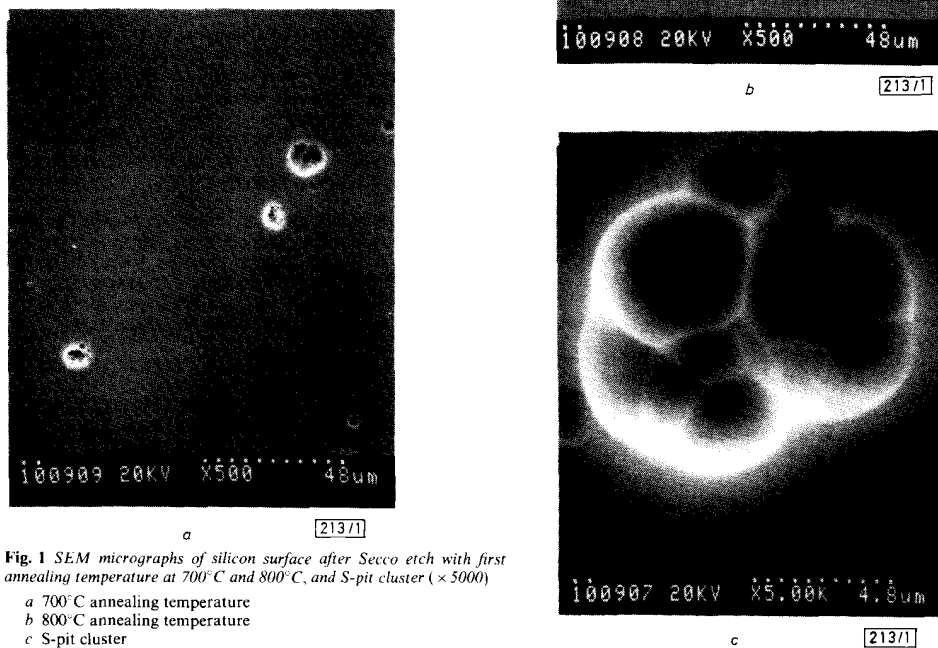
Fig. 1 *SEM micrographs of silicon surface after Secco etch with first annealing temperature at 700°C and 800°C, and S-pit cluster (× 5000)*

a 700°C annealing temperature
b 800°C annealing temperature
c S-pit cluster

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augmentation was observed. This indicates that ion implantation does not affect the quality of the field oxide.
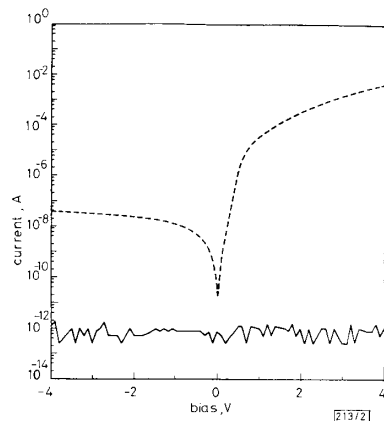

Fig. 2 *Typical I-V characteristics of leaky MOS diode as compared to those of nonleaky MOS device*

System noise is only present for nonleaky MOS device
- - - - leaky MOS diode
———— nonleaky MOS diode

In conclusion, it is found that direct silicidation above 700°C will degrade the performance of the field oxide and induce S-pit clusters in the silicon substrate. For samples annealed at 600°C, none of the above problems is observed. Thus, the first annealing of the salicide scheme below 600°C is a prerequisite for obtaining reliable processing of the α-Si/Co/SiO$_2$/Si structure during heat treatment.

Table 1 FREQUENCY OF FAILURE SITES AND S-PIT CLUSTERS OF SAMPLE SET A AFTER VARIOUS FIRST ANNEALING CONDITIONS

Sample set A	600°C	700°C	800°C
Percent of failure sites	0	0–3.3%	0–6.7%
S-pit clusters	no	yes	yes

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NONLINEAR CONTINUOUS-PHASE FREQUENCY SHIFT KEYING

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Indexing terms: Modulation, Frequency shift keying, Digital communication systems

Several nonlinear trellis modulation codes based on multilevel continuous-phase frequency-shift keying (*M*-CPFSK) are presented. On additive white Gaussian noise channels these digital FM schemes achieve higher minimum Euclidean distances and memory lengths than conventional CPFSK signals.

Introduction: Continuous-phase frequency-shift keying (CPFSK) has gained interest over other digital modulation schemes because of its phase continuity property [2, 3]. The inherent memory of CPFSK signals improves spectral performance and also enables maximum-likelihood sequence detection using the Viterbi algorithm [5]. The asymptotic error probability of CPFSK signals operating over the classical Gaussian channel at high signal to noise ratio is given by $P_e \simeq Q[\sqrt{(d_{min}^2/2N_0)}]$, where d_{min} is the normalised minimum Euclidean distance corresponding to all possible merging events of the finite-state trellis of the system. $N_0/2$ is the double-sided noise power spectral density and $Q(x) = [1/\sqrt{(2\pi)}] \int_x^\infty e^{-y^2/2} \, dy$. The performance of CPFSK signals can be improved by increasing the minimum Euclidean distance.

In the literature, techniques such as multi-h signalling [3], partial response signalling [1], and convolutional precoding [6] have been shown to increase the minimum Euclidean distance. Recently, a novel binary nonlinear multi-h CPFSK signalling technique [4] has been introduced where the state transition matrix is realised by adaptively changing the modulation index of the signals. Research reported in this Letter follows a similar strategy to increase the minimum Euclidean distance, but instead of binary multi-h signals, it uses single-h multilevel FSK signals. The numerical results obtained for nonlinear 4-CPFSK and nonlinear 8-CPFSK indicate that they achieve higher minimum Euclidean distances than the conventional *M*-CPFSK signals. Several schemes have been found to achieve the maximum memory length v_{max} allowed by the number of trellis phase states. For a system with N states, v_{max} is equal to $\lfloor 1 + \log_2 N \rfloor$[4], where $\lfloor ( ) \rfloor$ indicates the largest integer less than or equal to ( ).

Nonlinear continuous-phase FSK: Consider M-CPFSK with rational value modulation index $h = p/q$, where p and q are relatively prime positive integers. The state transition matrix T_q of such a system is a q by q matrix with elements a_n ($a_n \in \{\pm 1, \pm 3, \pm 5, \ldots, \pm(M-1)\}$) and 0s corresponding to the presence or absence of paths between the q phase states:

$$0, 2\pi h, 4\pi h, \ldots, 2(M-1)\pi h \qquad \text{(modulo-}2\pi\text{).}$$

For example, the finite-state system of $h = 1/4$, 4-CPFSK consists of the four phase states $0, \pi/2, \pi, 3\pi/2$ and has the state transition matrix

$$T_4 = \begin{bmatrix} -3 & 3 & 1 & -1 \\ -1 & -3 & 3 & 1 \\ 1 & -1 & -3 & 3 \\ 3 & 1 & -1 & -3 \end{bmatrix}.$$

The rows and columns of T_4 correspond to the phase angles in the reverse order. Therefore row one of T_4 corresponds to the