An Analytical Threshold-Voltage Model of Trench-Isolated MOS Devices with Nonuniformly Doped Substrates

Steve Shao-Shiun Chung, *Member, IEEE,* and Tung-Chi Li

Abstract—**A simple closed-form expression of the threshold voltage is developed for *Trench-Isolated MOS* (TIMOS) devices with feature size down to the deep-submicrometer range. The analytical expression is the first developed to include the non-uniform doping effect of a narrow-gate-width device. The *inverse narrow width effect* can be predicted *analytically* from the proposed model. It was derived by modeling the gate sidewall capacitance to include the two-dimensional field-induced edge fringing effect and solving the Poisson equation to include the channel implant effect at different operating backgate biases. A two-dimensional simulation program was also developed, and the simulated data were used for verification of the analytical model. Good agreements between the modeled and simulated data have been achieved for a wide range of gate widths and biases. The model is well suited for the design of the basic transistor cell in DRAM circuits using trench field oxide isolation structure.**

I. Introduction

The LOCOS field oxide isolation is a widely used isolation technology for the present VLSI process but not suitable for recent or future ULSI circuit with a minimum isolation width less than 1 μm for high-density DRAM applications. Therefore, we need a bird's-beak-free isolation structure to reduce the active area pitch. The trench-isolated (or fully recessed) field isolation structure (e.g., BOX[1], SWAMI[2]) which has a minimum isolation width down to the submicrometer range seems to be a very promising candidate for ULSI circuits. However, the small-geometry variation of the structure yields one peculiar second-order effect inherent in a Trench-Isolated MOS (TIMOS) device (see Fig. 1) known as the *Inverse Narrow-Width Effect* (INWE) [3]–[5], is quite different from the device with LOCOS structure [6]. In other words, as the channel width is reduced, this effect will cause a reduction of the threshold voltage [3], [4] and an increase of the subthreshold current [5] with reduced gate width. These abnormal characteristics are mainly due to the two-dimensional field-induced edge-fringing effect at the gate edge.

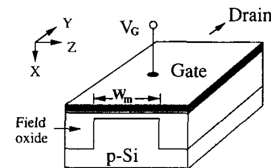

Fig. 1. A three-dimensional view of the TIMOS device used in this analysis.

The analytical expression of the threshold voltage for LOCOS device has been extensively studied [7]–[9]. In contrast, for TIMOS devices, only a limited amount of work has been reported [3], [4], [10], [11]. A first attempt to describe the inverse narrow-width effect was carried out by Akers [3]; he identified the sidewall capacitance to be the cause of such an effect and developed an analytical threshold voltage expression using a geometrical approximation and a conformal mapping method. However, the mapping method, by ignoring the bottom capacitance of the field oxide and the constant interface potential assumption, will affect the model accuracy. Later on, the model was refined by Hong and Cheng [10] who took into account the quadratic variation of the potential along the sidewall. They also demonstrated that the inverse narrow-width effect would revert to the conventional narrow-width effect for thick depletion layers (e.g., when a large backgate bias is applied). Hsueh and Akers [4] solved the two-dimensional (2D) Poisson equation and obtained a model based on the analytical expression of surface normal electrical field. However, this model did not match the simulation results very well when the gate width was decreased below 1 μm since it did not take into account the effect of backgate biases. Li *et al.* [11] also solved the Laplace equation in the field oxide using a conformal transformation method and deduced an analytical expression for the threshold voltage. However, all of the above models considered only the device with a uniformly doped substrate and could not be applied to practical devices with nonuniformly doped substrates. *No result of the threshold voltage in analytical form for devices with implanted channel has been reported so far* due to the difficulty of incorporating the channel implants into the solution.

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S. S. Chung is with the Department of Electronic Engineering and the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, ROC.

T. C. Li was with the Institute of Electronics, National Chiao Tung University. He is now with Seper Technology Inc., Taipei, Taiwan, ROC.

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In this paper, a closed-form expression of the threshold voltage for deep-submicrometer TIMOS device with a double-implanted channel will be developed. We use a complex mapping method to find the exact expression for the sidewall capacitance and a two-dimensional simulation program as an aid to predict the threshold voltage of the TIMOS device. A simple and more accurate model of the threshold voltage for uniformly doped devices is first developed. We also make a comparison with the models previously reported in [3], [10]. In order to apply this model to nonuniformly doped devices, we use the box approximation to depict the nonuniform impurity profile. A model for nonuniformly doped devices is thus derived. Section II describes the threshold voltage models for the the uniformly and nonuniformly doped devices. Results and comparisons with reported models and simulation results are given in Section III. Summary and conclusion are given in Section IV.

II. Formulation of the Model

A. Threshold Voltage Definition

In general, the conventional threshold voltage expression for a large-geometry MOSFET is based on the so-called *depletion approximation* [7] given by

$$V_T = V_{FB} + \phi_s + Q_B/C_G \tag{1}$$

where V_{FB} is the flat-band voltage, ϕ_s is the surface potential at strong inversion, C_G is the gate oxide capacitance per unit area, and Q_B is the depletion charge in the bulk region. Equation (1) is valid for a device with channel length longer than the source and drain depletion depths, and width wider than the depth of the gate-induced depletion region.

Q_B and C_G will become geometry-dependent as the size of the device is scaled down to the submicronmeter range [6], [9]. Fig. 2 shows three different types of device structures. Fig. 2(a) is for a large-geometry device; Fig. 2(b) is a MOS with LOCOS structure, and Fig. 2(c) is a TIMOS device. Since the threshold voltage is proportional to the drain current or the charge in the inversion layer Q_I ($= Q_n + Q_B$), we may use this as the definition of the threshold voltage that three devices have the same Q_I at the threshold point. For the case of Fig. 2(b), the depleted side charge ΔQ_B under the bird's beak of a LOCOS gate [2] results in an increase of the threshold voltage with the reduction of the gate width. In other words, the threshold voltage increases with a reduction in channel width due to this additional side charge ΔQ_B induced by the narrow-width effect. In contrast, for TIMOS devices operating at the threshold point, the depletion charge Q_B of Fig. 2(a) and (c) can be regarded as about the same while the inversion-layer charge (Q_n) of the two devices are assumed equal. As a consequence, the approach taken is to solve a one-dimensional Poisson equation to obtain the depletion charge Q_B in the bulk region that includes either uniform or nonuniform doping. This is the basic idea for deriving an analytical threshold voltage model in the paper.

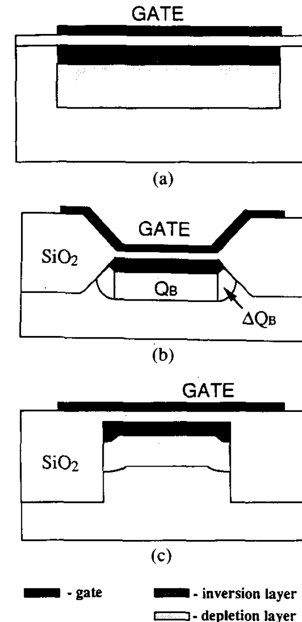

Fig. 2. Three types of device structures and the associated inversion and depletion layers. (a) Large-geometry MOSFET. (b) LOCOS gate MOSFET. (c) Trench-isolated MOSFET.

In order to make experimental–theoretical or simulation–theoretical comparison, the threshold voltage can be extracted from the measured or simulated I_D–V_{GS} curve as described in [9].

B. The Model for Uniformly Doped Substrate

The inverse-narrow-width effect of a TIMOS device is due to the two-dimensional field-induced edge fringing effect. This edge effect contributes to the sidewall capacitance which is comparable to the gate oxide capacitance term, e.g., C_G, in (1) for very-narrow-gate-width devices. Fig. 3 illustrates the simulated surface potential of a TIMOS from the middle of the gate to the end of the sidewall. Note that the enhanced potential at the edge of the gate is due to the fringing effect near the corner (point B in the insert of Fig. 3). The gate capacitance used in (1) is normally considered ideal and its value is calculated using the parallel-plate approximation. In a TIMOS device, the capacitance C_G should include not only the gate oxide capacitance but also the sidewall capacitance. Here, the total gate capacitance of a TIMOS device is modeled as the gate capacitance in parallel with two sidewall capacitances given by

$$C_T = C_{ox}W + 2C_F \tag{2}$$

where C_{ox} is the thin gate oxide capacitance per unit area, W is the device width, and C_F is the sidewall capacitance per unit length due to the edge fringing effect.

Consider the case of a long-channel but narrow-width TIMOS device. In the insert of Fig. 3 which shows one side of the channel, the gate electrode overlaps the re-

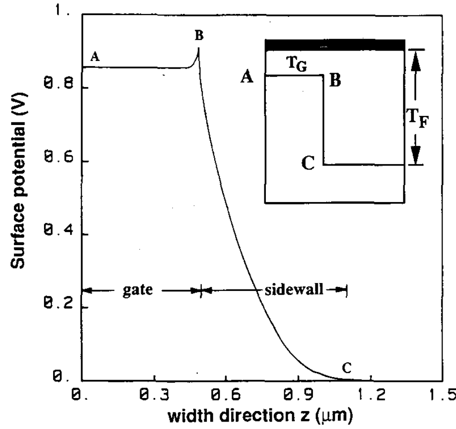

Fig. 3. Surface potential of a TIMOS device from the middle of the gate to the sidewall.

cessed oxide. The thickness of the thin oxide is T_G, and the thickness of the field oxide is T_F. First, the interface charge along both the thin and the field oxide–silicon boundary is considered uniform and constant. The conformal mapping method is used to calculate the sidewall capacitance. Fig. 4 illustrates the mapping method. The transform equation given by

$$u + iv = \cos\,[\pi(ix - y)/T_F] \quad (3)$$

is used to define the mapping between Fig. 4(a) and (b), in which u, v and x, y define the complex planes. To compute the capacitance between $\overline{CB}$ and $\overline{DE}$ segments, we may move the origin to the center of the $\overline{CD}$ segment as redrawn in Fig. 4(c), then the sidewall capacitance is obtained by integrating a half circle with radius r from point C to point B as

$$\begin{aligned} C_F &= \int_C^B \epsilon_{ox} \frac{dr}{r} \\ &= \frac{\epsilon_{ox}}{\pi} \ln \frac{2 - d_0}{d_0} \\ &= \frac{\epsilon_{ox}}{\pi} \ln \left(\frac{3 - \cos\,(\pi(T_F - T_G)/T_F)}{1 + \cos\,(\pi(T_F - T_G)/T_F)} \right) \end{aligned} \quad (4)$$

where ϵ_{ox} is the permittivity of the SiO_2 and $d_0 = \{1 + \cos\,[\pi(T_F - T_G)/T_G]\}/2$.

In order to verify the validity of this equation, we developed a two-dimensional simulator to numerically calculate the above sidewall capacitance as well as the device drain current for further extraction of the threshold voltages. First, we use the 2D simulator to calculate the capacitance of the sidewall. Assume the gate and the silicon-oxide interface ($\overline{cba}$ in Fig. 4) to be a metal plate, then the potential distribution in the metal–oxide–metal structure is simulated. The surface charge induced on the sidewall is defined as the sum of electrical field normal to the sidewall times the dielectric constant of oxide, i.e.,

$$Q_s = \epsilon_{ox} \int E_\perp\, dx = \epsilon_{ox} \sum_n E_\perp(n)\, \Delta x(n) \quad (5)$$

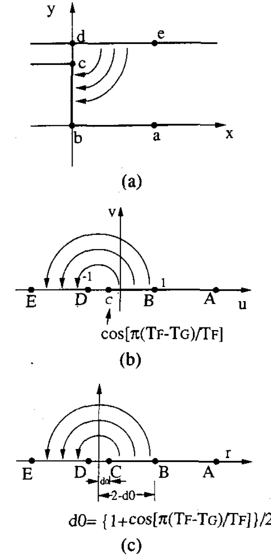

Fig. 4. The mapping method for calculating the sidewall capacitance. (a) The real edge structure. (b) Transformation of (a) into u-v plane. (c) Move the origin of (b) to the center of CD segment.

where $E_\perp(n)$ is the electrical field normal to the sidewall at the discretized grid. The capacitance of the sidewall is obtained by computing values of Q_s at two different gate voltages and then calculating

$$C = \frac{\Delta Q_s}{\Delta V_G}. \quad (6)$$

The comparison of the sidewall capacitance between the theoretical result (4) and the simulated result are shown in Fig. 5. The solid lines are the theoretically computed results at different gate thickness (from top to bottom, T_G = 100, 200, 300, and 400 Å), the cross marks are the simulation results based on a metal–oxide–metal structure. It is obviously seen that good agreement between equation and simulated results is achieved. However, in a real MOS structure the potentials at the sidewall are not uniform and the electrical field is not really normal to the sidewall, as shown in Fig. 3. The above derivation of (4) is based on the assumption that the potential in the inversion layer along the sidewall is constant. However, for a real MOS device simulation including the bulk region, the surface potential will cause the depletion-layer boundary to penetrate further into the silicon bulk and hance will result in a wider depletion. This will give rise to a smaller value of capacitance as compared with that computed from a metal-oxide-metal structure. This will cause the fringing capacitance C_F to be *overestimated* for a metal–oxide–metal structure. Therefore, it is necessary to add a correction factor (which is empirical and with value less than one) to get a closer approximation of the sidewall capacitance in a real device. This results in the following:

$$C_F = \delta \frac{\epsilon_{ox}}{\pi} \ln \left(\frac{3 - \cos\,(\pi(T_F - T_G)/T_F)}{1 + \cos\,(\pi(T_F - T_G)/T_F)} \right). \quad (7)$$

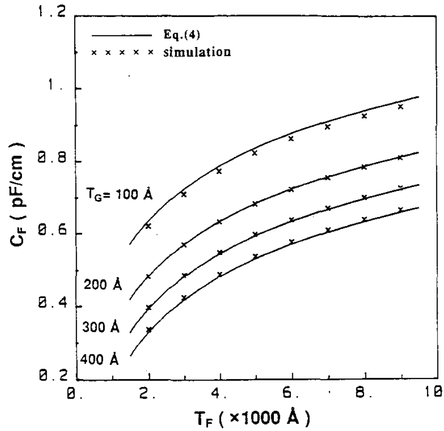

Fig. 5. Comparison of the sidewall capacitances between theoretical and simulated results for a metal-oxide-metal structure.

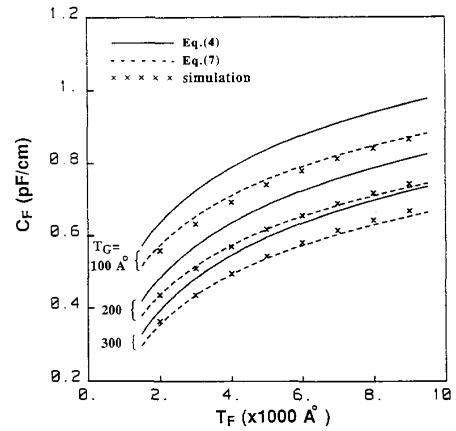

Fig. 6. Comparison of the sidewall capacitance between theoretical and simulated results of a real TIMOS structure. $N_A = 2 \times 10^{16}$ cm^{-3}. $\delta = 0.95$ in (8) is used to match it with simulated data denoted by cross marks.

The correction factor can be accurately determined from the 2D simulation of a real TIMOS structure. The sidewall capacitance obtained from simulation is illustrated in Fig. 6. The cross marks represent the simulated capacitance of the device and the solid lines are the solution of (4) for a wide range of gate-oxide thickness. By comparison, the difference between simulated and theoretical computed (4) values is due to the nonlinear effect of the surface potential at the SiO_2–Si interface. This factor is obtained by measuring the difference between solid lines and simulated data over a wide range of gate oxide and field oxide thicknesses. In this example, the solid lines data (computed from (4)) are multiplied by $\delta = 0.95$ which yields the dashed lines (7). These dashed lines are in good agreement with simulated data. The final expression of the threshold voltage in a TIMOS device is given by

$$V_T = V_{FB} + \phi_s + Q_B W / C_T \tag{8}$$

by using (7) in (2), and replacing the C_G with C_T in (1). Here, the depletion charge Q_B per unit gate width is

$$Q_B = \sqrt{2q\epsilon_{si}N_A(\Phi_s - V_{BS})} \tag{9}$$

for a uniform substrate doping N_A.

C. The Model for Nonuniformly Doped Substrate

In practical CMOS VLSI technology, it is always required to apply ion implants in the device channel to adjust the threshold and to prevent the punchthrough phenomena. The reported models that were previously mentioned [4], [10], [11] are too complicated and cannot be applied to a nonuniformly doped substrate. The model derived above, (8), has also been extended to a device with double-implanted channel. We adopt the Gaussian distribution to describe the implantation profile given by

$$n(x) = N_0 \exp\left(-\frac{x - R_p}{\sqrt{2}\sigma_p}\right)^2 \tag{10}$$

where N_0 is the peak concentration, R_p is the projected range, σ_p is the standard deviation. The parameters N_0, R_p, and σ_p are derived from empirical expression in [12]. We also simulate the 2D diffusion to account for the annealing process. Then the threshold voltages were extracted from the simulated I_D–V_{GS} characteristics as described in Section II-A.

In order to apply (8) to a nonuniformly doped substrate, we need to know the channel depletion-layer charge Q_B for estimating the threshold voltage. An analytical model for the depletion-layer charge can be easily obtained using the corrective box representation [13], [14] for the channel doping profile as shown in Fig. 7(a). Here, the depths d_1 and d_2 and the average doping N_{E1} and N_{E2} of the corrective equivalent boxes can be expressed in terms of process parameters R_p and σ_p and the implant dose Q_T per unit area given by

$$d = 1.57\ \sigma_p \exp\ (0.45\ R_p/\sigma_p) \tag{11}$$

and

$$N_E = Q_T/q/d \tag{12}$$

respectively. The box approximation was derived [13] by matching the charge-voltage relationships of the actual profile with the box profile. For a given depletion-layer charge Q_B, the voltage drop V_d across the depletion layer in the box-type approximation is given by

$$V_d = \frac{Q_B^2}{2q\epsilon_s N_E}. \tag{13}$$

The channel can be divided into three layers under different operating biases, as shown in Fig. 7(b). The solution of the depletion-layer width (X_D) and the depletion-layer charge (Q_B) can be obtained by solving the one-dimensional Poisson equation at different back-gate biases. In Fig. 7, $N_{T1} = N_{E1} + N_{E2} + N_A$, $N_{T2} = N_{E2} + N_A$, $d_{T1} = d_1$, and $d_{T2} = d_2 - d_1$. The values of these parameters are listed in Table I. The calculation of the depletion width can be divided into three cases as follows.

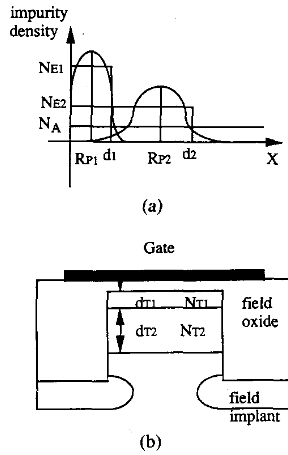

Fig. 7. (a) The box approximation for a double-implanted channel. (b) The approximate channel doping profile of a TIMOS device, in which $N_{T1} = N_{E1} + N_{E2} + N_A$ and $N_{T2} = N_{E2} + N_A$.

TABLE I
PARAMETERS OF THE DOUBLE-CHANNEL IMPLANTS

	Implant 1	Implant 2
Element	BF_2	B
Dose (cm^{-3})	9×10^{11}	9×10^{11}
Energy (keV)	60	150
R_p (Å)	289	2386
σ_p (Å)	224	832
N_E(cm^{-3})	1.43×10^{17}	1.90×10^{16}
d (Å)	630	4346
V_{ZB}(V)	−0.35	−2.87

Case 1 ($X_D \leq d_{T1}$): When the surface-to-bulk potential ($\phi_s - V_{BS}$) is sufficiently small so that the width of the depletion region X_D is less than the implant layer depth d_{T1}, the equation for the depletion width is similar to that from the depletion approximation given by

$$X_D = \sqrt{\frac{2\epsilon_s(\phi_s - V_{BS})}{qN_{T1}}} \tag{14}$$

in which the equivalent implanted layer concentration N_{T1} is used. Here, the surface inversion potential at the threshold point is approximated by

$$\phi_s = 2\frac{q}{kT}\ln(N_{T1}/n_i). \tag{15}$$

The depletion-layer charge is then found from the depletion width X_D, i.e.,

$$Q_B = qN_{T1}X_D. \tag{16}$$

Assuming that the depletion width X_D is equal to d_{T1}, we can find the boundary of channel to the back-gate bias potential V_{ZB1} by solving (14) which gives

$$V_{ZB1} = \phi_s - \frac{qN_{T1}\,d_{T1}^2}{2\epsilon_s}. \tag{17}$$

If V_{BS} is smaller than V_{ZB1}, then the depletion width would be larger than d_{T1}, and located in the second region as follows.

Case 2 ($d_{T1} < X_D \leq d_{T1} + d_{T2}$): When the back-gate bias V_{BS} is smaller than V_{ZB1}, the maximum depletion region width exceeds the first implant layer depth d_{T1}. We must take into account the effect of the two layers with different impurity concentrations N_{T1} and N_{T2}. By solving the 1D Poisson equation as described in detail in the Appendix, we have the expression of the depletion width

$$X_D = \sqrt{\frac{2\epsilon_s(\phi_s - V_{BS})}{qN_{T2}} + \left(1 - \frac{N_{T1}}{N_{T2}}\right) d_{T1}^2}. \tag{18}$$

Also, the depletion charge Q_B is

$$Q_B = q(N_{T1}\,d_{T1} + N_{T2}(X_D - d_{T1})). \tag{19}$$

Assuming that the depletion width X_D is equal to $d_{T1} + d_{T2}$, we can find the boundary of back-gate bias V_{ZB2} by solving (19)

$$V_{ZB2} = \phi_s - \frac{q(N_{T1}\,d_{T1}^2 + N_{T2}(d_{T1}\,d_{T2} + d_{T2}^2))}{2\epsilon_s}. \tag{20}$$

If V_{BS} is lower than V_{ZB2}, then the depletion region will extend into the third layer as follows.

Case 3 ($d_{T1} + d_{T2} < X_D$): When V_{BS} is smaller than V_{ZB2}, the depletion width will exceed the bottm of the second implant layer and extend into the region of substrate doping. Following the derivation in the Appendix, we have the expression of depletion width given by

$$X_D = \sqrt{\frac{2\epsilon_s(\phi_s - V_{BS})}{qN_A} + (d_{T1} + d_{T2})^2 - (N_{T1}\,d_{T1}^2 + 2N_{T2}\,d_{T1}\,d_{T2} + N_{T2}\,d_{T2}^2)/N_A}. \tag{21}$$

Also, the depletion charge is

$$Q_B = q(N_{T1}\,d_{T1} + N_{T2}\,d_{T2} + N_A(X_D - d_{T1} - d_{T2})). \tag{22}$$

The analytical procedure to find the threshold voltage of nonuniformly doped device is explained as follows: 1) First, apply the parameters of implant process, N_0, R_p, and σ_p, to (11), (12) and find the equivalent box representation parameters, depth d and the average doping N_E of the three layers. 2) Calculate the boundary of the back-gate bias, V_{ZB1} and V_{ZB2}, and compare it with the applied V_{BS} to find in which layer is the bottom of the depletion region located. Then, according to the expressions for X_D and Q_B in the three cases, we can calculate the values of X_D and Q_B. The sidewall capacitance C_F is calculated by (7). 3) The threshold voltage can be computed according to (8) and the values of X_D, Q_B, and C_F can be calculated.

III. Simulation Results and Comparison with Reported Models

This section deals with comparisons of simulated and modeled results as well as the comparison between the new and reported models [3], [10]. Since there are no threshold voltage models reported so far for nonuniformly doped substrate devices, the comparison between our new model and those of reported modeled results are for uniformly doped substrate devices only.

Comparison of the modeled and simulated results of uniformly doped TIMOS devices is given in Fig. 8. The cross marks represent the simulation data and the solid lines are the modeled results with different back-gate biases. There is good agreement between modeled and simulated data. We also made a comparison of the results between our model and other reported models, as shown in Fig. 9. It is believed that the new model is more accurate and reliable than reported models by looking at the consistency of our modeled and simulated results. Ackers' model will become less accurate for narrower gate widths since in his transformation method from Fig. 4(a) and (b), the bottom segment $\overline{ab}$ is neglected. This will induce large error of the threshold voltage due to the accuracy of the sidewall capacitance particularly when the gate width is rather small. For example, in Fig. 9, large error can be perceived at 0.25-μm gate width by comparing Ackers' and simulation results.

One important result from our model equation, (8), is a manifestation of the inverse narrow-width effect. Since the contribution of the sidewall capacitance ($2C_F$) is significant by comparison with the gate-oxide capacitance ($C_{ox}W$) as in (2) for narrow gate-width devices, from (8), it is obvious that a narrower gate-width device has a smaller value of threshold voltage in comparison to a large gate-width device. In other words, the threshold voltage decreases with decreasing gate width.

Fig. 10 gives the comparison of the new model and the simulation results for nonuniformly doped substrate devices. A p-type concentration of 9×10^{14} cm^{-3} substrate is used. The implantation data are listed in Table I. The field implant is a boron source with dose and implant energy of 2×10^{13} cm^{-3} and 25 keV, respectively. The thicknesses of gate and field oxides are 200 and 6000 Å, respectively. The lines represent the new model results at different V_{BS}, and the cross marks represent the simulated data. A little mismatch of the data at $V_{BS} = -5$ V is due to the lateral encroachment of the impurity from the field implant region. As the width is reduced, the field implant under both sides of the field oxide will pinch off the channel and form an extra impurity layer under the channel. At large back-gate biases, the depletion region will extend into this extra layer and cause the mismatch between modeled and simulated results. As we noticed in (7), $\delta = 0.75$ is used in Fig. 10 to get a best fit of the modeled and simulated data for the following reasons. The nonuniformity of the channel implant will affect the value of δ. In comparison with devices without channel implant, as

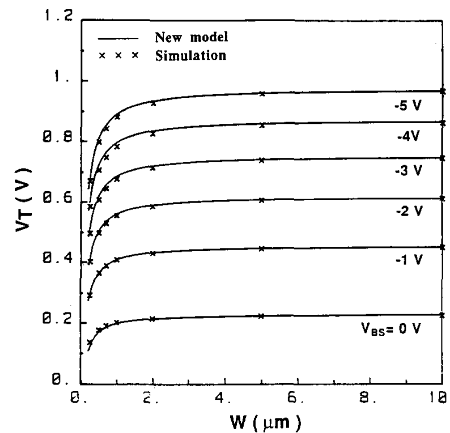

Fig. 8. Comparison of the modeled and simulated results of the threshold voltage for uniform substrate doping, T_G = 200 Å, T_F = 6000 Å, and $N_A = 2.0 \times 10^{16}$ cm^{-3}.

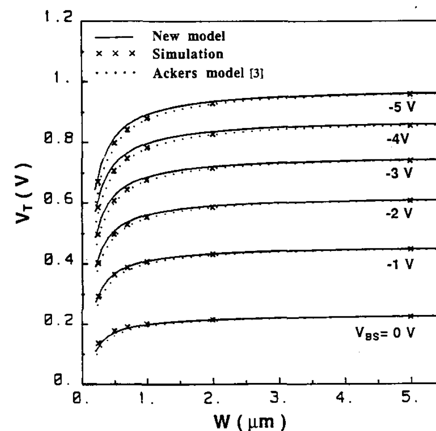

Fig. 9. Comparison of new model with Ackers' [3] model.

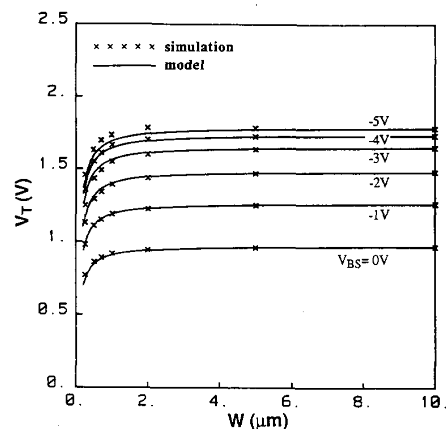

Fig. 10. Comparison of the modeled and simulated results of the threshold voltage for the device with nonuniformly doped substrate. $N_A = 9 \times 10^{14}$ cm^{-3} and channel implants are given in Table I.

in the case of Fig. 8, devices with channel implants will have a higher value of surface potential (along both the interface beneath the thin gate oxide and the sidewall) than devices without channel implants. This will give lower value of the induced fringing electric field between the gate and the sidewall since this electric field is proportional to the voltage defference between the gate and the sidewall. Thus according to (5), the induced surface charge Q_s and the resultant capacitance calculated by (6) will be smaller than that computed for devices without channel implants. This results in a smaller sidewall capacitance that we simulated for channel-implanted devices. Therefore, it is reasonable to use smaller value of δ to have a fit of the modeled threshold voltage with simulated results in Fig. 10.

IV. Summary and Conclusion

In summary, we propose for the first time an analytical model of the threshold voltage for trench-isolated MOS devices with feature size down to the deep-submicrometer range. Particularly, the proposed model is suitable for devices with either uniformly or nonuniformly doped substrate. The *inverse narrow-width effect* which causes the decrease of the threshold voltage with a reduction of the gate width has been analytically modeled.

The analytical threshold voltage model we developed is based on an accurate representation of the 2D field-induced sidewall capacitance and an explicit solution of the depletion-layer charge in the bulk. A conformal mapping method is employed to find the above sidewall capacitance which is further calibrated by the simulation results. A simple and accurate threshold voltage model for TIMOS devices with uniformly doped substrates is first obtained. In order to apply this model to nonuniformly doped devices, we use the box approximation to describe the nonuniform impurity profile and solve the 1D Poisson equation in the bulk region to obtain an analytical solution of the depletion-layer width and charge. A model for nonuniformly doped substrate is thus established. A two-dimensional simulation program was also developed, and the simulated data were used for verification of the analytical model. Good agreements between the modeled and simulated data have been achieved even when the gate width is reduced to 0.2 μm. Comparing to other reported models, our model is better in terms of accuracy and applicability. The most important feature of this threshold voltage model is its application to the design of a high-density DRAM transistor cell using trench field oxide isolation.

Appendix
The Derivation of the Depletion Layer Width and Charge

In Fig. 8, the double-implanted channel is divided into three regions with different impurity concentrations. If the bottom of the depletion width is located in the first region, then the expression for depletion width is the same as in

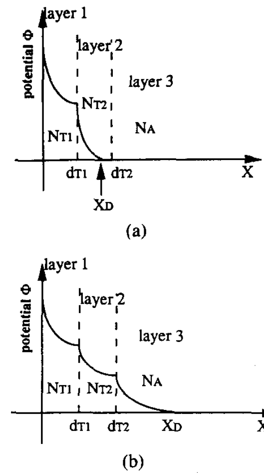

Fig. 11. The potential distribution in the depth direction when the depletion-layer width resides in (a) the second (deep-implant) layer, (b) the third (substrate) layer.

(14). If the depletion region is extended into the second (deep-implant) layer or the third (substrate doping) layer, one needs to solve the 1D Poisson equation and consider the continuity of electrical potential and field intensity at the interface between different layers. The derivation of the depletion width will be given as follows.

1) ($d_{T1} \leq X_D \leq d_{T1} + d_{T2}$): The bottom of depletion width is located in the second implanted layer, as shown in Fig. 11(a). The expressions of the electrical field and potential in the second and first implanted layers are given by

$$\frac{d\phi}{dx} = -\frac{qN_{T1}}{\epsilon_s}(x - X_D) \tag{A1a}$$

$$\phi = \frac{qN_{T2}}{2\epsilon_s}(x - X_D)^2 \tag{A1b}$$

and

$$\frac{d\phi}{dx} = -\frac{qN_{T1}}{\epsilon_s}(x - d_{T1}) + C_1 \tag{A2a}$$

$$\phi = \frac{qN_{T1}}{2\epsilon_s}(x - d_{T1})^2 - C_1(x - d_{T1}) + C_2 \tag{A2b}$$

respectively.

Considering the continuity at the interface $x = d_{T1}$, we have the expressions for C_1 and C_2 by equating (A1a) with (A2a) and (A1b) with (A2b), i.e.,

$$C_1 = \frac{qN_{T1}}{2\epsilon_s}(d_{T1} - X_D)^2 \tag{A3a}$$

and

$$C_2 = \frac{qN_{T2}}{2\epsilon_s}(d_{T2} - X_D)^2. \tag{A3b}$$

In order to solve the depletion width X_D, let $x = 0$ and $\phi = \phi_s - V_{BS}$. Equation (A2b) can be reduced to

$$\phi_s - V_{BS} = \frac{qN_{T1}}{2\epsilon_s} d_{T1}^2 - \frac{qN_{T2}}{\epsilon_s} d_{T1}(d_{T1} - X_D) + \frac{qN_{T2}}{2\epsilon_s}(d_{T1} - X_D)^2 \quad \text{(A4)}$$

which has the solution of X_D given by

$$X_D = \sqrt{\frac{2\epsilon_s}{qN_{T2}}(\phi_s - V_{BS}) + \left(1 - \frac{N_{T1}}{N_{T2}}\right) d_{T1}^2}. \quad \text{(A5)}$$

Hence, the depletion charge is obtained by

$$Q_B = \int_0^{XD} N(x)\, dx = q[N_{T1}D_{T1} + N_{T2}(X_D - D_{T1})]. \quad \text{(A6)}$$

2) $(d_{T1} + d_{T2} < X_D)$: The depletion width extends into the third layer of substrate doping, as shown in Fig. 11(b). The expressions of the electrical field and potential in three different layers are given as follows:

third layer

$$\frac{d\phi}{dx} = -\frac{qN_A}{\epsilon_s}(x - X_D) \quad \text{(A7a)}$$

$$\phi = \frac{qN_A}{2\epsilon_s}(x - X_D)^2 \quad \text{(A7b)}$$

second layer

$$\frac{d\phi}{dx} = -\frac{qN_{T2}}{\epsilon_s}[x - (d_{T1} + d_{T2})] + C_1 \quad \text{(A8a)}$$

$$\phi = \frac{qN_{T2}}{2\epsilon_s}[x - (d_{T1} + d_{T2})]^2 - C_1[x - (d_{T1} + d_{T2})] + C_2 \quad \text{(A8b)}$$

first layer

$$\frac{d\phi}{dx} = -\frac{qN_{T1}}{\epsilon_s}[x - d_{T1}] + C_3 \quad \text{(A9a)}$$

$$\phi = \frac{qN_{T1}}{2\epsilon_s}[x - d_{T1}]^2 - C_3 \cdot [x - d_{T1}] + C_4. \quad \text{(A9b)}$$

Taking into account the continuities of the electrical field and potential at the two interfaces between the three layers, we can solve the coefficients from the above equations, i.e.,

$$C_1 = -\frac{qN_A}{\epsilon_s}[(d_{T1} + d_{T2}) - X_D] \quad \text{(A10a)}$$

$$C_2 = \frac{qN_A}{2\epsilon_s}[(d_{T1} + d_{T2}) - X_D]^2 \quad \text{(A10b)}$$

$$C_3 = \frac{qN_{T2}}{\epsilon_s} d_{T2} - \frac{qN_A}{\epsilon_s}[(d_{T1} + d_{T2}) - X_D] \quad \text{(A10c)}$$

$$C_4 = \frac{qN_{T2}}{2\epsilon_s} d_{T2}^2 - \frac{qN_A}{\epsilon_s} d_{T2}[(d_{T1} + d_{T2}) - X_D] + \frac{qN_A}{2\epsilon_s}[(d_{T1} + d_{T2}) - X_D]^2. \quad \text{(A10d)}$$

To find the depletion layer width X_D, let $x = 0$ and $\phi = \phi_s - V_{BS}$. Equation (A9b) can be reduced to

$$\phi_s - V_{BS} = \frac{qN_{T1}}{2\epsilon_s} d_{T1}^2 + \frac{qN_{T2}}{2\epsilon_s} d_{T2}^2 + \frac{qN_{T2}}{\epsilon_s} d_{T1} d_{T2} - \frac{qN_A}{2\epsilon_s}[(d_{T1} + d_{T2})^2 - X_D^2] \quad \text{(A11)}$$

from which X_D can be determined and given by

$$X_D = \sqrt{\frac{2\epsilon_s}{qN_A}(\phi_s - V_{BS}) + (d_{T1}^2 + d_{T2}^2) - (N_{T1} d_{T1}^2 + 2N_{T1} d_{T1} d_{T2} + N_{T2} d_{T2}^2)/N_A}. \quad \text{(A12)}$$

Also, the depletion charge Q_B is given by

$$Q_B = q[N_{T1} D_{T1} + N_{T2} D_{T2} + N_A(X_D - D_{T1} - D_{T2})]. \quad \text{(A13)}$$

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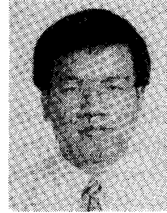
Steve Shao-Shiun Chung (S'83-M'85) received the B.S. degree from the National Cheng-Kung University, Taiwan, in 1973, the M.Sc. degree from the National Taiwan University, Taiwan, in 1975, and the Ph.D. degree from the University of Illinois at Urbana-Champaign, in 1985, all in electrical engineering.

From 1976 to 1978, he worked for an electronic instrument company as Head of the R&D division and subsequently as Manager of the Engineering Division. From 1978 to 1983, he was with the Department of Electronic Engineering and Technology at the National Taiwan Institute of Technology (NTIT) as a Lecturer. He was also in charge of an Instrument Calibration Center at NTIT. From 1983 to 1985, he held a research assistantship in the Solid State Electronics Laboratory and the Department of Electrical and Computer Engineering at the University of Illinois. In 1985, he served as NTIT again as an Associate Professor in the Department of Electronic Engineering. Since August 1987, he has been with the Department of Electronic Engineering and Institute of Electronics, National Chiao Tung University, and has been a Full Professor since the Fall of 1989. His current teaching and research interests are in the areas of solid-state device physics and VLSI technology; semiconductor device modeling and simulation; characterization and reliability study of VLSI devices and circuits, and computational algorithms for VLSI circuits.

Dr. Chung has served as a Technical Program Committee Member of the ASIC Conference, IEEE, since 1989.



Tung-Chi Li was born in Changhua, Taiwan, Republic of China, on October, 1964. He received the B.S. degree from the Department of Electrical Engineering, National Taiwan University, in 1986, and the M.Sc. degree from the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, in 1990. His master thesis was on the two-dimensional simulation and modeling of a quarter-micron trench-isolated MOS transistor.

Since August 1990, he has been with the Seper Technology Corporation in Taipei as an application engineer.