the pinch-off mode of operation, and found to be 2.11 and 4.06GHz, respectively. Under optical illumination f_T was increased by 20%, while f_{max} was improved by 10% compared with microwave performance under non-illumination.

In summary, a *p*-channel $In_{0.49}Ga_{0.51}P/GaAs/In_{0.13}Ga_{0.87}As$ pseudomorphic MODFET with 1μm gate length has been fabricated. DC and microwave performance of the devices were characterised with and without optical illumunation. We observed that the photocurrent was –0.36mA at V_{gs} = –0.2V and V_{ds} = –3.5V with incident optical power of 2.15mW. A significantly high responsivity was noted at low incident optical powers. Under the optical illumination, current gain cut-off frequency and maximum available gain cut-off frequency were improved. These results of the optical responses of the *p*-channel InGaP/GaAs/InGaAs pseudomorphic MODFET on a GaAs substrate are reported for the first time.

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Suppression of boron penetration in p^+ polysilicon gate using Si-B diffusion source

T.S. Chao, C.P. Kuo, T.F. Lei, T.P. Chen, T.Y. Huang and C.Y. Chang

The authors report a novel Si-B diffusion source for doping p^+-poly-Si gates in *p*MOSFETs. It is found that B penetration can be effectively suppressed by using this novel process. All of the electrical properties of the MOS capacitors are significantly improved over those in the conventional BF_2^+ or B^+-implanted samples. This new process is very promising for future surface-channel *p*MOSFETs.

Introduction: p^+-polycrystalline silicon (p^+-poly-Si) has been proposed as the gate material for surface-channel *p*-type metal-oxide-semiconductor transistor (*p*MOSFETs) in deep submicron complementary metal-oxide semiconductor devices [1]. This is because surface-channel *p*MOSFETs using p^+-poly-Si gates have better short-channel and sub-threshold I-V characteristics. They also exhibit improved controllability of the threshold voltage over buried-channel *p*MOSFETs with an n^+-poly-Si gate. However, the fast boron diffusion in the poly-Si and gate oxide, results in the susceptibility of boron penetration through the gate into the underlying silicon substrate. The presence of F, due to BF_2^+ implantation, further enhances the diffusion of B [2]. Boron penetration is known to cause device instability such as positive threshold voltage shift, increased subthreshold swing, increased electron trapping rate, low-field hole mobility degradation, and drive current degradation due to poly-Si depletion in *p*MOSFETs. Many methods have been proposed to suppress boron penetration. The first approach is to retard the boron diffusion in the poly-Si. This can be achieved by stacked or modified poly-Si gate structures [3]. The second approach is to establish a diffusion barrier at the interface of the poly-Si/oxide and/or oxide/Si-substrate. This can be achieved by nitridation of the gate and/or gate oxide by using N_2O or NO oxidation/annealing, or an inductive-coupling-nitrogen-plasma to incorporate a nitrogen-rich layer at the SiO_2/Si interface as a barrier to retard the boron diffusion [4] In this Letter, a novel Si-B layer is proposed, for the first time, as the diffusion source for doping the p^+-poly-Si. The comprehensive effects of annealing temperature and time on the p^+-poly-Si MOS capacitors using an Si-B layer are compared with the conventional BF_2^+- and B^+ ion-implanted counterparts by using secondary ion mass spectroscopy (SIMS) analyses, high/low frequency C-V measurements, J-E characteristics, and charge-to-breakdown (Q_{bd}) values. It is found that this new process, which is inherently free of F, has a better capability for suppressing boron penetration than conventional methods employing either BF_2^+ or B^+ implantation.

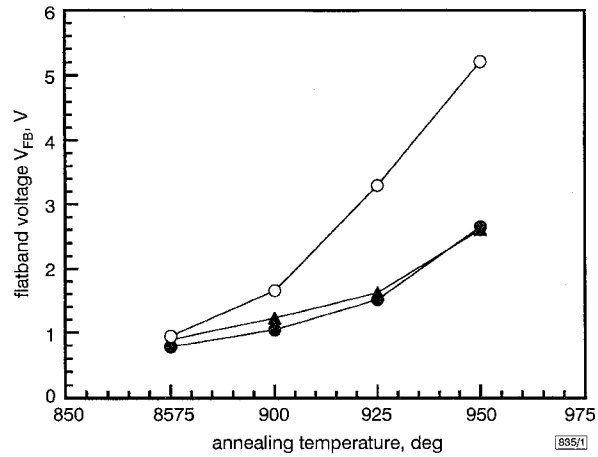

Fig. 1 *Flat-band voltage of BF_2^+-implanted, B^+-implanted and Si-B samples annealed at 875–950 °C for 15 min*

● Si-B
▲ B^+
○ BF_2^+

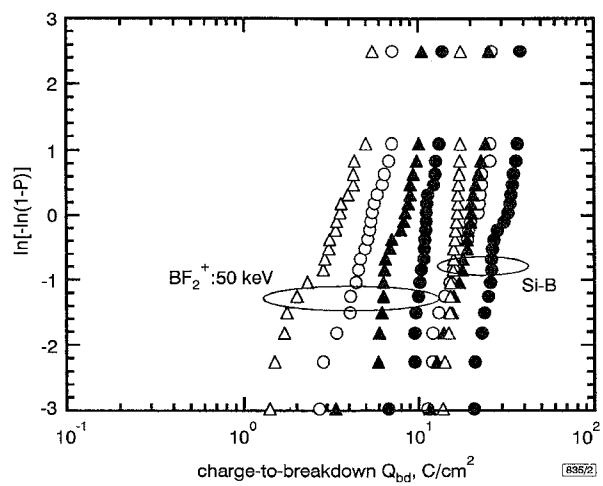

Fig. 2 *Distribution of charge-to-breakdown of BF_2^+-implanted and Si-B samples*

● 875 °C
○ 900 °C
▲ 925 °C
△ 950 °C

Experiment: p^+-poly-Si gate MOS capacitors were fabricated on *n*-type (100) Si-wafer with from 2 to 4Ω cm resistivity. The active area was defined with 550nm of field oxide. A thin 9.5nm gate oxide was grown at 900°C. A 300nm poly-Si was then deposited. Samples with the conventional implanted p^+-poly-Si gate were fabricated by using BF_2^+, 50keV, or B^+, 20keV, both to a dose of 5×10^{15}cm^{-2}; while for the Si-B samples, they were put instead into a ultra-high-vacuum vapour chemical deposition (UHV/CVD) system to deposit a 35nm Si-B layer upon the undoped poly-Si gate layer by using a 1:1 mixture of pure SiH_4 and B_2H_6 (1% in H_2) at 550°C. The base pressure was 2×10^{-8} torr. Afterwards, all samples were annealed in wet O_2, ambient at temperatures between 875 and 950°C for 15–35min. The Si-B layer was oxidised during

this annealing process to form SiO_2, while the boron was diffused simultaneously into the underlying poly-Si gate, forming the p^+-poly-Si gate. The formed oxides on top of the poly-Si gate were then dipped away. Al metal was then deposited and patterned for contacts.

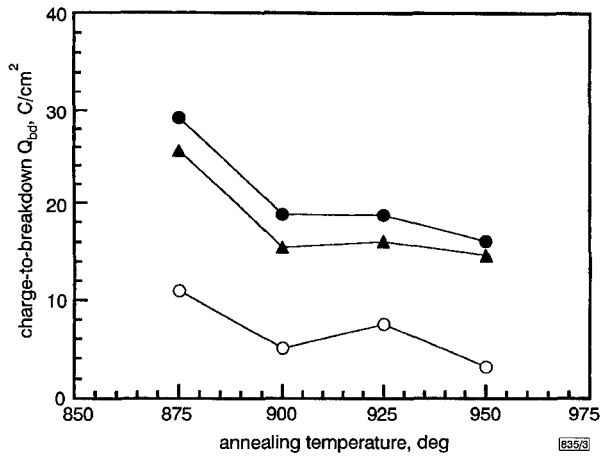

Fig. 3 *Average of charge-to-breakdown of BF_2^+-implanted, B^+-implanted and Si-B samples annealed at 875–950°C for 15min*

● Si-B
▲ B^+
○ BF_2^+

Result and discussion: To evaluate boron penetration, the flat-band voltage, V_{fb}, measured from the high-frequency C-V curves, is applied. Boron penetration causes a positive V_{fb} shift. More severe boron penetration results in a larger V_{fb} shift. Fig. 1 shows V_{fb} against different annealing temperatures from 875 to 950°C for 15min. The BF_2^+-implanted sample exhibits the largest V_{fb} shift resulting from the F-enhanced boron penetration. More importantly, although the B^+-implanted sample has a smaller value of V_{fb} than the BF_2^+-implanted sample, the V_{fb} shift is smallest for the Si-B sample. The Weibull plots of the charge-to-breakdown value for the BF_2^+-implanted and Si-B samples are shown in Fig. 2. The stress current density is 100mA/cm^2 and the gate area of the capacitor is 4.42×10^{-5}/cm^2. There are two groups clearly separated in the Figure. For the BF_2^+-implanted samples, the Q_{bd} is distributed over the wide range 1–10C/cm^2 for the annealing temperatures studied. In addition, they also depict a lower Q_{bd} value

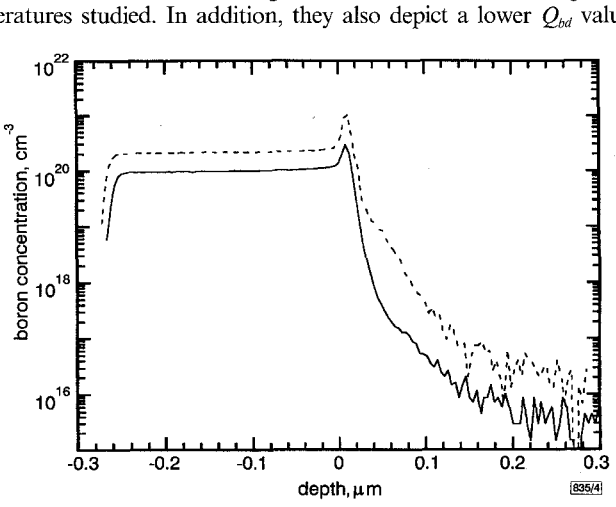

Fig. 4 *Boron profiles of BF_2^+-implanted and Si-B samples, measured by SIMS analyses*

925°C, 15min
——— Si-B
– – – – BF_2^+

compared with the Si-B samples. For the Si-B sample, the Q_{bd} distribution is much tighter and also higher in value. For the Si-B sample, the Q_{bd} decreases as the annealing temperature is increased. The average Q_{bd} for the Si-B, B^+-, and BF_2^+-implanted samples are compiled and shown in Fig. 3. The Si-B sample exhibits the largest Q_{bd} for all of the temperature range. The B^+-implanted sample is in-between the Si-B and BF_2^+-implanted samples. Fig. 4 shows the boron profiles of the Si-B and BF_2^+-implanted samples measured by SIMS analyses. The Si-B samples indeed show a smaller B concentration at both the SiO_2/Si interface and in the Si-substrate.

Conclusion: In conclusion, a novel Si-B diffusion source for a p^+-poly-Si gate in pMOSFETs has been investigated, for the first time, in this study. This process shows a better performance for suppressing boron penetration than conventional BF_2^+-or B^+-implanted samples, for a wide range of annealing temperatures and times. This new process is a very promising candidate for fabricating surface-channel *p*MOSFETs in future deep-submicron CMOS.

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Thermally evaporated ITO/GaAs Schottky barrier contacts

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ITO/*n*-GaAs Schottky barrier contacts have been fabricated by thermal evaporation of In_2O_3/SnO_2 on GaAs with various deposition rates r_D. The variation in the contact characteristics was systematically investigated with respect to the deposition rate. The optimal deposition rate of 0.2Å/s yields a barrier height of 0.80eV and unity ideality factor with a transmittance value of >80% in the visible region of the spectrum.

In recent years, considerable attention has been given to transparent electrically conducting thin films, especially indium tin oxide (ITO), because of their unique properties which make them useful in many applications. ITO films are characterised by a high visible transparency ($T > 80\%$) and a low electrical resistivity ($\rho \simeq 10^{-4}\Omega$cm), thus providing a very good Schottky contact to GaAs and InP photodiodes, solar cells [1, 2] and, more recently, optical HBTs [3]. In a previous paper [4], we reported the excellent radiation resistance of the ITO films [4]. Despite the significant progress in the use of ITO in device structures, surprisingly little research has been devoted to the fabrication of thermally evaporated ITO layers on semiconductors [5]. At present, there is no information about the role of deposition rate in opto-electronics properties of ITO layers.